IEEE

1999

INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM

http://www.irps.org/

March 22-25, 1999

TOWN & COUNTRY HOTEL
500 Hotel Circle North
SAN DIEGO, CALIFORNIA 92108
TELEPHONE: (800) 77-ATLAS
(619) 291-7131

Sponsored by
the IEEE Electron Devices Society
and
the IEEE Reliability Society

HIGHLIGHTS* FOR 1999:

Tutorials	Monday	8:00 a.m.-5:00 p.m.
Workshops	Monday	7:30 p.m.-9:30 p.m.
Equipment Demos	Mon.-Thurs.	by Appointment*
Technical Program	Tuesday	8:15 a.m.-5:20 p.m.
"	Wednesday	8:15 a.m.-5:45 p.m.
"	Thursday	8:15 a.m.-4:05 p.m.
Aquarium	Tuesday	6:30 p.m.-9:45 p.m.
Banquet Reception	Wednesday	7:00 p.m.-8:00 p.m.
Awards Banquet	Wednesday	8:00 p.m.

*Read about details in this program

GENERAL INFORMATION

ADVANCE INFORMATION—Avoid delays and extra expense by registering in advance using the form in the center of this program. Mail it with a check or register via fax (315-336-9134) or on-line at www.irps.org/ with a credit card. Advance registration fees apply only to remittances postmarked on or before March 5, 1999. Written cancellation requests will be honored up to March 5, 1999.

SYMPOSIUM REGISTRATION FEES*

	IEEE Member	Non-Member
Advance Registration	$260	$310
Registration at Symposium	$310	$360

TUTORIAL ATTENDANCE FEES**

Advance Tutorial Fee	$210
Door Tutorial Fee	$250

Apply for IEEE membership at ieee.org/join.html. At the Symposium membership application forms will be available near the registration desk also. For additional registration information, see the card in the center of this program or at www.irps.org/.

*Includes copy of Symposium Proceedings (hard copy & cd), workshop attendance, and banquet ticket. Additional banquet tickets may be purchased in advance or on arrival at a cost of $25 per ticket.

** Tutorial fee includes a bound set of notes for all tutorials (including the ones you don't attend). Please register in advance and indicate tutorial selection on your advance registration form so that appropriate room arrangements can be made for each tutorial subject.

REGISTRATION HOURS

The registration desk will be open at the following times:

Sunday, March 21	4:00 p.m.-9:00 p.m.
Monday, March 22	7:00 a.m.-8:00 p.m.
Tuesday, March 23	7:00 a.m.-3:00 p.m.
Wednesday, March 24	8:00 a.m.-3:00 p.m.
Thursday, March 25	8:00 a.m.-2:00 p.m.

HOTEL RESERVATIONS

Attendees will make their own reservations using the form in the center of this program. Note that a one-night deposit or a credit-card guarantee is required with your room reservation. Early reservations are strongly recommended.

The Town & Country Hotel has reserved a block of rooms until *February 19, 1999* for Symposium attendees at special single/double rates of $89 for accommodations in the East Garden; $99 in the East Tower/West Garden; and $109 in the West Tower. When making reservations, refer to "IRPS".

A limited number of rooms is also available at government rates for qualified government employees. Government employees must show identification at hotel check-in to receive the government rates.

SYMPOSIUM PROCEEDINGS (hard copy and cd)

The Proceedings will be provided at the Symposium. Additional copies of the Proceedings can be ordered/purchased from: (1) IRPS Registration using the registration form via on-line, fax, or mail; (2) IRPS Registration at the Symposium; (3) IEEE after March 25 via mail order through the IEEE Service Center, Single Copy Sales Unit, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331. For IEEE Service Center credit card/cash sales call 800-678-IEEE. Request IEEE Catalog No. 99CH36296. A substantial discount will be allowed IEEE members.

PAST PROCEEDINGS/TUTORIALS/VIDEOTAPES—A limited number of past proceedings, past tutorial notes, and previous years' videotape sets will be sold in the Past Publications Booth near the Symposium registration area. The booth will be open during regular registration hours.

VIDEOTAPES—Orders are being taken for a five volume videotape set of the '99 paper presentations. Order using the registration form via on-line, fax, mail, or at the Symposium. Please order by March 25.

GENERAL CHAIR'S GREETING

Welcome to the 37th annual International Reliability Physics Symposium! The Technical Program and Management committees have assembled an outstanding program of technical and social events for this symposium that I think you'll find educational and enjoyable.

Monday will start with a program of 10 tutorials, with topics ranging from a review of Dielectric Reliability to Intellectual Property Law. The tutorials are taught by recognized experts in their fields and are a great way to learn something new or enhance your present understanding of a topic. Starting Monday afternoon and continuing into the evening, the Workshops are a favorite place to talk about new topics, where the conversations are unrestrained, open and stimulating. This year, we are holding the failure analysis workshop in the afternoon, immediately after a failure analysis tutorial, so it won't conflict with the techniques workshops held that evening. Also new this year, we are using the IRPS web site for Workshop sign-ups prior to the conference.

Alan G. Street
General Chair

The Technical Program starts Tuesday morning and runs through Thursday afternoon. Details of the Technical Program are in the Technical Program Chair's greeting on the next page. As in previous years, we are using digital projection, which not only makes the visuals easy to see, it allows us to make the PowerPoint presentations available to you from our web site.

The Equipment Demonstration program opens Monday afternoon and continues through Thursday morning. Unlike a trade show, the Demo program allows equipment manufacturers to set up a demo laboratory where you can privately evaluate your samples and discuss the equipment. See the Equipment Demonstration section of this program or the IRPS web site for more details and a list of demonstrators.

In addition to the Technical Program, we have a number of social events throughout the week. Our Tuesday evening reception will be held at the Stephen Birch Aquarium in La Jolla. Overlooking the Pacific ocean, the aquarium is an ideal setting to relax, catch up with old friends and meet new ones. On Wednesday evening we will have our Annual Awards banquet, with presentations for the best paper awards for 1998. Finally, the companions program offers an excellent overview of the city and can help you plan later excursions on your own. Details of these events are available in the Arrangements section of this program.

Both San Diego and the Town & Country Hotel have changed quite a bit since the IRPS was last held here in 1992. The hotel has made a number of significant improvements, and the city has a new downtown shopping and nightlife area called the Gaslamp District, as well as the new San Diego trolley. The trolley is a light rail system that connects much of the city, including stops at Old Town, the Gaslamp District, Qualcomm Stadium, the San Ysidro border crossing, and the Town & Country Hotel. Of course, the other attractions like Mission Bay, Sea World, The San Diego Zoo, and Balboa Park are still here, making San Diego one of America's most popular tourist destinations as well as a great place to hold the IRPS.

America's Finest City welcomes The World's Finest Reliability Physics Symposium - And I look forward to seeing you at the IRPS in March!

Alan G. Street
General Chair

Technical Program Committee Chair's Welcome

The Technical Program – the heart of the symposium – will feature 67 papers chosen from the global microelectronics community and present the latest findings in reliability physics and engineering. Additionally the symposium includes our traditional Monday tutorial program, which this year will feature 10 tutorials that provide in-depth presentations of important reliability issues. The Monday night workshops supplement the Technical Program and tutorials and provide an opportunity for informal, in-depth discussions in 11 topic areas. Please be sure to sign up for the workshops using the IRPS web page at http://www.irps.org/ws/fram_ws.htm.

Tony Oates
Technical Program Chair

This year the Technical Program went electronic. For the first time we solicited electronic abstract submissions. The response was very encouraging with over 50% of the total number of abstracts submitted electronically. Abstracts were received from 22 countries, and were reviewed by a team of 75 industry and academic experts in reliability engineering and physics. These committee members are all volunteers and their efforts in selecting very high quality papers for the symposium are to be commended. The Technical Program Committee is organized into sub-committees dealing with specific areas of reliability physics. This year's sub-committees focused on traditional favorites at the IRPS such as failure analysis, interconnects, device and process, ESD and latch-up, device dielectrics, compound semiconductors, and hot carrier aging, as well as newer areas of reliability concern involving plasma process induced damage and micro-electro-mechanical systems (MEMS). The arrangement of paper sessions within the Technical Program reflects this sub-committee structure.

The Technical Program begins on Tuesday with a keynote presentation by Dr. Harald Eggers, who is Vice-President of Manufacturing for Siemens Inc. He will address reliability and business challenges for advanced memory development. The following plenary session discusses the latest developments in the effects of device design and structure and process related issues on microelectronics reliability. The remainder of the Program has been arranged to include parallel sessions, which have been arranged to minimize the overlap between subject areas. The Tuesday afternoon sessions cover dielectric breakdown mechanisms and Compound Semiconductors. The Wednesday morning parallel sessions deal with ESD and Latch-up, MEMS reliability and Interconnect. The Interconnect session continues through Wednesday afternoon, together with a parallel session on Hot Carrier effects on circuit reliability. The hot carrier session includes the best paper from the 1998 ESREF meeting, included here as an invited paper. Failure analysis methods, packaging and assembly and plasma-induced damage are the topics for Thursday morning's parallel sessions. The conference concludes with a plenary session discussing stress – induced leakage currents (SILC) in ultra-thin gate oxides.

I look forward to seeing you in San Diego!

Tony Oates
Technical Program Chair

ARRANGEMENTS INFORMATION

Chair: **Mike Stover, LSI Logic**

Vice Chair: **Cleston Messick, Fairchild Semiconductor**

The IRPS is pleased to host this years symposium at the Town and Country Hotel located in San Diego. Maps and information are available online at http://www.sandiego.org/start.idc.

TRANSPORTATION

Reduced rates with American Airlines, Southwest Airlines and Thrifty Rent a Car have been arranged for conference attendees and their guests. Please refer to the back of this program for specific details. Ground transportation between the airport and the hotel by shuttle or taxi is available for a nominal fee. The Town and Country is approximately 6 miles from the airport, and offers ample self parking facilities for your vehicle.

The hotel is only minutes by motor transportation from the from a wide assortment of restaurants,museums, night clubs, and other attractions. The public trolley with frequent and inexpensive service to Old Town, Downtown, Bayfront and the border departs from the back of the property. Both taxi and bus service depart from the main hotel entrance.

CONFERENCE ACTIVITIES

The symposium registration, technical program, tutorials, and equipment demonstrations are all located in the Convention Center. The workshops are split between the main and the mezzanine levels. Workshop rooms will be assigned on the basis of sign-ups. (Please refer to the hotel map on the back of the advance program). The conference registration will take place in the Mission foyer. Past proceedings sales desks are located in the foyer of the Atlas Ballroom. Technical sessions will take place in the Atlas Ballroom. The coffee break sponsor tables, and break area will be in the foyer of the Atlas Ballroom and the equipment demonstrations are housed in the Lower Level Exhibit Hall, just downstairs.

TUESDAY NIGHT RECEPTION

This years reception and buffet will be held at the Stephan Birch Aquarium-Museum. Bus service will be provided for symposium attendees and companions beginning at 6 p.m. This new facility features a spectacular location overlooking the Pacific Ocean. With thousands of sea creatures in 34 exhibits, including a two-story kelp forest tank with larger fish and giant marine plants, this facility allows you to experience a dazzling variety of marine life in realistic habitats. You can explore the nation's largest marine science mueseum, with deep dive simulator, and other multimedia attractions. Experience the panoramic vista while dining and meeting with friends old and new.

WEDNESDAY EVENING SYMPOSIUM BANQUET

The Award Banquet will be held on Wednesday March 24 at 8:00 p.m. in the Atlas Ballroom. A no host reception prior to the banquet will be held from 7:00 p.m. - 8:00 p.m. in the Atlas Ballroom foyer. The awards for the IRPS 98 Best and Outstanding Papers will be presented at the banquet. Registered attendees receive one ticket to attend the banquet. Additional tickets may be purchased at the Conference Registration Desk for $25 each.

HOTEL DINING

With 5 restaurants on site, something to suit a wide range of tastes and budgets can be found. For a quick bite, cold drink or a little diversion you'll enjoy Charlie's for fun , food and spirits. The Lanai coffee shop features lighter fare and serves breakfast, lunch and dinner. Adjacent is the Sunshine Deli, for meals on the go - Deli sandwiches and snacks, fresh baked pastries and cookies, cold drinks. Kelley's Steakhouse for lunch, dinner or cocktails is the place to go for Prime Rib, Steaks, and Chicken. Trellises Garden Grille serves breakfast lunch and dinner with a wide variety of creative appetizers, pastas, and pizzas, fresh seafood, and delicious desserts.

LOCAL ATTRACTIONS

With many famous local attractions like the San Diego Zoo, Sea World, Old Town State Park, Mission and Coronado Bay, and Wild Animal Park nearby, something of interest is sure to be found. One of the largest shopping malls in the area, Fashion Valley, is short walk from your room, with over 200 stores on two levels, a brand new 18-screen theatre, and a 10-restaurant food court. To help plan your visit and learn what's new in San Diego , you might link to the San Diego Visitors Bureau at http://www.sandiego.org/new.idc.

COMPANIONS' PROGRAM

The IRPS, is again, pleased to offer a Companions' Program. The tour will be one day, and will include a city tour of San Diego, shopping at two of the cities most outstanding complexes, and lunch at the world famous Hotel Del Coronado. In addition there will be a Hospitality Suite, for spouses and guests of IRPS attendees, open Monday through Thursday, 8:00 a.m. to 10:00 a.m.. For more information on the Companions' Program please contact Sandy Barber, P.O. Box 2098, Banner Elk, NC 28604-2098, or phone 828-898-6375 (Monday through Friday, 10:00 a.m. to 4:30 p.m. EST), or send an Email to: sandyirps@aol.com.

EQUIPMENT DEMONSTRATIONS

Chair: **Eric S. Snyder, Sandia Technologies, Inc.**
Vice Chair: **Marsha Abramo, IBM Microelectronics**

The Equipment Demonstration program of the IRPS focuses on providing attendees with an opportunity to learn about reliability software and equipment in a confidential, "hands-on" fashion. Unlike typical trade events, sales pressures are minimized, and manufacturers are prepared to help attendees learn about, and test their latest equipment and software developments. Attendees are strongly encouraged to contact the demonstrators prior to the conference, and to make arrangements to bring their own samples, if desired. The following abstracts provide an overview of the nature of each company's demonstration, along with contact information. The **www.irps.org** web site will contain the latest information as more demonstrators are added to the program.

Demonstrators and other companies providing a variety of reliability physics products and services are also represented in the coffee break area. There, they will provide information on their products and sign-up sheets for demonstrations. You can sign-up for demonstrations at any time during the conference. This service is included in your registration and you can sign-up for as many demonstrations as you like, on a first-come, first-serve basis. *So there is really no better way to evaluate so many state-of-the-art systems, and to collect so much information on services, latest equipment, and software developments ...than to participate in* ***IRPS Demos****!*

The coffee break area is located adjacent to the Technical Program and the demonstration areas is in the Lower Exhibition Hall. Hours for equipment demonstrations are as follows:

Monday, March 22:	Noon - 5:00 p.m.
Tuesday, March 23:	7:30 a.m. - 5:00 p.m.
Wednesday, March 24:	7:30 a.m. - 5:00 p.m.
Thursday, March 25:	7:30 a.m. - Noon

DEMONSTRATORS

Demo #1: RELIABILITY TEST SYSTEMS FOR PACKAGE LEVEL AND WAFER LEVEL CONVENTIONAL RELIABILITY TESTING—Aetrium Incorporated, Randy Snede (651) 704-1800; Fax (651) 704-0339

Aetrium will demonstrate its revolutionary new Model 1164 Reliability Test System, which provides capabilities for Electromigration,

Copper Electromigration, Hot Carrier, and TDDB (Constant Voltage, Constant Current, V-Ramp, J-Ramp). Modular design eliminates scanning while providing high performance, flexibility, and low cost. Small, innovative ovens for standard applications, and conductive thermal control sysytem for high power devices are integrated to eliminate cables and provide multiple temperatures in all systems. Friendly, full-featured software provides easy system operation and lifetime predictions.

Demo #2: DATA ANALYSIS TOOLS AND PROCESS EVALUATION TEST SYSTEMS—Micro Instrument Co., Ted Nation, (760)746-2010; Fax:(760)746-0433; www.microinstrument.com

Micro Instrument Company will provide a hands-on demonstration of new testing capabilities in the PE9000A test system for constant current electromigration and time dependent dielectric breakdown. Also shown is the PE9020A for testing up to 350 °C. The PE9020 accepts instrument cards for electromigration and t_{ddb} test, and may be used for wafer level evaluation or packaged tests. Both system accept the new series 600 instrument cards which provide greater measurement resolution in voltage and current. Hot Carrier Degradation testing is demonstrated in the PE9010.

Demo #3: TURN-KEY SEMICONDUCTOR RELIABILITY TEST—QUALITAU INC., Sigal Einspruch, 972-8-9365566; Fax: 972-8-936-5577; www.qualitau.com

QualiTau will exhibit a turn-key semiconductor reliability test solution for performing electromigration, dielectric breakdown and hot carrier degradation testing for package and wafer level, featuring various plug-in modules and complete analysis software. The MIRA (Modular Integrated Reliability Analyzer) enables a process or reliability engineer to run several applications in parallel with many different configurations and capacities. In addition two new products will be presented: MIRA INFINITY is a massively parallel testing solution for traditional wafer-level reliability. ACE is a pulsed Electromigration system with a dedicated temperature control and a current source for every DUT.

Demo #4: ACOUSTIC MICRO IMAGING (AMI) TECHNOLOGIES, SYSTEMS AND SERVICES -Sonoscan, Inc., Steve Martell, (630) 766-7088; Fax: (630) 766-4603; info@sonoscan.com

Sonoscan is introducing a new series of digital C-SAM™ Acoustic Microscopes designated D9000. These systems feature faster and more accurate scanning up to the theoretical limit of the speed of sound. The D9000 is equipped with pulser/receivers having 500 MHz bandwidth, which will accommodate virtually any reflection mode, high frequency transducer available on the market. The D9000 will produce images with up to 8192 x 7680 scan points. Sonoscan's new Visual Acoustics™ operating software is extremely simple to use and operates under Windows® 98. New features include automatic sequential micro slice layers of samples, 3D reconstruction of an "acoustic solid" and interactive analysis guide for new users.

Demo #5: FAST WAFER LEVEL RELIABILITY ASSESSMENT OF SEMICONDUCTOR PRODUCTS—Reedholm Instruments, Sonja McElroy, (512)869-1935; Fax:(512)869-0992; www.reedholm.com

Reedholm Instruments will demonstrate equipment for performing fast wafer level reliability assessment of semiconductor products. The equipment is fully automated and supports in-line process reliability control. Test wafers with a variety of test structures will be used for performing a large variety of reliability tests. Reedholm will demonstrate how customers can gather statistical reliability control data in a few minutes per wafer. The design methodology behind self-heated structures will be explained and demonstrated. Additionally, testing of visitor supplied test chips may be accomplished using a manual test

station. Visitors are encouraged to bring their own test chips for this demonstration. This can be coordinated through Reedholm in advance.

Demo #6: LOW NOISE, LOW CURRENT ANALYTICAL PROBING—The Micromanipulator Co., Karen Schanhals, (702)882-2400; Fax: (702)882-7694; www.micromanipulator.com

Probe at resolutions of up to 0.05 microns using Micromanipulator's 8860 semi-automatic analytical test station. Take measurements at very low femtoamp levels and at high temperature using triaxial probes, triaxial chucks, integrated shielding and unique high-stability probes. Examples of incorrect test setup which can introduce unwanted leakage, electrical and/or physical noise into probing measurement and practical solutions to these problems will be presented at Micromanipulator's workshop. Additionally work with UV laser light for high resolution passivation removal and visible laser light for conductor separation on integrated circuits for failure analysis and fault isolation. Then use equipment that is linked by software control for the transfer of positional data to tabular and graphical analysis programs.

Demo #7: TOTAL PACKAGE FOR FLIP CHIP INSPECTION—Sonix Inc., Jim Stradling, (703)440-0222; Fax: (703)440-9512; www.sonix.com

Sonix will demonstrate the total package approach for flip chip inspection. Ultra high frequency transducers (180 MHz+) combined with a matched pulser and 8 GHz sampling allow for signal verification, superior resolution, and imaging capabilities. Using the total package approach, the system evaluates underfill and solder ball attachment. Sonix will also introduce a non-destructive wafer inspection and marking system.

Demo #8: BACKSIDE EMISSION MICROSCOPY: DEMI JR. DOCKING EMISSION MICROSCOPE SYSTEM—Hypervision, Dan Hurley, (510)651-7768; FAX (510)651-1415

The DEMI Jr. Docking Emission Microscope portable assembly allows inspection of DUT's on ATE test heads and wafers in automatic probers. Includes custom insertable optics with high numerical aperture, motorized X-Y-Z microscope with 16M zoom, boom-mount with portable stand and overlay subtraction software. Available as an option or standalone system.

Demo #9: EMISSION and ATOMIC FORCE MICROSCOPY, 300 mm WAFERS, LOW NOISE TESTING—Karl Suss America, Inc., Paige Lowry, (802)244-5181; FAX (802) 244-5103; www.suss.com

Karl Suss will display new, innovative probing solutions related to emission microscopy, 300 mm wafers and low current/low noise temperature testing. The SUSS topside/backside probing systems integrated with an emission camera solves the problems relating to the detection of IR emissions through several layers of metalization. Wafer, as well as, packaged parts can be probed from the topside, backside and at temperature. Several configuration options and accessories are available, including probeheads, probecards, and thermal chuck.

Demo #10: TEST SYSTEMS THAT PERFORM HIGH RESOLUTION *IN SITU* MEASUREMENTS—Destin N.V., Luc Tielemans, +32-11-21-46-36; Fax: +32-11-21-46-26

DESTIN test systems perform high resolution *in-situ* measurements to monitor the degradation of test samples. This technique allows the performance of reliability tests in short test times (typically a few days to a week) at low stresses. This will be demonstrated for both electromigration and thermal degradation of packages. The software package "Failure" is a powerful tool to analyze reliability data. This program allows the prediction of lifetime and calculates the uncer-

tainty on the prediction. The IDDQ failure analysis test system is a helpful tool to locate failures with the aid of liquid crystals or emission microscopes.

Demo #11: SOFTWARE SOLUTIONS FOR CAD NAVIGATION AND YIELD ENHANCEMENT—Knights Technology Inc., Scott Shen, (408)522-8880; Fax:(408)739-4438; www.knights.com

Knights Technology will demonstrate its Merlin's Framework™ CAD Navigation software. New this year are several features that increase FA efficiency, including Bitmap, SGEN (Schematic GENeration), Schemview, I-Schem (Interactive Schematic), K-Edit, and Remote Log-In. The new FA Wizard™ failure analysis process guidance and multimedia reference package will also be demonstrated as well as our YieldManager® yield enhancement software.

Demo #12: TURN-KEY WAFER LEVEL RELIABILITY SYSTEM—Keithley Instruments Inc., Tim Turner, (800) 552-1115; www.keithley.com

Keithley Instruments will demonstrate a turn-key system solution WLR testing. This package features test structures and methods developed by Tim Turner optimized for wafer-level testing in a production environment. The value of data collected, pad usage, and test time for production monitoring are all optimized. The solution includes test structure design and documentation, robust test algorithms, test programs, and data analysis. New developments include test structures and methods designed to test electromigration in metal at stud vias and at plug contacts, and new techniques for testing oxides of less than 100 Å.

Demo #13: AUTOMATIC & SEMI-AUTOMATIC PROBERS—Cascade Microtech, Veronica Miller, (503) 601-1182; Fax: (503) 601-1140; www.cmicro.com

Cascade Microtech will demonstrate their new PS21 parametric autoprober with eight inch capacity, 25 wafer cassette, femtoAmp level 48-pin probe card interface, and -55 to 200 degree C guarded thermal chuck with <5 picoFarad capacitance. In addition, the new Summit series semi-automatic analytical probe stations. The new Summit probers offer fast transition, -65 to 300 degree thermal chucks optimized for all WLR disciplines. Included in the series is the new Summit 12861 for DC/CV characterization featuring the patented AttoGuard™ thermal system with < 1 picoFarad chuck capacitance, 3 femtoFarad chuck variation, < 20 femtoAmp noise and leakage, and 50 milliSecond recovery time from a 100 Volt pulse.

Demo#14: LONG TERM AND FAST ON-WAFER RELIABILITY TESTING—Hewlett Packard Company, Jay Thomas, (408)553-2212; www.hp.com/tmo

Hewlett-Packard and Sandia Technologies will introduce the first published predictive WLR applied to Copper/low-k process development. For benchtop needs, HP will show charge pump, mobile ion, flash and latchup tests on the HP 4155/4156 DC parameter analyzers. TDDB testing to 384 pins can be done by adding an HP reliability matrix and multiple site probing solution provides 300C temperature testing. For production testing, HP introduces the HP 4072 Semiconductor Parametric Tester. It expands the HP 4071 functionality with high frequency applications such a ring oscillator and flash reliability testing. HP is also introducing enhanced PDQ-WLR test software and integrated analysis tools for fast WLR as well as detailed qualification and development.

Demo #15: VERSATILE EOS/ESD SUSCEPTIBILITY TEST INSTRUMENTS—Oryx Instruments, Mark Guillaume, (510)249-6312; Fax:(510)249-1150; www.oryxinstruments.com

Oryx will introduce Transient Latch-up test capabilities in the Model 11000 Stress Test System, a comprehensive tool for determining

susceptibility to ESD and Latch-up. Oryx will also introduce new features in the Model 700 Manual ESD and 9000 CDM systems. Device testing will be available, but please contact the factory prior to IRPS to arrange appropriate device fixturing.

Demo #16: ELECTRICAL CHARACTERIZATION OF INTEGRATED CIRCUITS FOR FAILURE ANALYSIS—UltraTest International, Bob Herriford, (408)433-2244; Fax:(408)433-5508

UltraTest will demonstrate their MultiTrace DC Parametric Test and Automated Digital Curve Tracer. Basic curve trace concepts, techniques and interpretation of waveform results will be discussed. Also demonstrated will be the systems capability to perform DC parametric testing, logical pre-conditioning, CMOS Latch-up testing with up to 50A capability and new "curve compare" software. UTI will introduce several new software features and significant improvements in the system's "vectoring" capability, including IDDQ. Also, MiniTrace will be introduced as a new system dedicated to Digital Curve Tracing (both unpowered and powered) for devices up to 216 pins with greatly reduced fixture costs. Individual hands-on demonstration of the system may be scheduled.

Demo #17: PORTABLE EMISSION MICROSCOPY—Alpha Innotech Corporation, Peter Brown, (408)307-4603; Fax: (510)483-3227; www.alphainnotech.com

The Alpha Innotech FA-1000 is a unique portable Emission Microscope that uses a new technology, which eliminates the previously required stationary dark box, without giving up the sensitivity of the conventional FA environment. Thus, it can be taken out to the tester or prober on the test floor to examine a device under test. The Alpha Innotech software is designed for ease of use by FA Product, Production, or Design Engineers. Backside Emission Preparation is also available. Come to see emissions being collected during IRPS or bring your sample for testing on the FA-1000.

Demo #18: LASER SCAN MICROSCOPE FOR FAILURE ANALYSIS—Carl Zeiss, Inc., Buddy Bossmann, (800)233-2343; Fax: (914)681-7446; www.zeiss.com

The Zeiss LSM 321 (Laser Scan Microscope) is a Failure Analysis workstation that provides a unique array of tools for the localization & analysis of failures in microelectronics. A multitude of information can be collected quickly & efficiently by using one of the available techniques: High Resolution Confocual Imaging; 3-Dimensional Imaging; Emission Microscopy; OBIC; Infrared Imaging; Flourescence & Polarized Light Imaging. The LSM can perform these analysis for packaged parts or wafers. The latest addition to the LSM capabilities is Spectral Analysis of Photoemission. The EmSpec option provides direct imaging of the spectral content of the light emission.

Demo #19: OXIDE AND HOT CARRIER TESTING AND SIMULATION—BTA Technology, Inc., Bob Xu, (408)986-1011; Fax: (408)986-1012; www.btat.com

BTA will demonstrate BTABERT, transistor level reliability simulation software, and how to use BTABERT-HCI to generate realistic hot carrier AC design rules for deep submicron technologies and to predict circuit lifetime due to hot carrier degradation. BTA will also demo how to use BTABERT-TDDB to evaluate oxide reliability of circuits, and how to use TDDBWorks to select the burn-in conditions to screen out infant failure. You can also take a look at Glacier, the gate level hot carrier reliability simulation and characterization software, and RelPro+, the hot carrier and TDDB stress software.

Demo #20: MC500 AND TEM PREPARATION—SELA USA, Inc., Efrat Raz, (408)988-5151; Fax: (408)988-3322

The new MC500 System has been designed to allow fully automatic, reliable,and speedy cross-sectioning of both integral die and wafer level

samples. Aninnovative approach facilitates processing of segments down to a minimum sizeof 4.2 x 2.1mm. This also allows cross-sectioning of edge dies, too. Dedicatedsoftware enable automatic mapping and planning of a single target or multipletargets and features automatic off-loading for immediate inspection. Thisaccessibility, together with high throughput (15min/sample), high accuracy(less than 0.5 micron), and excellent quality of cross-sections, significantlyreduces the diagnostic cycle for both failure analysis and process monitoring.

Demo #21: BENCHTOP MEMORY TEST SYSTEM—Micro Control Co., Kim Knutson, (612)786-8750; Fax:(612)786-6543; www.microcontrol.com

Micro Control will demonstrate our new M-2, 200 MHz Benchtop Memory Test System and our latest high power (150W) Burn-in with Test system. These systems are ideally suited for Semiconductor Reliability Laboratory environments. We will have several new application notes in our demonstration area. Engineers will be on hand to discuss the various applications of our systems as well as the material contained in the literature.

Demo #22: REAL-TIME SPECTROSCOPIC PHOTON EMISSION MICROSCOPE (SPEMS) FOR FRONT-END AND BACKSIDE EMISSION DETECTION—SEMICAPS, Inc., Bruce Harley, (408)986-0121; Fax: (408)986-1059

SEMICAPS, Inc. will demonstrate the SPEMS 1000 System that includes: improved optics for the visible to NIR range, greater illumination through a CCD camera, motorized XYZ stage movement, and software that is suited for the failure analyst lab. The SPEMS software integrates the emission spectrum with the failure device mechanism through a patented Spectroscopic Mirror. The SPEMS is the quickest and most reliable non-destructive procedure for frontside and backside identification of failure mechanisms within the semiconductor environment. SEMICAPS, Inc., will also demonstrate the newly released SEMICAPS Image Capture and Processing System for the SEM and light microscope.

Demo #23: PACKAGE LEVEL RELIABILITY TEST SOLUTIONS—Cottonwood Technology Group, Inc., Judy Longhurst, 602-970-3333; 602-970-3322; www.ctgi.com

Cottonwood Technology Group offers package level reliability solutions for: (1) Power Cycle Testing, (2) Temperature and Humidity Testing, (3) In-situational Thermal Stress Testing. We will show how our solutions help quality and reliability engineers achieve greater effectiveness in their work by: (1) Decreasing test set up time from days to hours, (2) Reducing problem isolation time from weeks to hours, (3) Employing closed loop control to provide extremely accurate stresses, (4) Allowing trend data analysis while the stress is running.

Demo #24: SCANNING PROBE MICROSCOPE SYSTEM—Digital Instruments, Marlene Carlyle; (805)967-1400; Fax: (805)967-7717; www.di.com

Digital Instruments will demonstrate the Dimension 3100 scanning probe microscope (SPM) system which will (1) measure surface morphology using atomic force microscopy; (2) measure voltages applied to conductors using electric force microscopy; (3) measure carrier concentration and distributions in semiconductors using scanning capacitance microscopy; and (4) measure surface temperatures using scanning thermal microscopy. This SPM produces measurements of these and other parameters on a sample with very high spatial resolution (1-10 nm) with minimal or no sample preparation, without requiring vacuum and in a manner that is non-destructive to the samples. Attendees are encouraged to bring their own samples that we will image for them.

Demo #25: STATE-OF-THE-ART FOCUSED ION BEAM TECHNOLOGY—Micrion Corporation, Robin Lyness, (978)538-6700; Fax: (978)531-9648; www.micrion.com

Micrion Corporation will demonstrate its most current Focused Ion Beam (FIB) system. The system will include a variety of enhancements and greater resolution from Micrion's 50 keV ion column with less than 5 nm usable spot size. Attendees will be able to sit down and participate interactively using the latest focused ion beam technology, and as always, are encouraged to bring their own wafer or device samples for evaluating.

Demo #26: (Withdrawn)AUTOMATIC ESD AND LATCHUP TESTERS—Keytek, Suzanne Bellemore, (978) 275-0800; Fax: (978) 275-0850; www.keytek.com

Keytek will demonstrate four testers: (1) WAFERMASTER, the only wafer level ESD test system currently on the market. (2) PARAGON, an advanced ESD and Latch-up test system for testing from 256 to 1024 pin systems. The only system that tests beyond 512 pin devices. (3) ZAPMASTER, an automatic ESD and Latch-up test system. (4) RCDM, a Robotic CDM ESD test system. Attendees may also operate the equipment themselves, and time permitting, to perform ESD tests on one or two of their own devices. (Prior arrangements should be made to ensure appropriate DUT boards are available.)

Demo #27: LOW-COST QUICK, EASY I/O CHECKER—ICOM, Masao Kaji, (310) 544-0393; FAX (310) 541-8653

ICOM will demonstrate Nippon Scientific Company's FX Series, a user-friendly, PC-based automatic switch matrix and curve tracer designed for high pin-count devices. Although designed as a low-cost I/O checker, the FX Series can be upgraded for IDDQ testing. It can convert and run vector patterns to detect abnormal IDDQ current. It will hold on a failed vector, making it ideal for liquid crystal or SEM analysis. A low-cost alternative to LSI Testers, the FX Series will free up valuable test time. Designed to automatically find a hot spot, the FC201 Liquid Crystal System features a precise temperature controller (± 0.001 °C), software and a CCD camera.

Demo #28: OPTICAL AND E-BEAM SYSTEMS FOR THE FAILURE ANALYSIS AND DESIGN DEBUG OF COMPLEX DEVICES—Schlumberger, Pia Welch, (408) 437-7268; Fax: (408) 437-7238

Flip-chip packaging and dense interconnects have created a need for new analysis methodologies. Schlumberger has recently developed an innovative technology incorporating a laser beam that probes through the silicon and detects voltage swings directly on the active regions of transistors in CMOS ICs. The optical probing system and waveform results will be presented. In addition, Schlumberger will show the new Analog Measurement System (AMS). Design diagnosis time is minimized because mechanical probes are integrated into the Focused Ion Beam system. AMS also provides multiple FIB chemistries for probepoint creation and <10nm probe placement resolution for 0.18 µm technologies.

Demo #29: RELIABILITY MODELING, SIMULATION AND TECHNOLOGY DEVELOPMENT TOOLS—Silvaco International, David J. Warren, (408) 654-4353; Fax: (408) 496-6080; www.silvaco.com

Silvaco International offers reliability modeling tools. Through the power of it's unique TCAD Driven CAD, the ATLAS family of products is carefully designed to simulate all of todays semiconductor technologies. Be sure to check out the latest in precision reliability modeling with ORCHID and NOMAD. Visit our site at the conference for thorough demonstrations of all ATLAS products, plus the industry leading SmartSpice.

Demo #30: FULL LINE OF ELECTRON OPTICS AND SCANNING PROBE MICROSCOPES—JEOL USA, Inc., Bill Sousa, (978) 535-5900; Fax: (978) 546-2205; www.jeol.com

JEOL will be demonstrating one of it's new PC controlled Low Vacuum SEM'S. JEOL will also discuss it's full line of of electron optics based microscopes including SEM, TEM, EPMA and Auger; it's Scanning Probe Microscopes, vacuum evaporators and sputter coaters; as well as digital image acquisition, archiving and database management, line width metrology, defect review navigation, EDS integration.

Demo #31: MULTI-FUNCTION EMISSION MICROSCOPE FOR FA AND LASER MARKING IN SILICON AND FLAT PANEL DISPLAYS -- TnP Instruments, Inc., Nam Ly, (310) 532-2222; Fax: (310) 527-0470; www.tnpinstruments.com

TnP Model PEM-1000 is designed to perform as a Multi-functional system: Photon Emission Microscope for Failure Analysis and Laser Fault Marking for Silicon wafers and Flat Panel Displays of various sizes. In addition to the above-mentioned primary functions, the system can also be used as a Laser Repair System. The system is built around the standard Mitutoyo Microscope. Thus, current equipment could be retrofitted for PEM-1000 and current component utilized to minimize capital investment.

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- Sandia National Laboratories
- Viko Test Lab
- ASM Electronic Device Failure Analysis Society

TUTORIAL PROGRAM

Chair: **Carole Graas, SIEMENS Microelectronics**

Vice Chair: Bill Abadeer, IBM Microelectronics

The IRPS traditionally opens with a full day of Tutorials. The 1999 Program offers you opportunities to broaden your technical skills as well as your understanding of the microelectronics business environment. D. Dumin (Clemson U.), A. Witvrouw (IMEC) and M. Ibnabdeljalil (TI) will cover the fundamental reliability issues of dielectrics, interconnects, and plastic packages, respectively. Further discussion of these pivotal subjects is planned later in the day in matching workshop sessions (see workshop program).

In addition, technology-specific topics are introduced, some for the first time: Flash Memories, by N. Mielke (Intel); SOI Devices by D. Ioannou (George Mason U.); and Micro Electromechanical Systems by D. Tanner et.al. (Sandia National Labs). Alternatively, topics of critical general and economic interest are represented, including the design of reliability test structures, by J. Bordelon (Testchip Technologies); the selection of chip suppliers, by A. Kostic et.al. (IBM); and the competitive aspects of reliability and failure analysis, by T. Dellin (Sandia National Labs).

The Tutorial Program is a great value for IRPS attendees: with your tutorial registration fee, you receive a Tutorial Notes book including detailed abstracts and viewgraphs for all offered courses – not just the ones you attend. This amounts to over twenty hours of essential reference material. In order to facilitate meeting room planning, please register early and indicate your intended attendance choices on the registration card.

Monday March 22, 1998

Room	8:00 a.m. to 9:30	10:00 to 11:30	1:30 to 3:00	3:30 to 5:00 p.m.
Presideo	Topic 1		Topic 9	
San Diego	Topic 2		Topic 7	Topic 10
Friars/Padre	Topic 3		Topic 6	
Town & Country	Topic 4	Topic 5	Topic 8	

Topic 1. OXIDE WEAROUT, BREAKDOWN, AND RELIABILITY: THE PAST, PRESENT, AND FUTURE— D, Dumin – Clemson University, Clemson, SC (8:00 a.m. - 11:30 a.m., Presideo Room)

Oxide wearout, breakdown, and reliability will be reviewed from the mid-1960s to the present time. The various models that have been developed will be described and discussed. The state of our current knowledge will lead into a discussion of likely approaches to future work.

Topic 2. OEM COMPONENT SELECTION, QUALIFICATION, AND MONITORING— A. Kostic, G. Nelson, B. Bornstein - IBM , Hopewell Junction, NY (8:00 a.m. -11:30 a.m., San Diego Room)

The presentation is an overview of how Original Equipment Manufacturers (OEMs): (1) Select suppliers with which to do business;

(2) Identify supplier technology of interest to incorporate in end products; (3) Qualify supplier products for use in their application; and (4) Monitor and feedback performance to suppliers. The emphasis is on computer system manufacturer practices.

Topic 3. MEMS ACTUATORS: APPLICATIONS, FAILURE MODES, AND RELIABILITY—D. Tanner, S. Miller, and D. Plummer, Sandia National Laboratories, Albuquerque, NM (8:00 a.m. - 11:30 a.m., Friars/Padre Room)

As MicroElectroMechanical Systems (MEMS) become commercially feasible, reliability studies are crucial for success. This tutorial describes the various applications of MEMS sensors and actuators. We discuss reliability measurement techniques and how MEMS actuators fail. Several experiments of rubbing polysilicon surfaces, which indicate wear as a dominant failure mechanism, are summarized.

Topic 4. PROPER TEST STRUCTURE DESIGN FOR RELIABILITY PHYSICS EVALUATION—J. Bordelon, D. DeShazo, B. Tranchina, G. Yeric - TestChip Technologies, Inc., Dallas, TX (8:00 a.m. – 9:30 a.m., Town & Country Room)

Accurate reliability assessment requires test structures which do not introduce significant parasitic effects. Electrical and thermal properties of test structure layout must be carefully considered. This tutorial reviews common parasitics and layout techniques to minimize them for a number of important reliability physics failure mechanisms

Topic 5. IC PLASTIC PACKAGE RELIABILITY—M. Ibnabdeljalil and D. Edwards – Texas Instruments, Inc., Dallas, TX (10:00 a.m. – 11:30 a.m., Town & Country Room)

This workshop aims at giving an overview of the main reliability concerns in IC packages, with emphasis on plastic packaging. Though the overall geometry and materials in IC Packages have evolved to accommodate for more aggressive designs, the main concerns with IC package reliability have not changed much. These fall under 3 broad categories: 1) Solder joint reliability, and 2) resin delamination and cracking, and more recently 3) Inter-level dielectric failures.

Topic 6. RELIABILITY ASSESSMENT METHODS FOR INTERCONNECTS—A. Witvrouw, IMEC, Leuven, Belgium (1:30 p.m. – 5:00 p.m., Friars/Padre Room)

Electromigration and stress induced voiding are interconnect degrading mechanisms that become more critical as dimensions shrink. Both reliability issues are investigated in this tutorial. After a definition and some physical background, an overview will be given of the lifetime determining factors, sensitive measurement techniques and valid extrapolation methods for predicting the lifetime at user conditions.

Topic 7. COMPETITIVE RELIABILITY AND FAILURE ANALYSIS—T. Dellin – Sandia National Laboratories, Albuquerque, NM (1:30 p.m. – 3:00 p.m, San Diego Room)

The economic challenges facing the industry are as important as the technology challenges and will impact how we do reliability, as well as, the careers of reliability engineers. The major economic trends will be reviewed and their impact on how failure analysis and reliability add value will be considered.

Topic 8. FLASH MEMORY RELIABILITY—N. Mielke, Intel Corp., Santa Clara, CA (1:30 p.m. – 5:00 p.m., Town & Country Room)

This tutorial will review reliability failure mechanisms affecting non-volatile memories, with an emphasis on dielectrics. The focus will be on "NOR" Flash memories employing channel hot-electron programming and tunnel erase. Failure mechanisms will include disturbs, cycling degradation, and data loss.

Topic 9. BASICS OF SOI CMOS: PERFORMANCE AND RELIABIL-

ITY—D. Ioannou - George Mason University, Fairfax, VA (1:30 p.m. – 5:00 p.m., Presideo Room)

The basic physics of the SOI MOSFET will be covered, both for Partially Depleted and Fully Depleted operation, highlighting some unique features such as channel coupling and the floating body effects. This will be followed by a discussion of how these features impact performance and hot carrier reliability.

Topic 10. INTELLECTUAL PROPERTY—M. Lachuk, SAIC, San Diego, CA (3:30 p.m.-5:00 p.m., San Diego Room)

Abstract under construction

WORKSHOPS—Monday, March 22

Workshops #1 to #10: 7:30 p.m. - 9:30 p.m.

Workshop #11: 3:30 p.m. -5:30 p.m.

Chair: William R. Tonti, IBM, (wtonti@us.ibm.com)

Vice Chair: Neal Mielke, INTEL (nmielke@sc9.intel.com)

Eleven workshops covering important topics in reliability physics are available to all symposium registrants. Moderators will discuss topics of current interest and attendees are asked to participate, and share their thoughts prior to the actual workshop by sending e-mail directly to the moderators below. Attendees are encouraged to prepare questions or bring data on related topics which they may wish to discuss. Your data and questions can be posted on the website (irps.org/ws).

Overhead projectors will be available in the meeting rooms. Please note that the workshops will be held on Monday evening after the tutorials. Please register for the workshop of your choice either on-line, or alternately when you register for the symposium. Topics and moderators are listed below. For further information on the workshop program contact either William Tonti or Neal Mielke

Workshop 1. **Environmental-Stress Requirements for Certifying New Packages**

Moderators:

Phil Bechtold, Lucent Technologies, p.f.bechtold@lucent.com

Mike Stover, LSI Logic, stover@lsil.com

Nicholas P. Mencinger, Intel, Nicholas.P.Mencinger@intel.com

Changes in advanced semiconductor packaging materials to satisfy application specific requirements are drawing into question traditional reliability stressing methods. This workshop will focus on whether this methodology still makes sense in the current environment with respect to: relevant testing methods, linkage of these tests to the end use environment and lifetime expectations of semiconductor packages. Expectation is high for discussion concerning proposed alternative strategies for package certification.

Workshop 2. **Low Temperature Reliability**

Moderators:

Janet Wang-Ratkovic, AMD, janet.wang@amd.com

Ron Lacoe, Aerospace Corp., ronald.lacoe@aero.org

Jason Woo, UCLA, woo@icsl.ucla.edu

This workshop will focus on the reliability of microelectronics at low temperatures. Although many failure mechanisms are thermally activated, resulting in improved reliability as temperature is decreased,

there are known failure mechanisms, such as hot-carrier degradation and the effects of total ionizing dose radiation, which are enhanced at low temperatures. In addition, there are packaging issues associated with device operation at low temperatures. This workshop will discuss these and other related reliability issues of CMOS devices at low temperatures.

Workshop 3. **Dielectric Reliability (What does the data mean?)**
Moderators:
William Abadeer, IBM Microelectronics, abadeer@us.ibm.com
William Hunter, Texas Instruments, hunter@spdc.ti.com

Planning and execution for dielectric reliability data requires a discipline to ensure timely and meaningful information. It is a labor and time intensive effort in which, perhaps, one gets only one chance to make it work, and there is never enough time. There are two critical stages: first planning of the work, i.e., what do you need to do to get what you want, and secondly understanding what the data means. This workshop will concentrate on theses issues as they relate to: processing conditions, model for voltage (or field) and temperature, area dependence, process/device layout sensitivities (area vs perimeter, etc.), and DC vs transient conditions. The workshop will address how to plan for dielectric data with the existing constraints, and how to analyze the data for maximum information, and what conclusions or actions you should take based on it.

Workshop 4. **Hot Carrier by design. Is it possible?**
Moderators:
Giuseppe Larosa, IBM Microelectronics, larosa@us.ibm.com
Thomas Vogelsang, Siemens Microelectronics, v2vogels@us.ibm.com
Zihong Liu, BTA Technology, byx@btat.com

Hot Carrier (HC) reliability requirements are starting to become a limiting factor for the development of deep submicron technologies (< 0.25 μm). Global HC reliability rules, extensively used in the past , are starting to impact the performance/reliability tradeoffs to not acceptable levels. It is becoming more and more important to carefully quantify the link between DC HC studies and circuit reliability/performance requirements. This workshop will focus on possible methodologies to quantify circuit level reliability at very early stage in the technology development cycle. The main discussion will be on existing software tools to allow HC reliability by design, their limits and future developments to satisfy the needs of both reliability and circuit design. New stress/test methodologies to optimize and calibrate the reliability projections by simulation will be also covered.

Workshop 5. **ESD/Latchup for High Performance CMOS**
Moderators:
Timothy Maloney, Intel, timothy.j.maloney@intel.com
Charvaka Duvvury, Texas Instruments, duvvury@spdc.ti.com

ESD continues to be a major reliability threat as technologies advance further into the deep submicron regime and IC designs get more complex. This workshop will address the latest concerns for ESD including: 1) core damage, 2) new latchup issues and the tradeoff with ESD, 3) new packaging and processes, 4) building-in ESD reliability, 5) mixed voltage circuits, 6) Charged Device Model, 7) oxide reliability and charge trapping, 8) simulation and modeling efforts to solve ESD, 8) ESD testing standards, and 9) any other topics of interest to the audience.

Workshop 6. **Focused Ion Beam**
Moderators
Jan Reimer, Cirrus Logic, reimer@corp.cirrus.com
Marsha Abramo, IBM, mabramo@us.ibm.com
Ann Campbell, Sandia National Laboratories, ancampbe@sandia.gov

The FIB workshop brings together FIB practitioners to share their experience and those who are new to the field and want to become familiar with the diverse aspects of FIB techniques. Topics to be discussed include, but are not limited to, the challenges of high aspect ratio contact hole preparation and filling, design for repairability, is there reliability

in FIB micro surgery?, CAD layout overlay, and repair site navigation on deep submicron ICs.

Workshop 7. **How to deal with random failures?**
Moderators:
Fred Kuper, Philips Semiconductors, f.kuper@nym.sc.philips.com
Nick Lycoudes, Motorola, raqa01@email.sps.mot.com

In this workshop we want to exchange ideas and common practices on the response of an organization (wafer fab, assembly, customer interfaces,etc.) to random product reliability failures, identified during part reliability screening/testing, equipment manufacture or normal life. Does it make a difference where the random failures occurred? Furthermore, we want to discuss the practices for product reliability screening/testing. When is part screening (i.e. Burn-In, etc.) appropriate? What is the value of product reliability tests that consistently yield zero failures?

Workshop 8. **Why Wafer Level Reliability?**
Moderators:
Harry Schafft, NIST, schafft@piper.eeel.nist.gov
Eric Snyder, Sandia Technology, snyderst@aol.com
Tim Turner, Keithley, turner_tim@keithley.com

The WLR discussion group will focus on the status and accomplishments of various WLR standards and investigation committees. The work of the JEDEC Committee on WLR, JC14.2 will be summarized (including the results of recent inter-laboratory experiments) as will the status of ASTM standards for WLR tests. Also, the status of organizations such as the FSA and ESQMC, which are writing specifications that essentially encourage the use of WLR testing will be discussed. Attendee experience with any of these test techniques, standards, or activities will be solicited. The workshop is intended to generate a pooled knowledge of the various activities relevant to WLR.

Workshop 9. **Interconnect Reliability**
Moderators:
Jim Llyod, Lloyd Technology Associates, jlloyd@lta.ultranet.com
Carole Graas, Siemens, carole.graas@siemens-scg.com

Do you know how to answer your metallization reliability questions? Do you even know what questions to ask? These are changing times with new materials and challenges. At a time where cycle time and performance dominate process development, knowing the right test and what to do with the results is crucial. Please join a group of development and production engineers like yourself and share your views on testing Al or Cu-based systems, sincluding low "K" I.L.D.. All aspects of metallization reliability will be discussed. Topics will include, but not be limited to Electromigaiton, Stress Voiding, Defect Detection and Control, Corrosion etc.

Workshop 10. **MEMS: Phenomenological Theory or Bust**
Moderators:
Paul Boudreaux, Lab for Physical Sciences, Boudreau@eng.umd.edu
Sam Kayali, Jet Propulsion Laboratory, sammy.a.kayali@jpl.nasa.gov

MEMs reliability today is where semiconductor reliability was before we had activation energy concepts and accelerated life procedures using elevated temperatures. We have lots of empirical data that is often not reproducible and even contradictory. Tribological parameters can play havoc with experimental methods. Problems such as when to apply thin film characteristics versus bulk properties in a MEM design have yet to be clearly specified. With the lack of an in-depth a-priori first principles theory for reliability, a phenomenological theory is our next best goal.

Workshop 11. **Failure Analysis** ***(3:30 – 5:30 p.m.)***
Moderators:
Daniel L. Barton, Sandia National Laboratories, bartondl@sandia.gov
Edward I. Cole, Jr., Sandia National Laboratories, coleei@sandia.gov

This workshop will focus on recent failure analysis technique developments and analysis concerns for the current and next generation processes. Analysis techniques suitable for fault localization through the

substrate have become vital to the industry with the increasing use of multi-level metal processes and flip-chip packaging. Attendees are encouraged to prepare questions and presentation materials on issues current to their companies. This workshop is being coordinated by the newly formed Electronic Device Failure Analysis Society (EDFAS).

TECHNICAL PROGRAM

Tuesday, March 23, 8:15 a.m., Town & Country Room

SYMPOSIUM OPENING:

Alan G. Street, Symposium General Chair
Tony Oates, Technical Program Chair

KEYNOTE

RELIABILITY AND BUSINESS CHALLENGES FOR ADVANCED MEMORY DEVELOPMENT—H. Eggers, Siemens Inc., Dresden, Germany

DEVICE & PROCESS *(Session 1)*

Co-Chairs: Guido Groeseneken, IMEC and
Kin Cheung, Lucent Technologies

1.1 MICROPROCESSOR RELIABILITY PERFORMANCE AS A FUNCTION OF DIE LOCATION FOR A 0.25μm FIVE LAYER METAL CMOS LOGIC PROCESS—W.C. Riordan, R. Miller, Intel Corp., Chandler, AZ, J.M. Sherman, Intel Corp., Rio Rancho, NM, and J. Hicks, Intel Corp., Santa Clara, CA

Infant mortality performance of over one million microprocessor units was collected as a function of die location on the wafer. In this way, yield to reliability correlations could be made per die. It was found that burn-in failures matches sort yield maps and that die location sort yield correlates strongly to burn-in performance. Furthermore edge die and alternating row effects were observed. Using this technique burn-in failures could be traced to specific fabrication tools.

1.2 STUDY ON RELIABILITY OF Ta_2O_5/RUGGED SI CAPACITOR OF 23 μC/μm^2 APPLIED TO HIGH DENSITY DRAMS USING SUB-0.2μm PROCESS—Y. Ohji, S. Iijima, A. Saito, H. Miki, M. Kanai, M. Kunitiomo, S. Yamamoto, R. Furukawa, Y. Sugawara, T. Uemura, J. Kuroda, M. Nakata, T. Kisu, T. Kawagoe, K. Kawakita, M. Hasegawa, M. Nakamura, K. Kajigaya, M. Hidaka, H. Yamamoto, and I. Asano, Hitachi Ltd., Tokyo, Japan

The reliability of Ta_2O_5/rugged-silicon DRAM capacitor with 1.5 nm equivalent thickness was evaluated. The leakage current, initial defect density and TDDB data, as well as retention tests of a full-scale memory chip, show that the capacitor has sufficient quality for 256Mbit DRAM production.

1.3 A NEW PHYSICAL MODEL FOR NVM DATA-RETENTION TIME-TO-FAILURE—B. De Salvo, G. Ghibaudo, G. Pananakakis, LPCS/ENSERG, Grenoble, France, B. Guillaumot, ST Microelectronics, Grenoble, France, P. Candelier, and G. Reimbold, CEA/LETI, Grenoble, France

It is shown that the retention time for non-volatile memory cells is varying linearly with temperature T, rather than with the reciprocal temperature, as it is usually assumed, based on a classical Arrhenius model. The consequence of the T-model is a drastic reduction of the extrapolated time-to-failure in temperature accelerated lifetesting. The new T-model is supported by a thorough physical analysis.

1.4 USING ERASE SELF-DETRAPPED EFFECT TO ELIMINATE THE FLASH CELL PROGRAM/ERASE CYCLING VTH WINDOW CLOSE—J-H. Lee, K.R. Peng, J-R. Shih, B.K. Liew, and J.Y.C. Sun, TSMC, Taiwan ROC

Trapped electrons generated during programming of flash EPROM devices can cause program-erase window closure. An "erase self-de-trapped effect" has been found which will detrap the trapped electrons by applying a unique erase methodology. Using this effect, a new two step erasing scheme is proposed to reduce the flash EPROM cell program-erase Vth window closure.

1.5 INTERCONNECT AND MOS TRANSISTOR DEGRADATION AT HIGH CURRENT DENSITIES—A. Neugroschel, and C-T. Sah, Univ. of Florida, Gainesville, FL

A new mode of MOS transistor degradation is observed. High density of current typical of modern circuitry passing through metal line can release hydrogen atoms, which can then diffuse to the SiO_2/Si interface in the channel region and causes interface states generation by dangling bond depassivation. This mode of MOS transistor degradation may become the dominant reliability concern in the state-of-the-art and future Si integrated circuits.

1.6 THE INFLUENCE OF STUD BUMPING STRESS ON THE DEVICE DEGRADATION IN SCALED MOSFETS—N. Shimoyama, K. Machida, M. Shimaya, H. Koizuma, and H. Kyuragi, NTT System Electronic Labs, Kanagawa, Japan

Stud bumping above MOSFETs is shown to cause stress at the gate edges and results in reduced transconductance. The channel length dependence and 2D stress simulations indicate that the degradation mechanism is an increased interface trap density within 0.1 μm of the gate edge.

1.7 OFF-STATE STRESS-INDUCED REDUCTION OF OFF-STATE CURRENT IN POLYCRYSTALLINE SILICON THIN FILM TRANSISTORS—A.T. Krishnan and S.J. Fonash, Pennsylvania State Univ., University Park, PA

The off-state stress response of poly-Si TFTs was extensively studied using I-V and C-V measurements. About two orders of magnitude off-current reduction was observed after stress. Such off-current reduction is due to shielding states creation in n-channel TFTs and due to reduction of defects in p-channel TFTs.

Tuesday, March 23, 2:00 p.m., Parallel Session 2

DIELECTRICS I *(Session 2A, Town & Country Room)*

Co-Chairs: John S. Suehle, NIST and
Glenn Alers, Lucent Bell Labs

2A.1 A UNIFIED GATE OXIDE BREAKDOWN RELIABILITY MODEL—C. Hu and Q. Lu, UC Berkeley, Berkeley, CA

A gate oxide reliability model is presented to unify the E and 1/E models, T and E dependencies, intrinsic and defect breakdown lifetimes, and to relate fast screen and long-term operation reliability. Historical trend of decreasing gamma is explained. The safe operating field is projected and empirical refinement for <5nm oxide is presented.

2A.2 FIELD DEPENDENT CRITICAL TRAP DENSITY FOR THIN GATE OXIDE BREAKDOWN—K.P. Cheung, C.T. Liu, C-P. Chang, J.I. Colonell, W.Y-C Lai, R. Liu, J.F. Miner, C.S. Pai, H. Vaidya, and J.T. Clemens, Bell Labs, Murray Hill, NJ and E. Hasegawa, ULSI, Kanagawa, Japan

It is observed experimentally that the total number of trapped electrons just before breakdown increases rapidly with the stress field. Since the trap-filling factor is expected to be lower at higher fields, the trap density required for breakdown increases rapidly with field. An explanation is proposed.

2A.3 CHALLENGES FOR *ACCURATE* RELIABILITY PROJECTIONS IN THE ULTRA-THIN OXIDE REGIME—E. Wu and W. Abadeer, IBM, Essex Jct., VT, L.K. Han, G. Hueckel, and S.H. Lo, IBM, Hopewell Jct., NY

Several important aspects of oxide reliability and their impact on reliability projection, in particular, Weibull slopes determination and

area scaling are discussed For the first time, a rigorous analytical translation procedure is used to accurately determine Weibull slopes which are consistent with area scaling factor. The results indicate that reliability of ultra-thin oxides remains a serious concern.

2A.4 STUDY OF OXIDE BREAKDOWN UNDER VERY LOW ELECTRIC FIELD—A. Teramoto, H. Umeda, K. Azamawari, K. Kobayashi, K. Shiga, J. Komori, Y. Ohno, H. Miyoshi, Mitsubishi Electric Corp., Itami, Japan

TDDB measurement at temperatures lower than 125 °C in wide electric field range (7 - 13.5 MV/cm) are presented. The log(tBD) is shown to be not proportional to the electric field. The slope of log(tBD) versus E_{ox} plot increases with a decrease in oxide field.

2A.5 THE STATISTICAL DEPENDENCE OF OXIDE FAILURE RATES ON THE VDD AND TOX VARIATION, WITH APPLICATIONS FOR PROCESS DESIGN, CIRCUIT DESIGN, AND END USE—W.R. Hunter, Texas Instruments, Dallas, TX

The power of understanding the statistical dependence of oxide electric E, and average failure rate (AFR) on statistical variations of Vdd and tox is demonstrated. It leads to a mean oxide thickness for a technology which is 4Å thinner than a worst-case approach, while maintaining a required AFR. When applied to the quasi-static integral method for transient voltage overshoot reliability, it allows about 10 % higher voltages than the worst-case approach.

2A.6 INFLUENCE OF SOFT BREAKDOWN ON NMOSFET DEVICE CHARACTERISTICS—T. Pompl, Siemens, Muenchen, Germany, H. Wurzer, SIMEC, Dresden, Germany R.C. Wilkins, Univ. of Newcastle, Newcastle, UK, and M. Kerber, Siemens, Muenchen, Germany

The degradation of important transistor parameters related to soft breakdown and hard breakdown were studied. Long and short channel transistors were homogeneously stressed at elevated temperature until soft breakdown or hard breakdown occurred. The only noticeable signature of soft breakdown is an increase in off current due to enhanced gate induced drain leakage current. This effect arises if the soft breakdown is located within the gate-to-drain overlap region. Soft breakdown generates a spot or path of negative charges in the oxide and therefore enhances gate induced drain leakage currrent.

2A.7 CHARGE TRAPPING MECHANISM UNDER DYNAMIC STRESS AND ITS EFFECT ON FAILURE TIME—G. Ghidini, D. Brazzelli, C. Clementi, and F. Pellizzer, ST Microelectronics, Agrate Brianza, Italy

A comparison of dynamic versus DC stress applied to thin oxides is presented. Both lifetime and charge trapping results are explained by fast transient phenomenon experimentally observed using a measurement procedure capable of simulating the pulsed stress and detecting the evolution of charge trapping. A comparison of the charge trapping behavior in dry and stream oxides is presented.

2A.8 RE-CHALLENGE OF FLUORINE INCORPORATION INTO SIO_2 - SIGNIFICANT IMPROVEMENT OF CHARGE-TO-BREAKDOWN DISTRIBUTION-—Y. Mitani, H. Satake, Y. Nakasaki, A. Toriumi, Toshiba Corp., Yokohama, Japan

It is reported that Fluorine incorporation into SiO_2 can dramatically improve the Qbd distribution tail in the Weibull distribution function. It is inferred that the strain release and the restructuring of the SiO_2 by F incorporation are responsible for the Qbd Improvement as well as an increase in the oxide thickness.

COMPOUND SEMICONDUCTORS *(Session 2B, Presideo Room)*

Co-Chairs: Fausto Fantini, University of Modena and
Juin Liou, University of Central Floridaa

2B.1 RELIABILITY OF PASSIVATED 0.15 µm InAlAs/InGaAs HEMTS WITH PSEUDOMORPHIC CHANNEL—M. Dammann, M. Chertouk, W. Jantz, K. Kohler, K.H. Schmidt, and G. Weimann, Fraunhofer Institut fur Angewandte Festkorperphysik., Freiburg, Germany

Accelerated life test of 0.15 μm InAlAs/InGaAs HEMTs were performed under the DC electrical stress at four different temperatures in nitrogen. Using a 10% degradation of transconductance as failure criterion, we found an activation energy of 1.8 V and a projected life time of $5x10^6$ hours at 125 °C ambient temperature. The degradation was found to be much faster in air than in nitrogen.

2B.2 RELIABILITY EVALUATION OF MOCVD GROWN AlInAs/GaInAs/InP HEMTs—M. Nawaz, Chalmers Univ. of Technology, Goteborg, Sweden, W. Strupinski, Institute of Electronic Materials Technology, Warszawa, Poland, J. Stenarson, S.H.M Persson, and H. Zirath, Chalmers Univ. of Technology, Goteborg, Sweden

We report microwave performance and reliability evaluation of AlInAs/GaInAs/InP HEMTs with InP as a top surface layer grown by MOCVD. It is found that HEMTs with thin InP surface layer provide high threshold voltage uniformity and less thermal and bias stress degradation compared to conventional AlInAs/GaInAs/InP HEMTs. A cutoff frequency of 53 GHz and maximum frequency f_{max} of 210 GHz is obtained.

2B.3 BULK AND SURFACE EFFECTS OF HYDROGEN TREATMENT ON Al/Ti GATE POWER HFETs—R. Gaddi, Univ. of Modena, Modena, Italy, R. Menozzi, Univ. of Parma, Parma, Italy, A. Castaldini, Univ. of Bologna, Bologna, Italy, C. Lanzieri, Alenia System S.p.A., Rome, Italy, G. Meneghesso, Univ. of Padova, Padova, Italy, C. Canali, Univ. of Modena, Modena, Italy, and E. Zanoni, Univ. of Padova, Padova, Italy

We report novel results of unbiased Al/Ti-gate $Al_{0.25}$ $Ga_{0.75}$ As/GaAs power HFETs under 180 °C temperature and 5-15 % H_2/N_2 atmosphere. We observed both the bulk and surface degradation due to H_2 effects. It is also shown for the first time that hydrogenation can lead to large threshold voltage shift without changing significantly the gate barrier potential.

2B.4 THRESHOLD VOLTAGE SHIFT IN 0.1 μm SELF-ALIGNED-GATE GaAs MESFETs UNDER BIAS STRESS AND RELATED DEGRADATION OF ULTRA-HIGH-SPEED ICs—Y.K. Fukai, K. Yamasaki, K. Nishimura, NTT System Electronics Labs, Kanagawa, Japan

We have discovered a threshold voltage Vth shift in GaAs MESFET due to the high electric field near the gate edges. A 100 mV increase in Vth and a 20% reduction of f_{max} in ICs are found. A median life time above 10^6 hours at 100 °C can be obtained by incorporating $4x10^{13}$ cm^{-2} Si dose.

2B.5 FULL TWO-DIMENSIONAL ELECTROLUMINESCENT (EL) ANALYSIS OF GaAs/AlGaAs HBTs—M. Harris, B.Wagner, S. Halpern, M. Dobbs, Georgia Tech Research Institute, Atlanta, GA, C.Pagel, B. Stuffle, J. Henderson, and K. Johnson, Naval Surface Warfare Center, Crane, IN

The first full two-dimensional electroluminescent (EL) analysis of base-emitter junctions in heterojunction bipolar transistors (HBTs) is described. Correlation of the DC and RF characteristics with respect to the change in EL emission is presented. Rapid changes in the EL pattern occur at current densities of $1.5x10^4$ A/cm^2.

2B.6 A TDDB MODEL OF Si_3N_4 BASED CAPACITORS IN GaAs MMICs—J. Scarpulla, D.C. Eng, S.R. Olson, C-S. Wu, TRW, Redondo Beach, CA

It is possible to produce reliable GaAs MMICs which utilize low temperature PECVD silicon nitride as the dielectric in metal-insulator-metal capacitors (MIMCAPs). A TDDB model is described for these capacitors and is used to predict the reliability of product chips. The model is developed based upon breakdown measurements, ramped breakdown tests, and high temperature tests.

Tuesday March 23, 6:00 – 6:50 p.m., Atlas Ballroom Foyer
BUSES TO AQUARIUM

Tuesday March 23, 6:30 – 9:30 p.m.
SYMPOSIUM RECEPTION— STEPHEN BIRCH AQUARIUM

Wednesday, March 24, 8:15 a.m., Parallel Session 3

ESD & LATCH-UP

(Session 3A, Town & Country Room, in parallel with 3B–3C)
Co-Chairs: James W. Miller, Motorola and
Charvaka Duvvury, Texas Instruments, Inc.

3A.1 OCCURRENCE AND ELIMINATION OF ANOMALOUS TEMPERATURE DEPENDENCE OF LATCHUP TRIGGER CURRENTS IN BICMOS PROCESSES—E.R. Ooms and J.A. van der Pol, Philips Semiconductors, Nijmegen, The Netherlands

Latchup trigger currents in a BiCMOS process show an extreme temperature dependence (from > 100 mA to < 3 mA with $\Delta T = 1$ °C), severely affecting product latchup susceptibility. The effect is strongly process and wafer fab dependent and caused by lifting of the substrate potential primarily due to saturation of bipolar transistors causing hole injection and subsequent turn-on of parasitic n-type field transistors. It is shown that the effect can be eliminated by a combination of process and design measures.

3A.2 HIGH CURRENT PULSED CHARACTERIZATION OF DUAL-DAMASCENE COPPER INTERCONNECTS IN LOW- AND HIGH-K INTERLEVEL DIELECTRICS IN ADVANCED CMOS SEMICONDUCTOR TECHNOLOGIES—S. Voldman, R. Gauthier, K. Morrisseau, IBM, Essex Jct., VT, M. Hargrove, and V. McGahay, IBM, Hopewell Jct., NY

Characterization of copper-based interconnects in low-K hydro silsesque oxane (HSQ) and high-K SiO_2 interlevel dielectrics (ILD) is compared in the Joule heating regime ($J=10^7$ to 10^8 A/cm^2). Electrothermal extraction of critical current density (J_{crit}) of Cu-based/HSQ interconnects shows the ESD robustness decreases less than 15% (compared to Cu/SiO_2) but is superior to Al-based/SiO_2 interconnects.

3A.3 THE EFFECT OF SILICIDE ON ESD PERFORMANCE—G. Notermans, A. Heringa, M. van Dort, S. Jansen, and F. Kuper, Philips Semiconductor, Nijimegen, The Netherlands

A new model for localized breakdown in grounded-gate NMOSTs under ESD stress is developed which accounts for the reduced ESD strength in silicided devices. The model explains the impact of the stabilizing drain resistance on second breakdown current for both silicided as well as unsilicided drain diffusions.

3A.4 ANALYSIS OF SNAPBACK BEHAVIOR ON THE ESD CAPABILITY OF SUB-0.20 µm NMOS—A. Amerasekera, V. Gupta, and K. Vasanth, Texas Instruments, Dallas, TX

The self-biased lateral NPN operation under high current conditions is analyzed and the requirements to support a given injection current are determined. Three technologies with feature sizes of 0.13 µm, 0.18 µm, and 0.25 µm, are characterized experimentally and by simulation and the effects of process design and scaling on the lateral NPN behavior are shown.

3A.5 MODULAR APPROACH OF A HIGH CURRENT MOS COMPACT MODEL FOR ESD CIRCUIT-LEVEL SIMULATION INCLUDING TRANSIENT GATE COUPLING BEHAVIOR—M. Mergens, W. Wilkening, S. Mettler, Robert Bosch GmbH, Reutlingen, Germany, H. Wolf, Fraunhofer Institut Festkorpertechnologie IFT, Munich, Germany and W. Fichtner, Swiss Federal Institute of Technology, Zurich, Switzerland

A novel strategy for the highly flexible modeling of ESD-capable CMOS circuits is introduced. The high current MOS models comprise the important gate-coupling effect and an excellent approximated ava-

lanche generation formula crucial to obtain convergence. Measurement and simulation of an application example employing the new model exhibit the relevance of dynamic gate coupling on the ESD reliability of the circuit.

Wednesday, March 24, 8:15 a.m., Parallel Session 3

MICROELECTROMECHANICAL SYSTEMS

(Session 3B, Presideo Room)

Co-Chairs: William M. Miller, Sandia National Laboratories
Susanne Arney, Lucent Bell Labs

3B.1 PERFORMANCE AND RELIABILITY OF A NEW MEMS ELECTROSTATIC LATERAL OUTPUT MOTOR—S.T. Patton, W.D. Cowan, and J.S. Zabinski, Air Force Research Lab, Wright-Patterson AFB, OH

This study investigates the effect of relative humidity on the performance, reliability, and failure mechanisms of a new type of MEMS electrostatic motor. Observations at high relative humidity include the formation of water menisci and increased adhesion forces. In durability tests, changes in system forces occurred as motor cycles increased.

3B.2 THE EFFECT OF HUMIDITY ON THE RELIABILITY OF A SURFACE MICROMACHINED MICROENGINE—D.M. Tanner, K.A. Peterson, L.W. Irwin, N.F. Smith, W.P. Eaton, W.M. Miller, and S.L. Miller, Sandia National Labs, Albuquerque, NM

Humidity is shown to be a strong factor in the wear of rubbing surfaces in polysilicon micromachines. We describe a completely unexpected result, that low humidity can lead to very high wear without a significant change in reliability. We will explain this potentially counterintuitive result.

3B.3 LASER POWER MONITORING USING MOEMS MICROMIRROR TECHNOLOGY—A. Agarwal, S. Arney, B. Barber, S. Kosinski, J. LeGrange, R. Raju, and R. Ruel, Lucent Technologies, Bell Labs, Murray Hill, NJ

We have fabricated fiberized MEMS *in situ* power monitor chips in which an out-of-plane micromirror partially deflects the incident multimode light to an on-chip fiber tap. This first prototype shows stability to hundreds of milliwatts.

3B.4 RELIABILITY METHODOLOGY FOR PREDICTION OF MICROMACHINED ACCELEROMETER STICTION—A. Hartzell and D. Woodilla, Analog Devices Inc., Cambridge, MA

This study reports on an empirically-generated stiction field predictive methodology for accelerometers prone to stiction failure. A probability distribution function was generated as a function of shock level. Although the population studied was stiction prone, the failure mode is probabilistic and overall, the parts have a high survival rate.

INTERCONNECTS I

(Session 3C, Presideo Room, following 3B)

Chair: J. Joseph Clement, Sandia National Laboratories

3C.1 THE RELATIONSHIP BETWEEN RESISTANCE CHANGES AND VOID VOLUME CHANGES IN PASSIVATED Al INTERCONNECTS—J. Doan, J. Bravman, P. Flinn, Stanford Univ., Stanford, CA and T. Marieb, Intel Corp., Santa Clara, CA

Passivated Al lines were electromigration tested using an *in situ* technique that continuously imaged an entire 300 μm long structure. The resistance data were compared with void volume data. Solely from the resistance data, the nucleation time of the first void can usually be found, but the void volume cannot be estimated.

3C.2 A NOVEL FAST TECHNIQUE FOR DETECTING VOIDING DAMAGE IN IC INTERCONNECTS—S. Foley, L. Floyd, and A. Mathewson, NMRC, University College, Cork, Ireland

A novel high frequency technique has been developed that is sensitive to voiding damage induced in an interconnect line by stress migration or electromigration. A high frequency (GHz) signal is applied to a microstrip-like test structure, and measurements of the scattering parameters allow the detection of the amount of voiding damage.

3C.3 SIGNIFICANT IMPROVEMENT IN ELECTROMIGRATION OF REFLOW-SPUTTERED Al-0.5wt% Cu/Nb-LINER DUAL DAMASCENE INTERCONNECTS WITH LOW-k ORGANIC SOG DIELECTRIC—T. Usui, T.Watanabe, S. Ito, M. Hasunuma, M. Kawai, and H. Kaneko, Toshiba Corp., Yokohama, Japan

Reflow-sputtered Al-0.5wt%Cu/Nb-liner dual damascene interconnects with a monolithic Al via and a low-k organic SOG passivation were fabricated and electromigration tested. A significant improvement in the MTF was observed when the SOG was compared to a standard TEOS passivation. This is achieved by the suppression of the stress evolution in the Al interconnect around the via due to the low Young's modulus of the SOG dielectric.

3C.4 THE APPARENT ACTIVATION ENERGY AND CURRENT DENSITY EXPONENT OF ELECTROMIGRATION DAMAGE IN CHIP-LEVEL INTERCONNECT LINES: A GRAIN-STRUCTURE-BASED STATISTICAL APPROACH—M.A. Korhonen, T.M. Korhonen, Cornell University, Ithaca, NY, D.D. Brown, AMD, Sunnyvale, CA, and C.-Y. Li, Cornell University, Ithaca, NY

Although current density exponents and activation energies are well known for elemental processes, there is no consensus on which values should be used in reliability estimates for realistic lines comprising both bamboo and polycrystalline sections. In this contribution a Monte-Carlo approach was used to generate realistic lines, and their electromigration lifetimes were simulated. Stress evolution along a line was simulated, letting voids nucleate where stress exceeded a critical level and then grow until the largest reached a specified critical size. Repeating this process for various current densities and temperatures gave the apparent activation energies and current density exponents.

Wednesday, March 24, 2:00 p.m., Parallel Session 4

HOT CARRIERS *(Session 4A, San Diego Room)*

Co-Chairs: Matt Wordeman, IBM Microelectronics and Roland Thewes, Siemens AG

4A.1 (ESREF best paper invited) PRECISE QUANTATIVE EVALUATION OF THE HOT-CARRIER INDUCED DRAIN SERIES RESISTANCE DEGRADATION IN LATID-N-MOSFETs—G.H. Walter, W. Weber, R. Benderlow, R. Jurk, C.G. Linnenbank, C. Schlunder, Siemens, Munich, Germany, D. Schmitt-Landsiedel, Technical Univ. of Munich, Germany and R. Thewes, Siemens, Munich, Germany

A method is described that distinguishes the drain series resistance increase from other mechanisms contributing to drain current degradation of hot-carrier stressed n-MOSFETs. For short stress times, the drain current degradation is dominated by series resistance changes. For long stresses, an equivalent channel length increase prevails.

4A.2 CHANNEL LENGTH DEPENDENCE OF HOT-CARRIER DEGRADATION OF LATID N-MOSFETS UNDER ANALOG OPERATION—R. Thewes, G.H. Walter, R. Brederlow, C. Schlunder, A.v. Schwerin, R. Jurk, C.G. Linnenbank, G. Lengauer, D. Schmitt-Landsiedel*, and W. Weber, Siemens, Munich, Germany *Technical Univ. of Munich, Munich, Germany

Applying stress techniques related to the operating conditions of analog CMOS applications, damage proportional to (channel length)$^{-1}$ is found. The resulting drain current degradation is proportional to (channel length)$^{-(s+1)}$, with S+1=2 in linear and S+1>2 in saturation mode. The

physical insight achieved yields important information for analog CMOS reliability.

4A.3 HOT CARRIER DEGRADATION OF THE LOW FREQUENCY NOISE OF MOS TRANSISTORS UNDER ANALOG OPERATING CONDITIONS—R. Brederlow, W. Weber, Siemens, Munich, Germany, D. Schmitt-Landsiedel, Technical Univ. of Munich, and R. Thewes, Siemens, Munich, Germany

An investigation of the 1/f-noise behavior of n- and p-MOS transistors under typical analog operating conditions is performed. It is shown that the noise magnitude in saturation mode significantly increases after hot-carrier degradation. In low noise circuits this increase can become a major reliability issue. The mechanisms responsible for this kind of degradation and the resulting analog circuit design considerations are discussed.

4A.4 A UNIFIED COMPACT SCALABLE ΔId MODEL FOR HOT-CARRIER RELIABILITY SIMULATION—P. Chen, L. Wu, G. Zhang, and Z. Liu, BTA Technology, Inc., Santa Clara, CA

A unified compact scalable ΔId model for hot-carrier induced reliability simulation has been developed. For the first time, it unifies the sub-threshold, linear and saturation regions. The model has been verified against a 0.25 μm technology (Tox=50Å) in both forward and reverse operation modes with good scalability.

4A.5 AN ACCURATE HOT-CARRIER RELIABILITY MONITOR FOR DEEP-SUBMICRON SHALLOW S/D JUNCTION THIN GATE OXIDE N-MOSFETS—S.S. Chung, S.J. Chen, C.M. Yih, W.J. Yang, National Chiao Tung Univ., and T.S. Chao, National Nano Device Lab, Taiwan R.O.C.

A new monitor for hot-carrier reliability evaluation has been developed using total values of Nit in the effective channel length region. A degradation model has also been developed based on the Nit distribution and mobility scattering effect. This approach has been successfully applied to gate-engineering studies.

4A.6 HOT-CARRIER EFFECTS IN NMOSFETS IN 0.1μm CMOS TECHNOLOGY—E. Li, E. Rosenbaum, Univ. of Illinois at Urbana-Champaign, Urbana, IL, J.Tao, AMD, Sunnyvale, CA, G. Yeap, Motorola, Austin, TX, M.-R. Lin, and P. Fang, AMD, Sunnyvale, CA

This paper demonstrates that the worst case hot-carrier stress condition is determined by the ratio of Ib/Id at Ib,peak to Ib/Id at Vg=Vd. At the operating voltage, for 0.1 μm technology, the worst case stress condition is Ib,peak. PMA in deuterium is equally effective for improving lifetime under bias at Ib,peak and Vg = Vd.

4A.7 DEGRADATION OF HOT-CARRIER LIFETIME FOR NARROW WIDTH MOSFETS WITH SHALLOW TRENCH ISOLATION—W. Lee, Kwangju Institute of Science and Technology, Kwangju, Korea, S. Lee, T. Ahn, LG Semicon Co., Cheongju, Korea, and H. Hwang, Kwangju Institute of Science and Technology, Kwangju, Korea

Under maximum substrate current stress, the lifetime of shallow trench isolated transistors is not sensitive to channel width. However, a significant degradation of device lifetime was observed under maximum gate current condition (Vg=Vd) in narrow devices. This mechanism may have a significant effect in narrow-width transfer gates used in DRAM pass transistor circuits.

INTERCONNECT II *(Session 4B, Town & Country Room)*

Chair: William Filter, Sandia National Laboratories

4B.1 MICROSTRUCTURE AND ELECTROMIGRATION IN COPPER DAMASCENE LINES—L. Arnaud, G. Tartavel, LETI CEA-G, Grenoble, France, T. Berger, SGS Thomson Microelectronics, Crolles, France, D. Mariolle, and Y.Gobil, LETI CEA-G, Grenoble, France

The microstructure of damascene Cu interconnects was analyzed versus linewidth by FIB imaging. Pure bamboo lines were not obtained because grain size decreased with line width. Electromigration results for wide-line (3 μm) polygrain and narrow-line (0.5 μm) quasi-bamboo structures gave the same activation energy, E_a = 0.65 eV, in CVD Cu. These results are consistent with copper diffusion along grain boundaries and a slow surface diffusion. In contrast, PVD Cu showed a better activation energy, E_a = 1.1 eV.

4B.2 SURFACE ELECTROMIGRATION IN COPPER INTERCONNECTS—N.D. McCusker and H.S. Gamble, The Queen's Univ. of Belfast, Belfast, Northern Ireland

This work describes the important role of surface migration in small-grained, sputtered copper interconnects. Electromigration test structures were patterned from RF magnetron-sputtered copper films using standard photolithography and then stressed. The microstructure of the films was extensively characterized and the void sites in the test structures studied by optical, scanning electron, and atomic force microscopy. We show that it is important to understand the failure process fully in the context of the line microstructure when comparing copper to aluminum.

4B.3 THE LEAKAGE-CURRENT DEGRADATION OF Cu/BCB SINGLE DAMASCENE UNDER THERMAL AND BIAS-TEMPERATURE STRESS—S.U. Kim, SEMATECH, T. Cho, and P.S. Ho, Univ. of Texas, Austin, TX

The leakage-current degradation of a Cu/benzocyclobutene (BCB) test structure under thermal and bias-temperature stresses was investigated. A transition temperature was observed, above which leakage-current failure occurs under thermal stress. Cu/BCB also failed rapidly under bias-temperature stress. Failure analysis indicates that surface leakage is responsible for this failure. A model for bias-temperature stress degradation is proposed, in which Cu ions are injected into the dielectric through localized surface defects in the metallization.

4B.4 THERMAL STRESSES IN L- AND T- SHAPED METAL INTERCONNECTS: A THREE-DIMENSIONAL ANALYSIS—Y.-L. Shen, Univ. of New Mexico, Albuquerque, NM

Numerical analyses of thermal stresses in L- and T-shaped aluminum interconnects were carried out using three-dimensional finite element modeling. The stress distributions in unpassivated and passivated lines with different aspect ratios were quantified. Implications for the design of test interconnect structures for spatially-resolved stress measurements and related reliability issues are discussed.

4B.5 THE USE OF A WLR TECHNIQUE TO CHARACTERIZE STRESS-INDUCED VOIDING IN 0.25 AND 0.18 MICRON TECHNOLOGIES FOR INTEGRATED CIRCUITS—A. Marathe, P. Besser, J. Tsiang, V. Pham, and P. Fang, AMD, Sunnyvale, CA

An accelerated wafer-level reliability test has been used to characterize stress-induced voiding in sub-micron interconnect structures used in advanced multilayer integrated circuits. A quantitative correlation between isothermal wafer-level test results and severity of voiding has been demonstrated. The $T_{50\%}$ and $T_{0.1\%}$ of the lognormal distribution of failures in the test decrease, while the lognormal sigma increases as the voiding becomes more severe. The wafer-level test has been successfully demonstrated as a reliability tool for process monitoring and characterization.

4B.6 INVESTIGATION OF SELF-HEATING PHENOMENON IN SMALL-GEOMETRY VIAS USING SCANNING JOULE EXPANSION MICROSCOPY—K. Banerjee, G. Wu, M. Igeta, UC Berkeley, Berkeley, CA, A. Amerasekera, Texas Instruments, Dallas, TX, A. Majumdar, and C. Hu, UC Berkeley, Berkeley, CA

A novel thermometry technique, scanning Joule expansion microscopy (SJEM), has been used to study the steady-state and dynamic thermal

behavior of small-geometry vias under sinusoidal and pulsed-current stresses. The spatial distribution of temperature rise in a sub-micron via is measured directly, and the thermal time constant of the via is determined from the AC frequency dependence of the temperature rise. Furthermore, the average and peak temperature rises under pulsed stress have been estimated from the first-harmonic temperature rise.

4B.7 THERMO-MECHANICAL STRESS-INDUCED VOIDING IN A TUNGSTEN-AlCu INTERCONNECT SYSTEM—B. Wallace, Y.-H. Lee, D. Pantuso, K. Wu, and N. Mielke, Intel Corp., Santa Clara, CA

Thermal-mechanical stress-induced metal voiding has been characterized in tungsten-plug via chains with short metal links. An AC current stress thermally cycles the W-AlCu interface, resulting in large mechanical stress gradients. These stress gradients, coupled with localized interface aberrations, are responsible for void nucleation, formation, and growth. Using a cleaner ILD/metal etch process increases the time to failure due to this voiding mechanism.

Wednesday, March 24, 7:00 – 8:00 p.m., Atlas Ballroom Foyer
BANQUET RECEPTION

Wednesday, March 24, 8:00 p.m., Atlas Ballroom
AWARDS BANQUET

Thursday, March 25, 8:15 a.m., Parallel Session 5

FAILURE ANALYSIS (Session 5A, Town & Country Room)
Co-Chairs: Dan Barton, Sandia National Laboratories
and Steven J. Kirch, Intel Corporation

5A.1 TWO-DIMENSIONAL CARRIER PROFILING OF 0.4 μm DEVICES USING SCANNING SCHOTTKY CAPACITANCE MICROSCOPY—D.J. Thomson, J.N. Nxumalo, Y. Li, and T. Tran, Univ. of Manitoba, Manitoba, Canada

We present a technique for measuring carrier profiles in semiconductor device cross-sections using the Schottky capacitance between a conductive probe and a semiconductor surface. The capacitance versus voltage can be related to the carrier concentration. We have used this technique to image the carriers in a 0.4 micron scale p-MOSFET.

5A.2 THRESHOLD VOLTAGE SHIFT CAUSED BY COPPER CONTAMINATION—B. Vermeire, C.A. Pederson, H.G. Parks, and D. Sarid, Univ. of Arizona, Tucson, AZ

A novel approach was used to investigate the effect of trace amounts of process-induced copper contamination on thin oxides. Highly localized field emission mapping reveals small bumps on top of the SiO_2 surface not detectable by conventional means. These bumps cause intolerable threshold voltage shifts upon transistor scaling to 0.13 μm and beyond.

5A.3 FAULT MODEL FOR VLSI CIRCUITS RELIABILITY ASSESSMENT—B. Lisenker and Y. Mitnick, Intel Israel, Haifa, Israel

This paper introduces a fault model for reliability estimation of VLSI circuits. The model is based on the general Percolation Theory applied to the sub-micron CMOS technology. New segregation methodologies are presented and experimentally verified in reliability stresses.

5A.4 LASER MICRO-MACHINING OF SILICON AND DEPOSITION OF CONDUCTOR LINES FOR DESIGN DEBUG OF C4 PACKAGED ICS—R.R. Goruganthu, M. Bruce, J. Birdsley, V. Bruce, and G. Gilfeather, AMD, Austin, TX

The authors describe a method for localized thinning of silicon at very high etch rates using a laser based process. A novel technique was implemented for determining endpoint for this backside thinning process. Controlled silicon thinning is successfully demonstrated. We also describe a process for deposition of long metal lines that can work in tandem with methods using focused ion beams for circuit edits.

5A.5 FAILURES INDUCED ON BIPOLAR OPERATIONAL AMPLIFIERS FROM ELECTROMAGNETIC INTERFERENCE CONDUCTED ON THE POWER SUPPLAY RAILS—N. Specialo and G. Setti, Univ. of Bologna, Bologna, Italy

In this work we will study the effects of electromagnetic interference conveyed to the supply rails of integrated bipolar operational amplifiers. In particular, with reference to the well known mA741 topology, we will show that amplifiers undergo very strong failures when subjected to EMI conveyed to the negative supply, while they are only moderately sensitive to interference conveyed to the positive supply. Finally, on the basis of detailed circuit analysis and simulations, we will demonstrate the physical origin of such failures.

PACKAGING AND ASSEMBLY

(Session 5B, Town & Country Room, following 5A)

Co-Chairs: Thomas M. Moore, Texas Instruments and S. Sidharth, AMD

5B.1 BACKSIDE PROBING OF FLIP-CHIP CIRCUITS USING ELECTROSTATIC FORCE SAMPLING—R.Qi, D.J. Thomson, and G.E. Bridges, Micron Force Instruments Inc., San Jose, CA

A non-contact voltage probing technique for flip chips is presented. Signals in the device layer are accessed by Focused Ion Beam milling through the backside. Local electrostatic forces are sensed by a small micromachined probe held in close proximity to the circuit measurement point. The instrument has a 3GHz bandwidth and a capacitive loading on the test point of less than 1fF.

5B.2 FILLER INDUCED METAL CRUSH FAILURE MECHANISM IN PLASTIC ENCAPSULATED DEVICES—P. Yalamanchili and V. Baltazar, Analog Devices Inc., Santa Clara, CA

Mold compound filler can produce local stresses at the die surface sufficient to crack the passivation and result in metal-to-polysilicon or metal-to-metal shorts (metal crush). Metal crush takes place only in plastic encapsulated devices and is predominant in plastic packages with silicone die overcoat. The use of ultra-low stress mold compound without die overcoat eliminates metal crush and results in high electrical test yield.

5B.3 DESIGN OPTIMIZATION OF RF ANTENNA BGA INTERCONNECT STRUCTURES USING TEST VALIDATED PHYSICS OF FAILURE METHODS—D.A. Pietila and M. Rassaian, Boeing, Seattle, WA

A concurrent reliability and design optimization study is presented on a BGA interconnect between a ceramic-packages RF device and a plastic encapsulated phased array antenna element for the reception of direct broadcast television on commercial jet liners. A plastic-strain damage model based on a modified Coffin-Manson fatigue criterion was selected to represent the dominant failure mechanism of low cycle solder fatigue of the BGA interconnects.

PLASMA INDUCED DAMAGE

(Session 5C, Town & Country Room, in parallel with 5A–5B)

Co-Chairs: James McVittie, Stanford University and Srikanth Krishnan, Texas Instruments

5C.1 U-V BLOCKING TECHNOLOGY TO REDUCE PLASMA-INDUCED TRANSISTOR DAMAGE—S. Shuto, I. Kunishima, and S. Tanaka, Toshiba Corp., Kawasaki, Japan

The effect of plasma-UV on plasma damage during backend fabrication is studied using UV-blocking protective layers. Results show damage can be reduced by using a P-SiON or P-SiN protection layer which absorbs UV-light. The degradation is modeled as a plasma-induced gate stress in conjunction with the UV-photon induced electron excitation.

5C.2 NEW EXPERIMENTAL FINDINGS ON PROCESS-INDUCED HOT-CARRIER DEGRADATION OF DEEP-SUBMICRON N-MOSFETS—D.Y.C. Lie, J. Yota, W. Xia, A.B. Joshi, R.A. Williams, R. Zwingman, L. Chung, Rockwell Semiconductor Systems, Newport Beach, CA, and D.L. Kwong, Univ. of Texas, Austin, TX

The impact of plasma damage during backend processing (M1-M4) on channel-Hot carrier reliability is studied. With a SiN layer as a Pre-Metal Dielectric (PMD), results show that CHC lifetime reduction from subsequent high density plasma (HDP) deposition damage is reduced. A mechanism is proposed explaining the improvement in device reliability with the SiN dielectric layer.

5C.3 A MODEL FOR CHANNEL HOT CARRIER RELIABILITY DEGRADATION DUE TO PLASMA DAMAGE IN MOS DEVICES—S. Rangan, Pennsylvania State Univ., University Park, PA, S. Krishnan, A. Amerasekara, S. Aur, Texas Instruments, Dallas, TX, and S. Ashok, Pennsylvania State Univ., University Park, PA

The impact of process-induced damage on CHC lifetime has been studied. An empirical model is developed to establish the trade-off between antenna ratio and CHC lifetime degradation due to plasma damage. The model delineates the contribution of device-dependent and process-dependent parameters to the overall device lifetime.

5C.4 A NEW EXPERIMENTAL APPROACH TO EVALUATE PLASMA DAMAGE IN NMOS AND PMOS DEVICES—L. Pantisano, A. Paccagnella, M. Barbazza, A. Scarpa, Univ. of Padova, Padova, Italy, and M.G. Valentini, ST Microelectronics, Agrate Brianza, Italy

Latent plasma damage in gate oxides is evaluated through a new experimental technique. The oxide charge trapping kinetics is studied during electrical stress, permitting the separation of latent plasma damage from measurement introduced damage. The extracted plasma damage and its distribution map is presented.

Thursday, March 25, 2:00 p.m., Session 6, Town & Country Room

DIELECTRICS II

Co-Chairs: Bonnie Weir, Lucent Bell Labs and
Elyse Rosenbaum, University of Illinois

6.1 A FAST AND SIMPLE METHODOLOGY TO PREDICT DIELECTRIC BREAKDOWN—T. Nigam, R. Degraeve, G. Groeseneken, M. Heyns, and H. Maes, IMEC, Leuven, Belgium

A simple and time-efficient methodology to predict breakdown in ultra-thin oxides at low voltages is presented. The new method is based on measuring Stress Induced Leakage Current (SILC) generation during stress without interruption. It is demonstrated that oxide lifetime correlates better with Vgate.

6.2 TRAP-ASSISTED TUNNELING CURRENT THROUGH ULTRA-THIN OXIDE—J. Wu, L.F. Register, and E. Rosenbaum, Univ. of Illinois at Urbana-Champaign, Urbana, IL

Based only on a consideration of tunneling probabilities, this work explains why stess induced leakage current is observed only within a "window" of oxide thickness, ~3-8 nm. This work also provides further experimental evidence thaat SILC is due to inelastic trap-assisted tunneling of electrons from the cathode conduction band.

6.3 A MODEL OF THE STRESS TIME DEPENDENCE OF SILC—Q. Lu, UC Berkeley, Berkeley, CA, K.P. Cheung, N.A. Ciampa, C.T. Liu, C-P. Chang, J.I. Colonell, W-Y-C. Lai, R. Liu, J.F. Miner, H. Vaidya, C-S. Pai, and J.T. Clemens, Bell Labs, Lucent Technologies, Murray Hill, NJ

The stress time dependence of SILC is studied in detail and the saturation behavior is reported. A physical model based on the depletion of trap

generation precursor sites is presented. The model fits well to a variety of data and is further supported by annealing experiments."

6.4 LOW VOLTAGE STRESS-INDUCED-LEAKAGE-CURRENT IN ULTRATHIN GATE OXIDES—P. Nicollian, M. Rodder, D.T. Grider, P. Chen, R.M. Wallace, and S.V. Hattengady, Texas Instruments, Inc.

It is shown that for oxides less than 3.5nm thick, interfacial traps generated during direct tunneling stress result in a measured voltage dependent SILC phenomenon that can dominate the gate leakage current under low voltage operating conditions. Thin mechanism is an important consideration in sub-1.2 V technologies.

6.5 A COMPARATIVE STUDY OF SILC TRANSIENT CHARACTERISTICS AND MECHANISMS IN FN STRESSED AND HOT HOLE STRESSED TUNNEL OXIDES—N-K. Zous, T. Wang, C.C. Yeh, C.W. Tsai, National Chiao-Tung Univ. and C. Huang, Macronix Co.,Taiwan, ROC

Mechanisms and transient characteristics of hot hole (HH) stress and FN stress induced leakage currents in tunnel oxides are investigated. The HH SILC is found to have a more pronounced transient effect. The transient is attributed to positive oxide charge detrapping and thus annihilation of positive charge-assisted tunneling (PCAT) centers. The PCAT current can be significantly reduced by using an electron neutralization technique.

6.6 ATOMICALLY SMOOTH ULTRA-THIN OXIDE IMPROVED SOFT BREAKDOWN AND SILC—A. Chin, B.C. Lin, National Chiao-Tung University, W.J. Chen, National Yun-Lin Polytechnic Inst., Y.H. Wang and C.Tsai, National Chiao-Tung University, Taiwan, ROC

Soft-breakdown and intrinsic defect-induced leakage currents limit the integrity of ultra-thin oxide. It is reported that the stress-induced leakage current and soft-breakdown are process-dependent and can be largely improved by using an *in-situ* desorbing native oxide with an atomically smooth surface.

6.7 J-RAMP ON SUB-3nm DIELECTRICS: NOISE AS A BREAKDOWN CRITERIA—G.B. Alers, B.E. Weir, M.R. Frei, and D. Monroe, Bell Labs, Lucent Technologies, Murray Hill, NJ

The statistics and the implementation of a noise breakdown test for breakdown in ultra-thin oxides is presented. The addition of noise as a criterion for breakdown makes the determination of the breakdown event much easier even when the change of voltage during the test diminishes to the point that it is not detectable.

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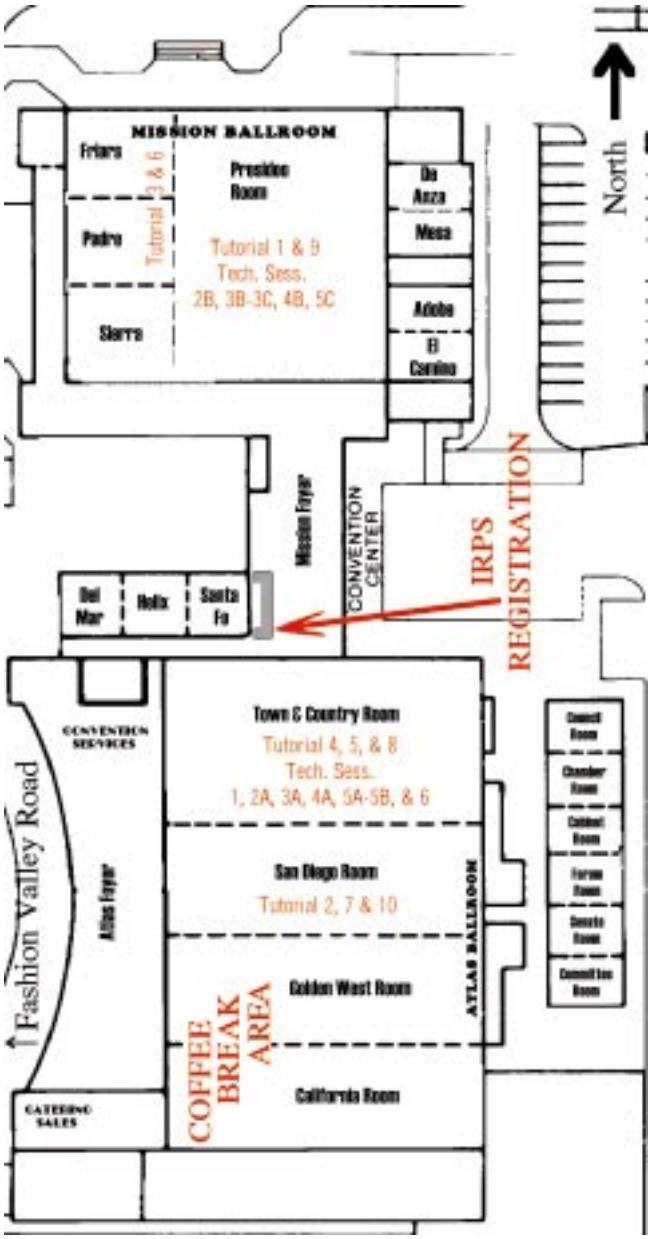
Event/Location/Time Table

Time	Event	Room
Sunday		
4:00 p.m.-9:00 p.m.	Symposium Registration	Mission Foyer
7:00 p.m.-9:00 p.m.	Companions' Prog. Reg.	Mission Foyer
Monday		
7:00 a.m.	Tutorials' Coffee/Danish	GoldenWest/California
7:00 a.m.-6:00 p.m.	Info Tables/Demo Sign Ups	GoldenWest/California
7:00 a.m.-8:00 p.m.	Symposium Registration	Mission Foyer
8:00-11:30 a.m.	Tutorials 1	Presideo
8:00-11:30 a.m.	Tutorials 2	San Diego
8:00-11:30 a.m.	Tutorials 3	Friars/Padre
8:00-9:30 a.m.	Tutorials 4	Town & Country
10:00-11:30 a.m.	Tutorials 5	Town & Country
12:00-5:00 p.m.	Equip. Demonstrations	Exhibition Hall
1:30-5:00 p.m.	Tutorials 6	Friars/Padre
1:30-3:00 p.m.	Tutorials 7	San Diego
1:30-5:00 p.m.	Tutorials 8	Town & Country
1:30-5:00 p.m.	Tutorials 9	Presideo
3:30-5:00 p.m.	Tutorials 10	San Diego
6:00 p.m.-8:00 p.m.	Companions' Prog. Reg.	Mission Foyer
3:30-5:30 p.m.	Workshop #11	To be posted on-site
7:30 p.m.-9:30 p.m.	Workshops #1 to 10	To be posted on-site
Tuesday		
7:00 a.m.	Coffee/Danish	GoldenWest/California
7:00 a.m.-5:30 p.m.	Info Tables/Demo Sign Ups	GoldenWest/California
7:15 a.m.-3:00 p.m.	Symposium Registration	Mission Foyer
7:30 a.m.-5:00 p.m.	Equip. Demonstrations	Exhibition Hall
8:15-noon	Opening/Keynote/Tech. Sess. 1	Town & Country
9:55-10:20 a.m.	Coffee Break	GoldenWest/California
2:00-5:45 p.m.	Technical Session 2A	Town & Country
2:00-4:55 p.m.	Technical Session 2B	Presideo Room
3:15-3:40 p.m.	Coffee Break	GoldenWest/California
6:30 p.m.-9:45 p.m.	Symposium Reception	Stephen Birch Aquarium*
	*(Buses at convention center—starting 6:00 p.m.)	
Wednesday		
7:00 a.m.	Coffee/Danish	GoldenWest/California
7:00 a.m.-5:30 p.m.	Info Tables/Demo Sign Ups	GoldenWest/California
8:00 a.m.-3:00 p.m.	Symposium Registration	Mission Foyer
7:30 a.m.-5:00 p.m.	Equip. Demonstrations	Exhibition Hall
8:15-10:45 a.m.	Technical Session 3A	Town & Country
8:15-noon a.m.	Technical Session 3B–3C	Presideo
9:55-10:20 a.m.	Coffee Break	GoldenWest/California
2:00-5:20 p.m.	Technical Session 4A	Town & Country
2:00-5:20 p.m.	Technical Session 4B	Presideo
3:15-3:40 p.m.	Coffee Break	GoldenWest/California
7:00 p.m.-8:00 p.m.	Awards Banquet Reception	Atlas Foyer
8:00 p.m.	Awards Banquet	Town & Country/San Diego
Thursday		
7:00 a.m.	Coffee/Danish	GoldenWest/California
7:00 a.m.-noon	Info Tables/Demo Sign Ups	GoldenWest/California
8:00 a.m.-2:00 p.m.	Symposium Registration	Mission Foyer
7:30 a.m.-noon	Equip. Demonstrations	Exhibition Hall
8:15-noon	Technical Session 5A-5B	Town & Country
8:15-9:55 a.m.	Technical Session 5C	Presideo
9:55-10:20 a.m.	Coffee Break	GoldenWest/California
2:00-5:20 p.m.	Technical Session 6	Town & Country
3:15-3:40 p.m.	Coffee Break	GoldenWest/California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Friars
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Slarr's
Presidio Room
Tutorial 1 & 9
Tech. Sess.
2B, 3B-3C, 4B, 5C
Da Anza
Mesa
Adobe
El Camino
North
Mission Foyer
CONVENTION CENTER
IRPS REGISTRATION
Del Mar
Bella
Santa Fe
CONVENTION SERVICES
Fashion Valley Road
Atlas Foyer
Town & Country Room
Tutorial 4, 5, & 8
Tech. Sess.
1, 2A, 3A, 4A, 5A-5B, & 6
San Diego Room
Tutorial 2, 7 & 10
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