9.2A, 100V, 0.270 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA09594.

**Features**
- 9.2A, 100V
- $r_{DS(ON)} = 0.270 \Omega$
- SOA is Power Dissipation Limited
- Single Pulse Avalanche Energy Rated
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

**Symbol**

```
\( \begin{array}{c}
\text{G} \\
\text{D} \\
\text{S} \\
\end{array} \)
```

**Packaging**

JEDEC TO-220AB

```
\( \begin{array}{c}
\text{SOURCE} \\
\text{DRAIN} \\
\text{GATE} \\
\text{DRAIN (FLANGE)} \\
\end{array} \)
```
Absolute Maximum Ratings  \( T_C = 25^\circ\text{C}, \text{Unless Otherwise Specified} \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain to Source Breakdown Voltage (Note 1)</td>
<td>( V_{DSS} )</td>
<td>( I_D = 250\mu\text{A}, V_{GS} = 0\text{V} ) (Figure 10)</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Gate to Threshold Voltage</td>
<td>( V_{GS(TH)} )</td>
<td>( V_{GS} = V_{DSS}, I_D = 250\mu\text{A} )</td>
<td>2.0</td>
<td>-</td>
<td>4.0</td>
<td>V</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>( I_{DSS} )</td>
<td>( V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0\text{V} )</td>
<td>-</td>
<td>-</td>
<td>250</td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>( I_{DSS} )</td>
<td>( V_{DS} = 0.8 \times \text{Rated } V_{DSS}, V_{GS} = 0\text{V}, T_J = 150^\circ\text{C} )</td>
<td>-</td>
<td>-</td>
<td>1000</td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>On-State Drain Current (Note 2)</td>
<td>( I_{D(ON)} )</td>
<td>( V_{DS} &gt; I_{D(ON)} \times I_{DS} \times \text{OnMax}, V_{GS} = 10\text{V} ) (Figure 7)</td>
<td>9.2</td>
<td>-</td>
<td>-</td>
<td>A</td>
</tr>
<tr>
<td>Gate to Source Leakage Current</td>
<td>( I_{GSS} )</td>
<td>( V_{GS} = \pm 20\text{V} )</td>
<td>-</td>
<td>-</td>
<td>±100</td>
<td>( \text{nA} )</td>
</tr>
<tr>
<td>Drain to Source On Resistance (Note 2)</td>
<td>( I_{DS(ON)} )</td>
<td>( I_D = 5.6\text{A}, V_{GS} = 10\text{V} ) (Figure 8, 9)</td>
<td>-</td>
<td>0.25</td>
<td>0.27</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Forward Transconductance (Note 2)</td>
<td>( g_{fs} )</td>
<td>( V_{DS} \geq 50\text{V}, I_D = 5.6\text{A} ) (Figure 12)</td>
<td>2.7</td>
<td>4.1</td>
<td>-</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Turn-On Delay Time</td>
<td>( t_d(ON) )</td>
<td>( V_{DD} \geq 50\text{V}, I_D \approx 9.2\text{A}, R_G = 18\Omega, R_L = 5.5\Omega )</td>
<td>-</td>
<td>9</td>
<td>13</td>
<td>ns</td>
</tr>
<tr>
<td>Rise Time</td>
<td>( t_r )</td>
<td>Temperature</td>
<td>-</td>
<td>30</td>
<td>45</td>
<td>ns</td>
</tr>
<tr>
<td>Turn-Off Delay Time</td>
<td>( t_d(OFF) )</td>
<td>Time</td>
<td>-</td>
<td>18</td>
<td>29</td>
<td>ns</td>
</tr>
<tr>
<td>Fall Time</td>
<td>( t_f )</td>
<td>-</td>
<td>-</td>
<td>20</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>Total Gate Charge (Gate to Source + Gate to Drain)</td>
<td>( Q_{g(TOT)} )</td>
<td>( V_{GS} = 10\text{V}, I_D = 9.2\text{A}, V_{DS} = 0.8 \times \text{Rated } V_{DSS}, I_{G(REF)} = 1.5\text{mA} ) (Figure 14)</td>
<td>-</td>
<td>10</td>
<td>15</td>
<td>nC</td>
</tr>
<tr>
<td>Gate to Source Charge</td>
<td>( Q_{gs} )</td>
<td>Temperature</td>
<td>-</td>
<td>2.5</td>
<td>-</td>
<td>nC</td>
</tr>
<tr>
<td>Gate to Drain “Miller” Charge</td>
<td>( Q_{gd} )</td>
<td>-</td>
<td>-</td>
<td>2.5</td>
<td>-</td>
<td>nC</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>( C_{ISS} )</td>
<td>( V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz} ) (Figure 11)</td>
<td>-</td>
<td>350</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>( C_{OSS} )</td>
<td>-</td>
<td>-</td>
<td>130</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>Reverse Transfer Capacitance</td>
<td>( C_{RSS} )</td>
<td>-</td>
<td>-</td>
<td>25</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>Internal Drain Inductance</td>
<td>( L_D )</td>
<td>Measured From the Contact Screw On Tab To Center of Die</td>
<td>-</td>
<td>3.5</td>
<td>-</td>
<td>nH</td>
</tr>
<tr>
<td>Internal Source Inductance</td>
<td>( L_S )</td>
<td>Measured From the Source Lead, 6mm (0.25in) From Header to Source Bonding Pad</td>
<td>-</td>
<td>4.5</td>
<td>-</td>
<td>nH</td>
</tr>
<tr>
<td>Thermal Resistance Junction to Case</td>
<td>( R_{jJC} )</td>
<td>-</td>
<td>-</td>
<td>2.5</td>
<td>-</td>
<td>( ^\circ\text{C} / \text{W} )</td>
</tr>
<tr>
<td>Thermal Resistance Junction to Ambient</td>
<td>( R_{jJA} )</td>
<td>Free Air Operation</td>
<td>-</td>
<td>80</td>
<td>-</td>
<td>( ^\circ\text{C} / \text{W} )</td>
</tr>
</tbody>
</table>

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. \( T_J = 25^\circ\text{C} \) to 150\( ^\circ\text{C} \).
Source to Drain Diode Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
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<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Continuous Source to Drain Current</td>
<td>ISD</td>
<td>Modified MOSFET Symbol</td>
<td>-</td>
<td>-</td>
<td>9.2</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Showing the Integral</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reverse P-N Junction Diode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pulse Source to Drain Current (Note 3)</td>
<td>ISDM</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>37</td>
<td>A</td>
</tr>
<tr>
<td>Source to Drain Diode Voltage (Note 2)</td>
<td>VSD</td>
<td>TJ = 25°C, ISD = 9.2A, VGS = 0V</td>
<td>-</td>
<td>-</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(Figure 13)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reverse Recovery Time</td>
<td>trr</td>
<td>TJ = 25°C, ISD = 9.2A, dISD/dt = 100A/µs</td>
<td>5.5</td>
<td>100</td>
<td>240</td>
<td>ns</td>
</tr>
<tr>
<td>Reverse Recovered Charge</td>
<td>QRR</td>
<td>TJ = 25°C, ISD = 9.2A, dISD/dt = 100A/µs</td>
<td>0.25</td>
<td>0.5</td>
<td>1.1</td>
<td>µC</td>
</tr>
</tbody>
</table>

NOTES:
2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. VDD = 25V, starting TJ = 25°C, L = 640mH, Rg = 25Ω, peak IAIS = 9.2A.

Typical Performance Curves Unless Otherwise Specified

![Normalized Power Dissipation vs Case Temperature](image1)

![Maximum Continuous Drain Current vs Case Temperature](image2)

![Maximum Transient Thermal Impedance](image3)
**Typical Performance Curves**  Unless Otherwise Specified  (Continued)

![Figure 4. Forward Bias Safe Operating Area](image1)

**FIGURE 4. FORWARD BIAS SAFE OPERATING AREA**

![Figure 5. Output Characteristics](image2)

**FIGURE 5. OUTPUT CHARACTERISTICS**

![Figure 6. Saturation Characteristics](image3)

**FIGURE 6. SATURATION CHARACTERISTICS**

![Figure 7. Transfer Characteristics](image4)

**FIGURE 7. TRANSFER CHARACTERISTICS**

![Figure 8. Drain to Source On Resistance vs Gate Voltage and Drain Current](image5)

**FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT**

![Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature](image6)

**FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE**
**Typical Performance Curves**  Unless Otherwise Specified  (Continued)

**FIGURE 10.** NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

**FIGURE 11.** CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

**FIGURE 12.** TRANSCONDUCTANCE vs DRAIN CURRENT

**FIGURE 13.** SOURCE TO DRAIN DIODE VOLTAGE

**FIGURE 14.** GATE TO SOURCE VOLTAGE vs GATE CHARGE
Test Circuits and Waveforms

FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

FIGURE 17. SWITCHING TIME TEST CIRCUIT

FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

FIGURE 19. GATE CHARGE TEST CIRCUIT

FIGURE 20. GATE CHARGE WAVEFORMS
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