Agilent HCPL-3180
2.0 Amp Output Current
High Speed Gate Drive
Optocoupler
Data Sheet

Features
- 2.0 A minimum peak output current
- 250 kHz maximum switching speed
- High speed response:
  200 ns maximum propagation delay
  over temperature range
- 10 kV/µs minimum Common Mode
  Rejection (CMR) at VCM = 1500 V
- Under Voltage Lock-Out protection
  (UVLO) with hysteresis
- Wide operating temperature range:
  -40°C to 100°C
- Wide VCC operating range:
  10 V to 20 V
- 20 ns typical pulse width distortion
- Safety approvals:
  - UL approval, 3750 Vrms for
    1 minute
  - CSA approval
  - IEC/EN/DIN EN 60747-5-2
    approval

Applications
- Plasma Display Panel (PDP)
- Distributed Power Architecture
  (DPA)
- Switch Mode Rectifier (SMR)
- High performance DC/DC converter
- High performance Switching Power
  Supply (SPS)
- High performance Uninterruptible
  Power Supply (UPS)
- Isolated IGBT/Power MOSFET gate
  drive

Description
This family of devices consists of a
GaAsP LED. The LED is optically
coupled to an integrated circuit
with a power stage. These
optocouplers are ideally suited for
high frequency driving of power
IGBTs and MOSFETs used in
Plasma Display Panels, high
performance DC/DC converters,
and motor control inverter
applications.

A 0.1 µF bypass capacitor must be connected between pins VCC and Ground.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation, which may be induced by ESD.
Ordering Information
Specify part number followed by option number (if desired).

Example:

HCPL-3180-XXXX

- No option = Standard DIP package, 50 per tube.
- 300 = Gull Wing Surface Mount Option, 50 per tube.
- 500 = Tape and Reel Packaging Option, 1000 per reel.
- 060 = IEC/EN/DIN EN 60747-5-2, \( V_{\text{FORM}} = 630 \, V_{\text{PEAK}} \).
- XXXE = Lead Free Option.

Package Outline Drawings
HCPL-3180 Standard DIP Package

DIMENSIONS IN MILLIMETERS AND (INCHES).
* MARKING CODE LETTER FOR OPTION NUMBERS
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.
NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.
HCPL-3180 Gull Wing Surface Mount Option 300

**Land Pattern Recommendation**

**Dimensions in Millimeters (Inches).**
Lead Coplanarity = 0.10 mm (0.004 inches).

NOTE: Floating lead protrusion is 0.25 mm (10 mils) max.

**Solder Reflow Temperature Profile**

- Preheating Rate: 3°C + 1°C to -0.5°C/sec.
- Reflow Heating Rate: 2.5°C ± 0.5°C/sec.
- Peak Temp: 240°C
- Soldering Time: 100°C, 90 ± 30 sec.
- TIGHT TYPICAL - LOOSE
**Regulatory Information**

The HCPL-3180 has been approved by the following organizations:

**IEC/EN/DIN EN 60747-5-2**

Approved under:
- DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01 (Option 060 only)

**UL**

Approval under UL 1577, component recognition program up to $V_{ISO} = 3750 \text{ V}_{rms}$. File E55361.

**CSA**

Approval under CSA Component Acceptance Notice #5, File CA 88324.

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**IEC/EN/DIN EN 60747-5-2 Insulation Characteristics (HCPL-3180 Option 060)**

<table>
<thead>
<tr>
<th>Description</th>
<th>Symbol</th>
<th>HCPL-3180</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Installation classification per DIN EN 0110 1997-04</td>
<td></td>
<td>I - IV</td>
<td></td>
</tr>
<tr>
<td>for rated mains voltage $\leq 150 \text{ V}_{rms}$</td>
<td></td>
<td>I - III</td>
<td></td>
</tr>
<tr>
<td>for rated mains voltage $\leq 300 \text{ V}_{rms}$</td>
<td></td>
<td>I - II</td>
<td></td>
</tr>
<tr>
<td>for rated mains voltage $\leq 600 \text{ V}_{rms}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Climatic Classification</td>
<td></td>
<td>55/100/21</td>
<td></td>
</tr>
<tr>
<td>Pollution Degree (DIN EN 0110 1997-04)</td>
<td></td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Maximum Working Insulation Voltage</td>
<td>$V_{ORM}$</td>
<td>630</td>
<td>$V_{peak}$</td>
</tr>
<tr>
<td>Input to Output Test Voltage, Method b*</td>
<td>$V_{PR}$</td>
<td>1181</td>
<td>$V_{peak}$</td>
</tr>
<tr>
<td>$V_{ORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m=1 \text{ sec}$, Partial Discharge $&lt; 5 \text{ pC}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input to Output Test Voltage, Method a*</td>
<td>$V_{PR}$</td>
<td>945</td>
<td>$V_{peak}$</td>
</tr>
<tr>
<td>$V_{ORM} \times 1.5 = V_{PR}$, Type and Sample Test, $t_m=60 \text{ sec}$, Partial Discharge $&lt; 5 \text{ pC}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 10 \text{ sec}$)</td>
<td>$V_{IOTM}$</td>
<td>6000</td>
<td>$V_{peak}$</td>
</tr>
<tr>
<td>Safety-limiting values – maximum values allowed in the event of a failure.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Case Temperature</td>
<td>$T_S$</td>
<td>175</td>
<td>°C</td>
</tr>
<tr>
<td>Input Current**</td>
<td>$I_{S,INPUT}$</td>
<td>230</td>
<td>mA</td>
</tr>
<tr>
<td>Output Power**</td>
<td>$P_{S,OUTPUT}$</td>
<td>600</td>
<td>mW</td>
</tr>
<tr>
<td>Insulation Resistance at $T_S$, $V_{IO} = 500 \text{ V}$</td>
<td>$R_S$</td>
<td>$&gt;10^9$</td>
<td>Ω</td>
</tr>
</tbody>
</table>

* Refer to the optocoupler section of the Isolation and Control Components Designer’s Catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-2 for a detailed description of Method a and Method b partial discharge test profiles.

** Refer to the following figure for dependence of $P_S$ and $I_S$ on ambient temperature.
### Insulation and Safety Related Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>HCPL-3180</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum External Air Gap (Clearance)</td>
<td>L(101)</td>
<td>7.1</td>
<td>Measured from input terminals to output terminals, shortest distance through air.</td>
</tr>
<tr>
<td>Minimum External Tracking (Creepage)</td>
<td>L(102)</td>
<td>7.4</td>
<td>Measured from input terminals to output terminals, shortest distance path along body.</td>
</tr>
<tr>
<td>Minimum Internal Plastic Gap (Internal Clearance)</td>
<td>0.08</td>
<td>mm</td>
<td>Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.</td>
</tr>
<tr>
<td>Tracking Resistance (Comparative Tracking Index)</td>
<td>CTI</td>
<td>&gt;175</td>
<td>DIN IEC 112/VDE 0303 Part 1</td>
</tr>
<tr>
<td>Isolation Group</td>
<td></td>
<td>IIIa</td>
<td>Material Group (DIN VDE 0110, 1/89, Table 1)</td>
</tr>
</tbody>
</table>

**Note:** Option 300 – surface mount classification is Class A in accordance with CECC 00802.

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage Temperature</td>
<td>$T_S$</td>
<td>-55</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>$T_J$</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Average Input Current</td>
<td>$I_{F(AVG)}$</td>
<td>25</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak Transient Input Current (&lt;1 µs pulse width, 300 pps)</td>
<td>$I_{F(TRAN)}$</td>
<td>1.0</td>
<td>A</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Reverse Input Voltage</td>
<td>$V_R$</td>
<td>5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>“High” Peak Output Current</td>
<td>$I_{OH(PEAK)}$</td>
<td>2.5</td>
<td>A</td>
<td></td>
<td>2</td>
</tr>
<tr>
<td>“Low” Peak Output Current</td>
<td>$I_{OL(PEAK)}$</td>
<td>2.5</td>
<td>A</td>
<td></td>
<td>2</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>$V_{CC-VEE}$</td>
<td>-0.5</td>
<td>25</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output Voltage</td>
<td>$V_{O(PEAK)}$</td>
<td>0</td>
<td>$V_{CC}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output Power Dissipation</td>
<td>$P_O$</td>
<td>250</td>
<td>mW</td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>Total Power Dissipation</td>
<td>$P_T$</td>
<td>295</td>
<td>mW</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td>Lead Solder Temperature</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Solder Reflow Temperature Profile</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:** Lead Solder Temperature 260°C for 10 sec., 1.6 mm below seating plane

**Note:** Solder Reflow Temperature Profile See Package Outline Drawings section
### Electrical Specifications (DC)

Over recommended operating conditions unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
<th>Fig.</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt;-V&lt;sub&gt;EE&lt;/sub&gt;</td>
<td>10</td>
<td></td>
<td>20</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Current (ON)</td>
<td>I&lt;sub&gt;F(ON)&lt;/sub&gt;</td>
<td>10</td>
<td></td>
<td>16</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage (OFF)</td>
<td>V&lt;sub&gt;F(OFF)&lt;/sub&gt;</td>
<td>-3.0</td>
<td></td>
<td>0.8</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>T&lt;sub&gt;A&lt;/sub&gt;</td>
<td>-40</td>
<td></td>
<td>100</td>
<td>°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High Level Output Current</td>
<td>I&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>0.5</td>
<td></td>
<td>2.0</td>
<td>A</td>
<td>V&lt;sub&gt;O&lt;/sub&gt; = V&lt;sub&gt;CC&lt;/sub&gt;-4</td>
<td>2, 3, 17</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V&lt;sub&gt;O&lt;/sub&gt; = V&lt;sub&gt;CC&lt;/sub&gt;-10</td>
<td>2, 3, 17</td>
<td>2</td>
</tr>
<tr>
<td>Low Level Output Current</td>
<td>I&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>0.5</td>
<td></td>
<td>2.0</td>
<td>A</td>
<td>V&lt;sub&gt;O&lt;/sub&gt; = V&lt;sub&gt;EE&lt;/sub&gt;+2.5</td>
<td>5, 6, 18</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V&lt;sub&gt;O&lt;/sub&gt; = V&lt;sub&gt;EE&lt;/sub&gt;+10</td>
<td>5, 6, 18</td>
<td>2</td>
</tr>
<tr>
<td>High Level Output Voltage</td>
<td>V&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt;-4</td>
<td></td>
<td></td>
<td>V</td>
<td>I&lt;sub&gt;0&lt;/sub&gt; = -100 mA</td>
<td>1, 3, 19</td>
<td>6, 7</td>
</tr>
<tr>
<td>Low Level Output Voltage</td>
<td>V&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
<td>I&lt;sub&gt;0&lt;/sub&gt; = 100 mA</td>
<td>4, 6, 20</td>
<td></td>
</tr>
<tr>
<td>High Level Supply Current</td>
<td>I&lt;sub&gt;CCH&lt;/sub&gt;</td>
<td>3.0</td>
<td>6.0</td>
<td></td>
<td>mA</td>
<td>Output Open</td>
<td>7, 8</td>
<td></td>
</tr>
<tr>
<td>Low Level Supply Current</td>
<td>I&lt;sub&gt;CCL&lt;/sub&gt;</td>
<td>3.0</td>
<td>6.0</td>
<td></td>
<td>mA</td>
<td>Output Open</td>
<td>7, 8</td>
<td></td>
</tr>
<tr>
<td>Threshold Input Current</td>
<td>I&lt;sub&gt;FLH&lt;/sub&gt;</td>
<td>8.0</td>
<td></td>
<td></td>
<td>mA</td>
<td>I&lt;sub&gt;0&lt;/sub&gt; = 0 mA, V&lt;sub&gt;O&lt;/sub&gt; &gt; 5 V</td>
<td>9, 15, 21</td>
<td></td>
</tr>
<tr>
<td>Low to High</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Threshold Input Voltage</td>
<td>V&lt;sub&gt;FHL&lt;/sub&gt;</td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High to Low</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Forward Voltage</td>
<td>V&lt;sub&gt;F&lt;/sub&gt;</td>
<td>1.2</td>
<td>1.5</td>
<td>1.8</td>
<td>V</td>
<td>I&lt;sub&gt;F&lt;/sub&gt; = 10 mA</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>Temperature Coefficient</td>
<td>ΔV&lt;sub&gt;F&lt;/sub&gt;/ ΔT&lt;sub&gt;A&lt;/sub&gt;</td>
<td>-1.6</td>
<td></td>
<td></td>
<td>mV/ °C</td>
<td>I&lt;sub&gt;F&lt;/sub&gt; = 10 mA</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>Input Forward Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Coefficient</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>UVLO Threshold</td>
<td>V&lt;sub&gt;UVLO+&lt;/sub&gt;</td>
<td>7.9</td>
<td></td>
<td></td>
<td>V</td>
<td>I&lt;sub&gt;F&lt;/sub&gt; = 10 mA, V&lt;sub&gt;O&lt;/sub&gt; &gt; 5 V</td>
<td>22, 33</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;UVLO-&lt;/sub&gt;</td>
<td>7.4</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>UVLO Hysteresis</td>
<td>UVLO&lt;sub&gt;HYST&lt;/sub&gt;</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Reverse Breakdown Voltage</td>
<td>B&lt;sub&gt;V&lt;/sub&gt;</td>
<td>5</td>
<td></td>
<td></td>
<td>V</td>
<td>I&lt;sub&gt;R&lt;/sub&gt; = 10 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>C&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>60</td>
<td></td>
<td></td>
<td>pF</td>
<td>f = 1 MHz, V&lt;sub&gt;F&lt;/sub&gt; = 0 V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Package Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
<th>Fig.</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input-Output Momentary Withstand Voltage</td>
<td>( V_{ISO} )</td>
<td>3750</td>
<td></td>
<td></td>
<td></td>
<td>( T_A = 25^\circ C )</td>
<td>8,9</td>
<td></td>
</tr>
<tr>
<td>Input-Output Resistance</td>
<td>( R_{I-O} )</td>
<td>10[\text{[11]}]</td>
<td>1</td>
<td></td>
<td>( \Omega )</td>
<td>( V_{I-O} = 500 \text{ V} )</td>
<td>9</td>
<td></td>
</tr>
<tr>
<td>Input-Output Capacitance</td>
<td>( C_{I-O} )</td>
<td>1</td>
<td></td>
<td></td>
<td>( \text{pF} )</td>
<td>( \text{Freq} = 1 \text{ MHz} )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. Derate linearly above +70°C free air temperature at a rate of 0.3 mA/°C.
2. Maximum pulse width = 10 μs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with IO peak minimum = 2.0 A. See Application section for additional details on limiting IOL peak.
3. Derate linearly above +70°C, free air temperature at the rate of 4.8 mW/°C.
4. Maximum pulse width = 50 μs, maximum duty cycle = 0.5%.
5. Common mode transient immunity in the high state is the maximum tolerable d\( V_{CM} \)/dt of the common mode pulse \( V_{CM} \) to assure that the output will remain in the high state (i.e. \( V_O > 10 \text{ V} \)).
6. Common mode transient immunity in a low state is the maximum tolerable d\( V_{CM} \)/dt of the common mode pulse, \( V_{CM} \), to assure that the output will remain in a low state (i.e. \( V_O < 1.0 \text{ V} \)).
7. The difference between \( t_{PHL} \) and \( t_{PLH} \) between any two HCPL-3180 parts under same test conditions.
Figure 1. $V_{OH}$ vs. temperature.

Figure 2. $I_{OH}$ vs. temperature.

Figure 3. $V_{OH}$ vs. $I_{OH}$.

Figure 4. $V_{OL}$ vs. temperature.

Figure 5. $I_{OL}$ vs. temperature.

Figure 6. $V_{OL}$ vs. $I_{OL}$.

Figure 7. $I_{CC}$ vs. temperature.

Figure 8. $I_{CC}$ vs. $V_{CC}$.

Figure 9. $I_{FLH}$ vs. temperature.
Figure 10. Propagation delay vs. $V_{CC}$.

Figure 11. Propagation delay vs. $I_f$.

Figure 12. Propagation delay vs. temperature.

Figure 13. Propagation delay vs. $R_g$.

Figure 14. Propagation delay vs. $C_g$.

Figure 15. Transfer characteristics.

Figure 16. Input current vs. forward voltage.
Figure 17. $I_{OH}$ test circuit.

Figure 18. $I_{OL}$ test circuit.

Figure 19. $V_{OH}$ test circuit.

Figure 20. $V_{OL}$ test circuit.

Figure 21. $I_{FLH}$ test circuit.

Figure 22. UVLO test circuit.
Applications Information Eliminating Negative IGBT Gate Drive

To keep the IGBT firmly off, the HCPL-3180 has a very low maximum $V_{OL}$ specification of 0.4 V. The HCPL-3180 realizes the very low $V_{OL}$ by using a DMOS transistor with $1 \text{ } \Omega$ (typical) on resistance in its pull down circuit. When the HCPL-3180 is in the low state, the IGBT gate is shorted to the emitter by $R_g + 1 \text{ } \Omega$. Minimizing $R_g$ and the lead inductance from the HCPL-3180 to the IGBT gate and emitter (possibly by mounting HCPL-3180 on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in Figure 25. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the HCPL-3180 input as this can result in unwanted coupling of transient signals into the input of HCPL-3180 and degrade performance.

(If the IGBT drain must be routed near the HCPL-3180 input, then the LED should be reverse biased when in the off state to prevent the transient signals coupled from the IGBT drain from turning on the HCPL-3180.)
Selecting the Gate Resistor ($R_g$) for HCPL-3180

**Step 1:** Calculate $R_g$ minimum from the $I_{OL}$ peak specification. The IGBT and $R_g$ in Figure 25 can be analyzed as a simple RC circuit with a voltage supplied by the HCPL-3180.

\[
R_g \geq \frac{V_{CC} - V_{OL}}{I_{OL}\text{PEAK}}
\]

\[
= \frac{20 - 3}{2}
\]

\[
= 8.5 \, \Omega
\]

The $V_{OL}$ value of 3 V in the previous equation is the $V_{OL}$ at the peak current of 2 A. (See Figure 6.)

**Step 2:** Check the HCPL-3180 power dissipation and increase $R_g$ if necessary. The HCPL-3180 total power dissipation ($P_T$) is equal to the sum of the emitter power ($P_E$) and the output power ($P_O$).

\[
P_T = P_E + P_O
\]

\[
P_E = I_F \cdot V_F \cdot \text{Duty Cycle}
\]

\[
P_O = P_{O(BIAS)} + P_{O(SWITCHING)}
\]

\[
= I_{CC} \cdot V_{CC} + E_{SW} (R_gQ_g) \cdot f
\]

For the circuit in Figure 25 with $I_F$ (worst case) = 16 mA, $R_g = 10 \, \Omega$, Max Duty Cycle = 80%, $Q_g = 100 \, \text{nC}$, $f = 200 \, \text{kHz}$ and $T_{MAX} = +75^\circ\text{C}$:

\[
P_E = 16 \, \text{mA} \cdot 1.8 \, \text{V} \cdot 0.8 = 23 \, \text{mW}
\]

\[
P_O = 4.5 \, \text{mA} \cdot 20 \, \text{V} + 0.85 \, \mu\text{A} \cdot 200 \, \text{kHz}
\]

\[
= 260 \, \text{mW} \geq 226 \, \text{mW} (P_{O(MAX)} @ 75^\circ\text{C} = 250 \, \text{mW} (5^\circ\text{C} \cdot 4.8 \, \text{mW}/^\circ\text{C}))
\]

The value of 4.5 mA for $I_{CC}$ in the previous equation was obtained by derating the $I_{CC}$ max of 6 mA to $I_{CC}$ max at $+75^\circ\text{C}$. Since $P_O$ for this case is greater than the $P_{O(MAX)}$, $R_g$ must be increased to reduce the HCPL-3180 power dissipation.

\[
P_{O(SWITCHING \, \text{MAX})} = P_{O(MAX)} - P_{O(BIAS)}
\]

\[
= 226 \, \text{mW} - 90 \, \text{mW}
\]

\[
= 136 \, \text{mW}
\]

\[
E_{SW(\, \text{MAX})} = \frac{P_{O(SWITCHING \, \text{MAX})}}{f}
\]

\[
= \frac{136 \, \text{mW}}{200 \, \text{kHz}}
\]

\[
= 0.68 \, \mu\text{W}
\]

For $Q_g = 100 \, \text{nC}$, a value of $E_{sw} = 0.68 \, \mu\text{W}$ gives a $R_g = 15 \, \Omega$. 
Thermal Model
(Discussion applies to HCPL-3180)
The steady state thermal model for the HCPL-3180 is shown in Figure 27. The thermal resistance values given in this model can be used to calculate the temperatures at each node for a given operating condition. As shown by the model, all heat generated flows through $\theta_{CA}$ which raises the case temperature $TC$ accordingly. The value of $\theta_{CA}$ depends on the conditions of the board design and is, therefore, determined by the designer. The value of $\theta_{CA} = +83 \, ^{\circ} C/W$ was obtained from thermal measurements using a 2.5 x 2.5 inch PC board, with small traces (no ground plane), a single HCPL-3180 soldered into the center of the board and still air. The absolute maximum power dissipation derating specifications assume a $\theta_{CA}$ value of $+83 \, ^{\circ} C/W$.

From the thermal model in Figure 27, the LED and detector IC junction temperatures can be expressed as:

$$T_{JE} = P_E \times (57^{\circ} C/W + \theta_{CA}) + P_D \times (111^{\circ} C/W + \theta_{CA}) + T_A$$

$$T_{JD} = P_E \times (57^{\circ} C/W + \theta_{CA}) + P_D \times (140^{\circ} C/W + \theta_{CA}) + T_A$$

For example, given $P_E = 45 \, mW$, $P_O = 250 \, mW$, $T_A = +70 \, ^{\circ} C$ and $\theta_{CA} = +83 \, ^{\circ} C/W$:

$$T_{JE} = (45 \, mW \times 339^{\circ} C/W + 250 \, mW \times 140^{\circ} C/W + 70^{\circ} C)$$

$= 120^{\circ} C$

$$T_{JD} = (45 \, mW \times 140^{\circ} C/W + 250 \, mW \times 194^{\circ} C/W + 70^{\circ} C)$$

$= 125^{\circ} C$

$T_{JE}$ and $T_{JD}$ should be limited to $+125 \, ^{\circ} C$ based on the board layout and part placement ($\theta_{CA}$) specific to the application.
LED Drive Circuit Considerations for Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 28. The HCPL-3180 improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and optocoupler pins 5-8 as shown in Figure 29. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 25), can achieve 10 kV/µs CMR while minimizing component complexity.

Techniques to keep the LED in the proper state are discussed in the next two sections.

Figure 28. Optocoupler input to output capacitance model for unshielded optocouplers.

Figure 29. Optocoupler input to output capacitance model for shielded optocouplers.

CMR with the LED On (CMR_H)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by over-driving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 10 mA provides adequate margin over the maximum I_FLH of 8 mA to achieve 10 kV/µs CMR.

CMR with the LED Off (CMR_L)

A high CMR LED drive circuit must keep the LED off (V_F ≤ V_F(Off)) during common mode transients. For example, during a -dV_CM/dt transient in Figure 30, the current flowing through C_LEDP also flows through the R_SAT and V_SAT of the logic gate. As long as the low state voltage developed across the logic gate is less than V_F(Off), the LED will remain off and no common mode failure will occur.

The open collector drive circuit, shown in Figure 31, cannot keep the LED off during a +dV_CM/dt transient, since all the current flowing through C_LEDN must be supplied by the LED, and it is not recommended for applications requiring ultra high CMR performance. Figure 32 is an alternative drive circuit, which like the recommended application circuit (Figure 25), does achieve ultra high CMR performance by shunting the LED in the off state.

Figure 30. Equivalent circuit for Figure 25 during common mode transient.
Under Voltage Lockout Feature

The HCPL-3180 contains an under voltage lockout (UVLO) feature that is designed to protect the IGBT under fault conditions which cause the HCPL-3180 supply voltage (equivalent to the fully charged IGBT gate voltage) to drop below a level necessary to keep the IGBT in a low resistance state. When the HCPL-3180 output is in the high state and the supply voltage drops below the HCPL-3180 VUVLO- threshold (typ 7.5 V) the optocoupler output will go into the low state. When the HCPL-3180 output is in the low state and the supply voltage rises above the HCPL-3180 VUVLO+ threshold (typ 8.5 V) the optocoupler output will go into the high state (assume LED is “ON”).

IPM Dead Time and Propagation Delay Specifications

The HCPL-3180 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize “dead time” in their power inverter designs. Dead time is the time during which the high and low side power transistors are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices from the high voltage to the low-voltage motor rails.

To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 34. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDDMAX, which is specified to be 90 ns over the operating temperature range of -40 °C to +100 °C.

*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR PDD CALCULATIONS, THE PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.
Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specification as shown in Figure 35. The maximum dead time for the HCPL-3180 is 180 ns (= 90 ns - (-90 ns)) over the operating temperature range of -40 °C to +100 °C.

Figure 35. Waveforms for dead time.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.