Projet 5 - GSCRCP / Générateur de Signal Carré à Rapport Cyclique Programmable

Projet : TRAIN1

Info : [DATA084]

Révision : 1, du 4 juin 1991

Révision : 2, du 26 mai 2001.

Révision : 3, du 17 juin 2001

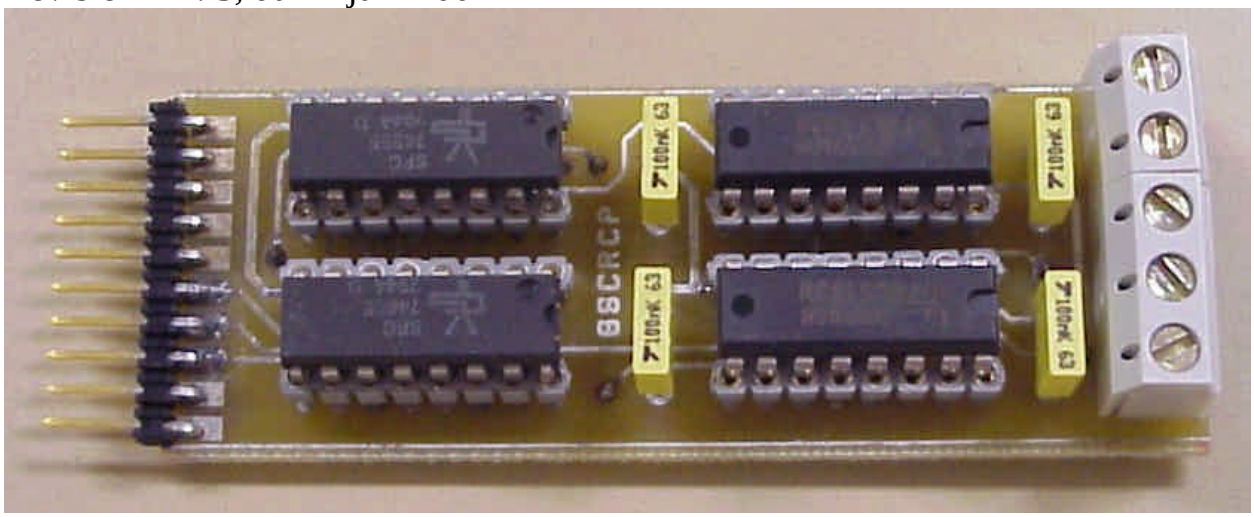


Figure 5.1. GSCRCP (images_maquettes\gscrcp-1.jpg).

5.1 Liste des documents

- Liste des composants.
- Prix du montage.
- Schéma électronique général.
- Schéma électronique d'un commande.
- Implantation des composants
- Circuit imprimé coté composants.
- Circuit imprimé coté cuivre.
- Documentations : 74HC193, 74HC85.

5.2 Calcul de la fréquence de fonctionnement

Les deux compteurs binaire 4 bits 74LS193 forment un compteur binaire 8 bits (de 0 à 255).

La fréquence de base de la MLI correspond à la fréquence d'horloge CLK divisée par 256.

Pour F_{CLK} = 4 MHz, $F_{MLI} = \frac{4 \cdot 10^6}{256} = 15{,}6\,\text{kHz}$.

Pour F_{CLK} = 5 MHz, $F_{MLI} = \frac{5 \cdot 10^6}{256} = 19{,}5\,\text{kHz}$.

5.3 Liste des composants

Tableau 5.1. Liste de composants (projets-train.xls / GSCRCP).

N°	Quantité	Référence	Désignation	Empreinte
1	4	C1,C2,C3,C4	100nF	CK06
2	1	JP1	8 bits	10PL1
3	1	JP2	IN-OUT	03PL2
4	1	JP3	ALIM +5V	02PL2
5	2	U2,U1	74LS193	16DIP300
6	2	U4,U3	74LS85	16DIP300

5.4 Brochages des connecteurs

Tableau 5.2. HE14 mâle coudé 10 points

GND	10
D7	9
D6	8
D5	7
D4	6
D3	5
D2	4
D1	3
D0	2
+5V	1

Tableau 5.3. Connecteurs à visser 5 points

2	GND
1	+5V
3	CLK
2	GND
1	OUT

5.5 Allure des principaux composants

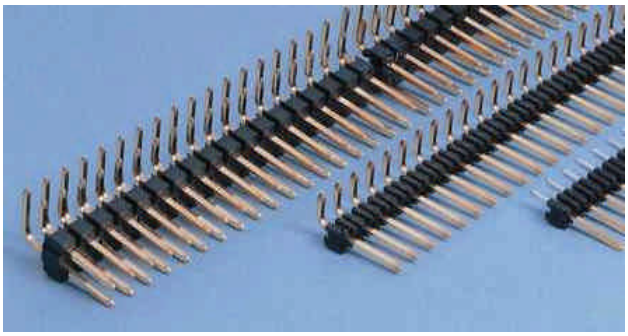


Figure 5.2. Connecteur HE14 mâle coudé (images-composants\barette.jpg).

Figure 5.3. Borniers (images-composants\bornier1.jpg).

5.6 Siganux de sortie pour F_{CLK} = 5 MHz

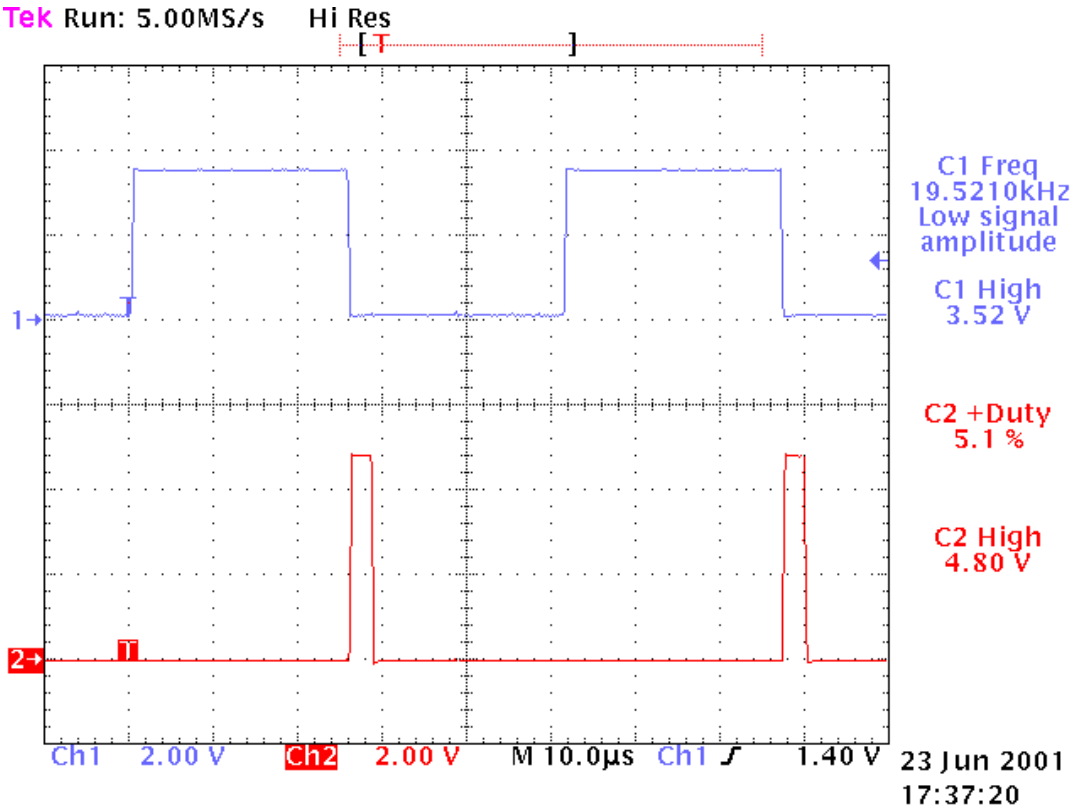


Figure 5.4. Rapport cyclique faible (images-composants\gscrcp01.pcx).

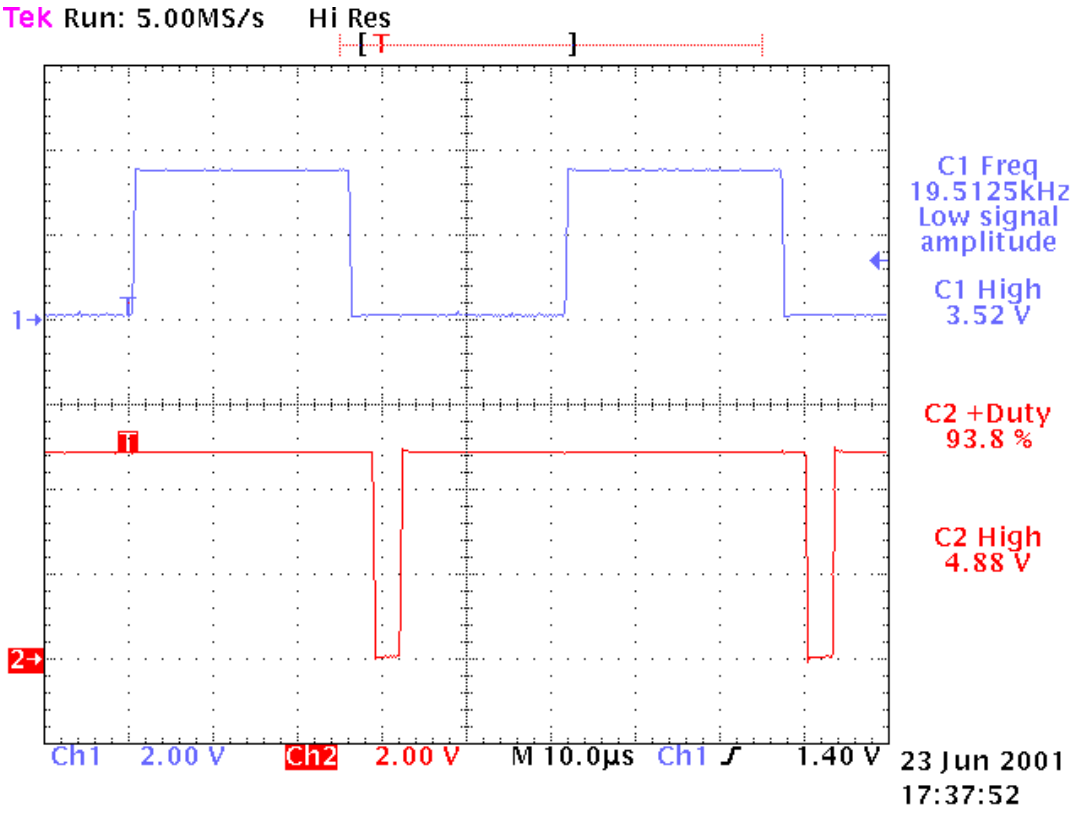
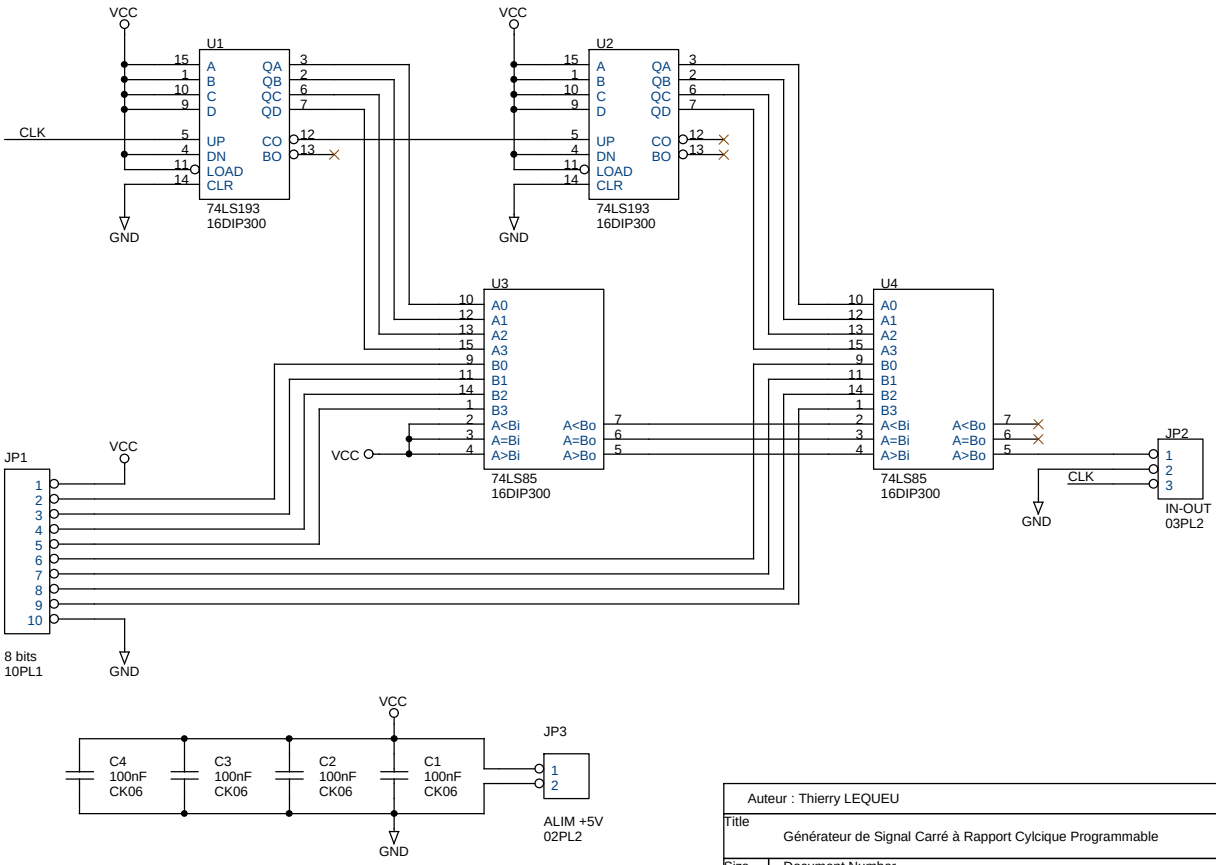
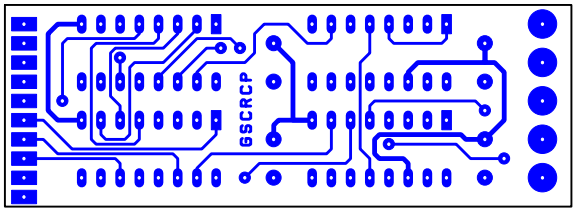
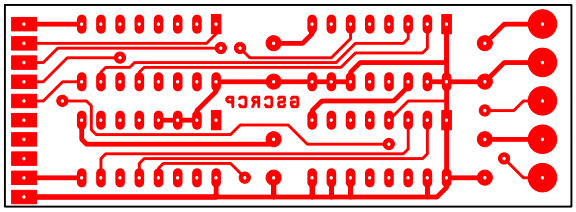


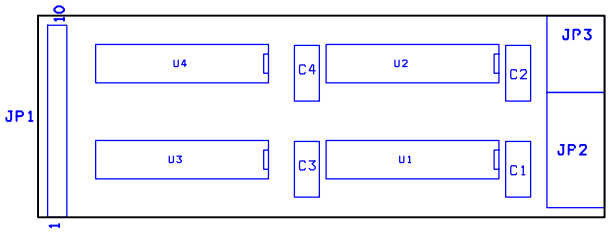
Figure 5.5. Rapport cyclique grand (images-composants\gscrcp02.pcx).

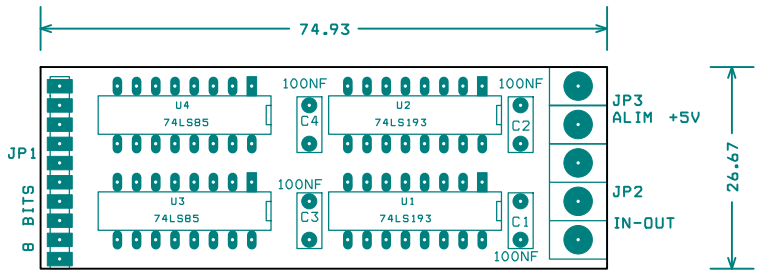


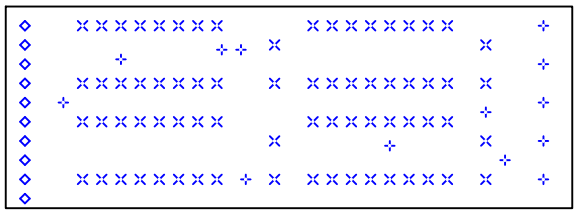
Auteur : Thierry LEQUEU			
Title: Générateur de Signal Carré à Rapport Cylcique Programmable			
Size: A	Document Number: TRAIN1 / [DATA084] / GSCRCP		Rev: 3
Date: Sunday, June 17, 2001	Sheet 1 of 1		


GSCRCP


88CRCP


10
1
JP1
U4
C4
U2
C2
JP3
U3
C3
U1
C1
JP2


74.93
26.67
JP1
8 BITS
U4
74LS85
U3
74LS85
U2
74LS193
U1
74LS193
C4
100NF
C3
100NF
C2
100NF
C1
100NF
JP3
ALIM +5V
JP2
IN-OUT



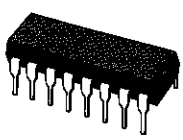
DRILL CHART				
SYM	DIAM	TOL	QTY	NOTE
×	0.508 mm		72	
+	0.787 mm		8	
+	1.000 mm		5	
◇	1.194 mm		10	
TOTAL			95	

SGS-THOMSON MICROELECTRONICS

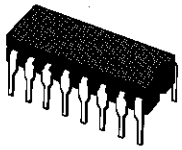
M54/M74HC192
M54/M74HC193

HC192 - SYNCHRONOUS UP/DOWN DECADE COUNTER
HC193 - SYNCHRONOUS UP/DOWN BINARY COUNTER

- HIGH SPEED
  f_{MAX} = 54 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS192-193



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

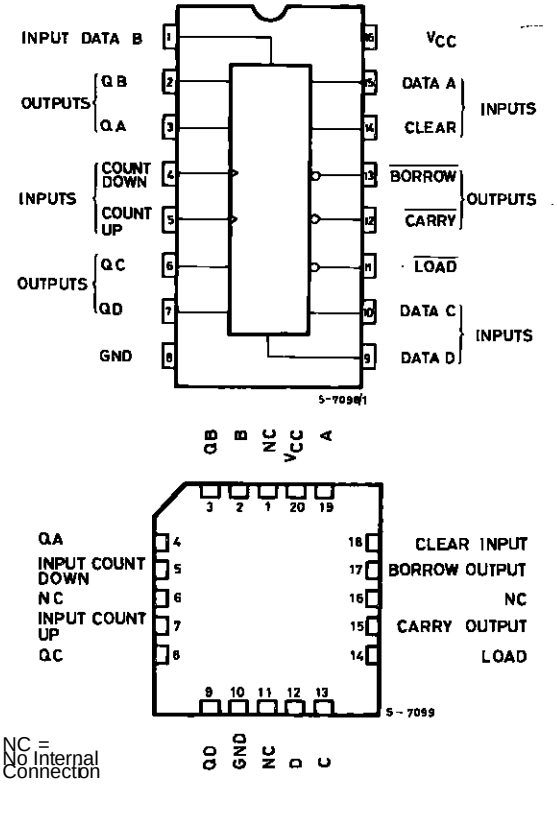
ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

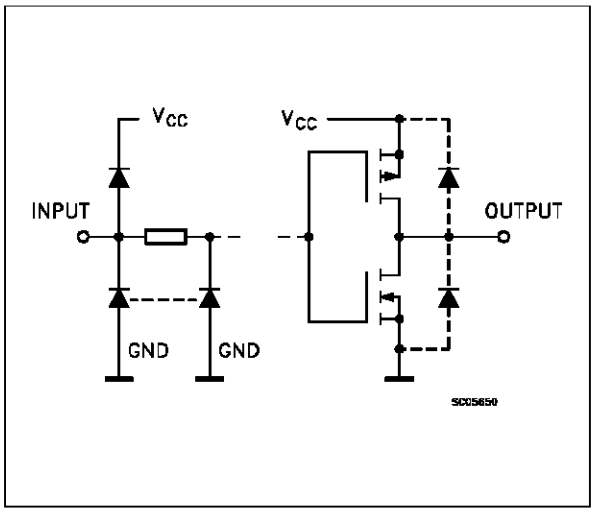
The M54/74HC192/193 are a high speed CMOS SYNCHRONOUS UP/DOWN DECADE COUNTERS fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. The counter has two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flop are simultaneously triggered on the low to high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked. This counter may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D input. When the LOAD input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n counters by modifying the count length with the preset inputs. In addition the counter can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to low independently of either COUNT input. Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counter can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)



NC = No Internal Connection

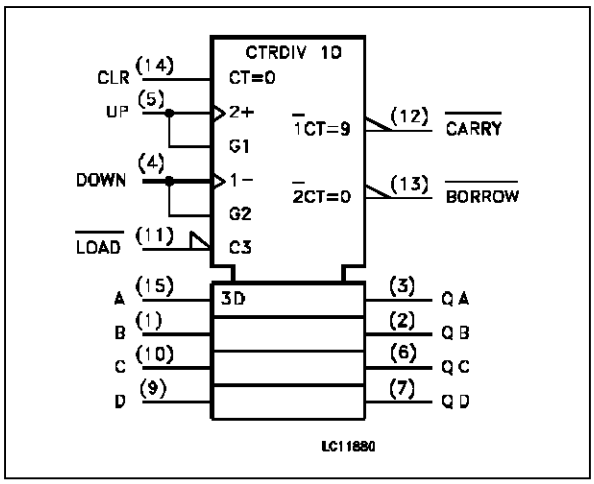
INPUT AND OUTPUT EQUIVALENT CIRCUIT



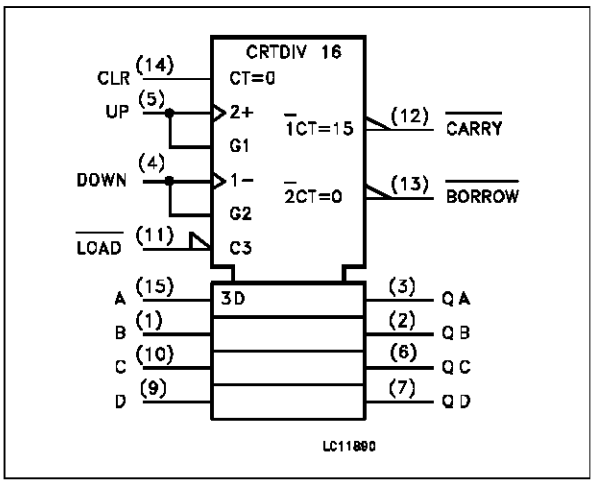
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	QA to QD	Flip-Flop Outputs
4	CP_D	Count Down Clock Input
5	CP_U	Count Up Clock Input
11	$\overline{LOAD}$	Asynchronous Parallel Load Input (Active LOW)
12	$\overline{CARRY}$	Count Up (Carry) Output (Active LOW)
13	$\overline{BORROW}$	Count Down (Borrow) Output (Active LOW)
14	CLEAR	Asynchronous Reset Input (Active HIGH)
15, 1, 10, 9	DA to DD	Data Inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL (HC191)



IEC LOGIC SYMBOL (HC193)

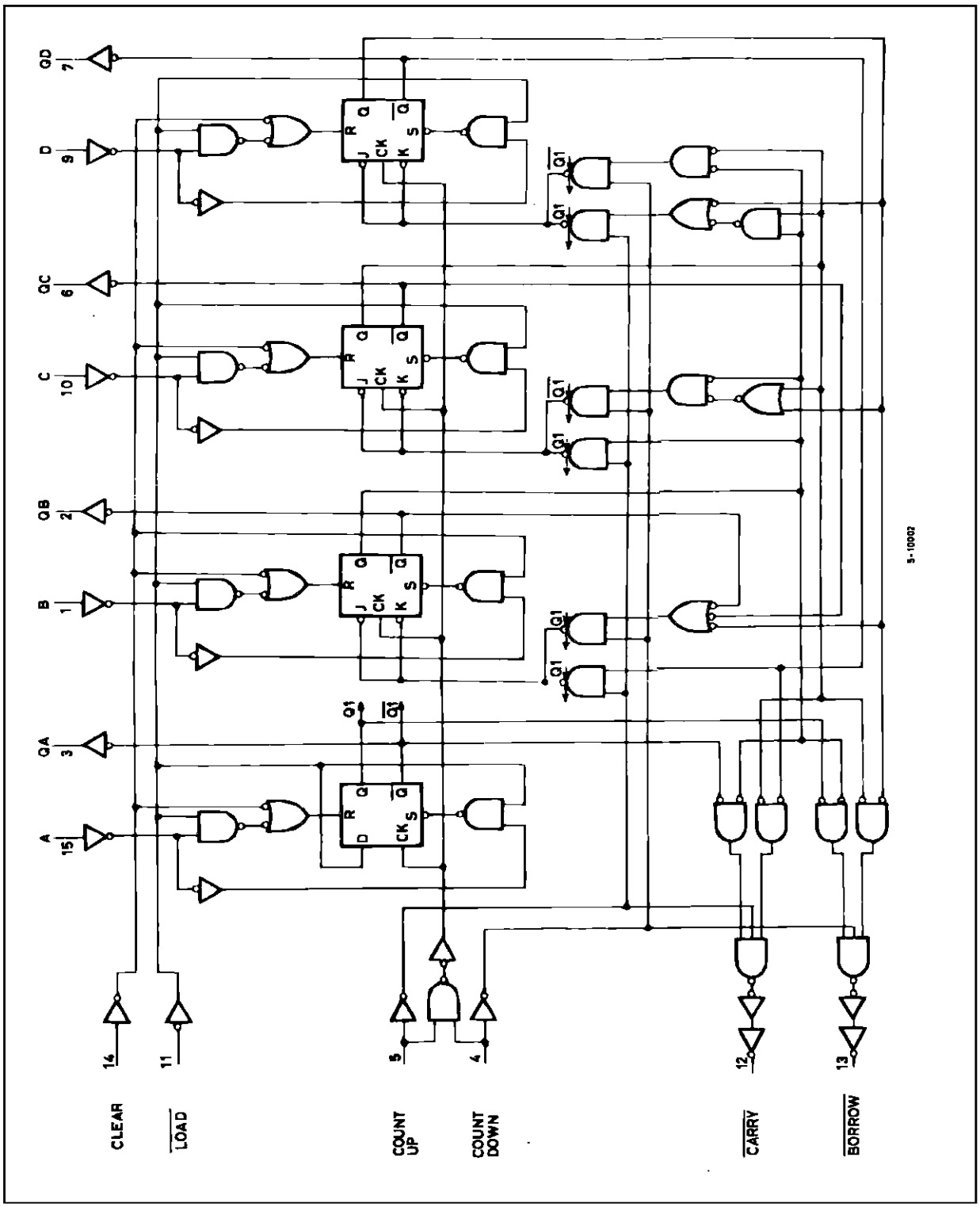


TRUTH TABLE

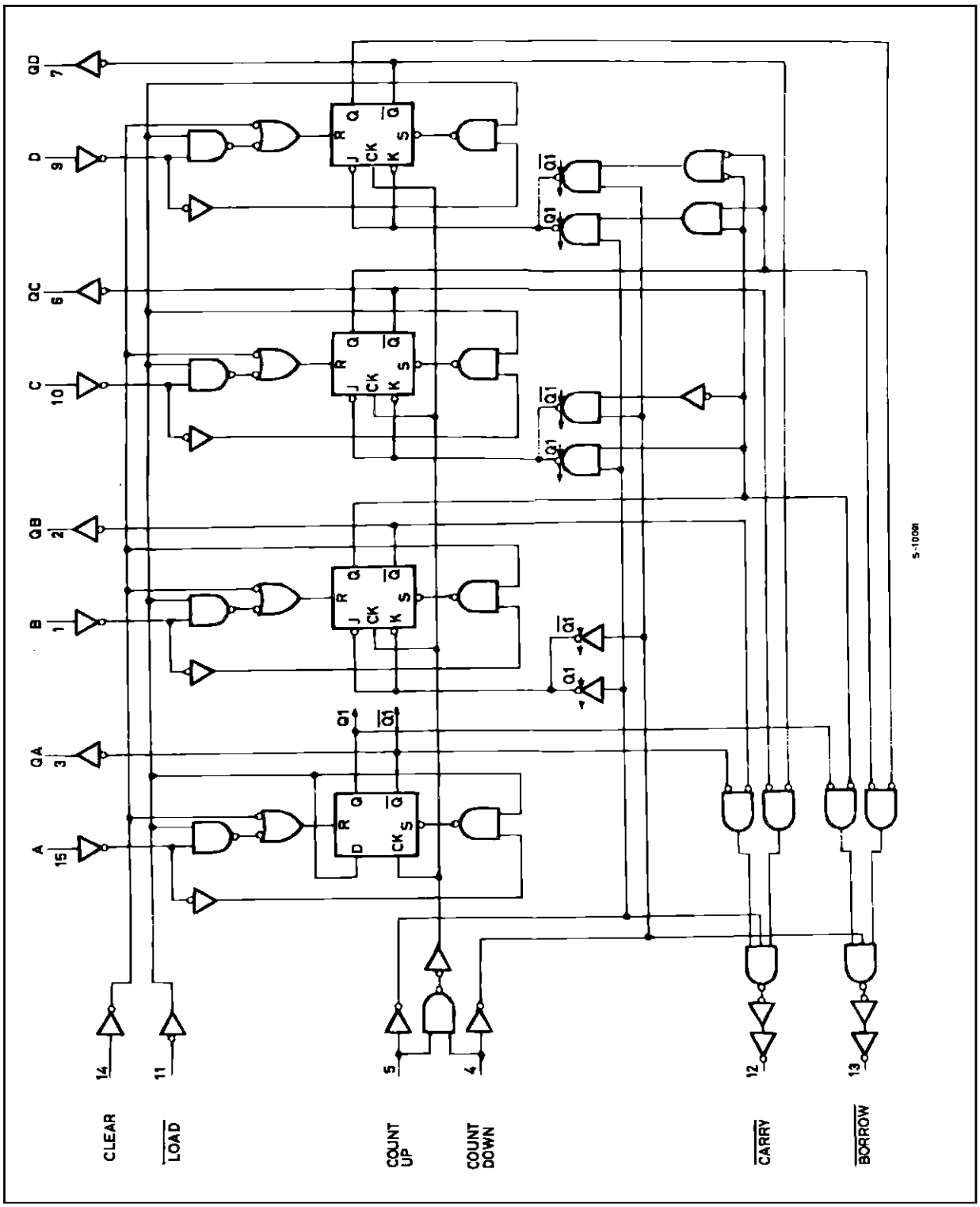
COUNT UP	COUNT DOWN	$\overline{LOAD}$	CLEAR	FUNCTION
⎍	H	H	L	COUNT UP
⎏	H	H	L	NO COUNT
H	⎍	H	L	COUNT DOWN
H	⎏	H	L	NO COUNT
X	X	L	L	PRESET
X	X	X	H	RESET

X: Don't Care

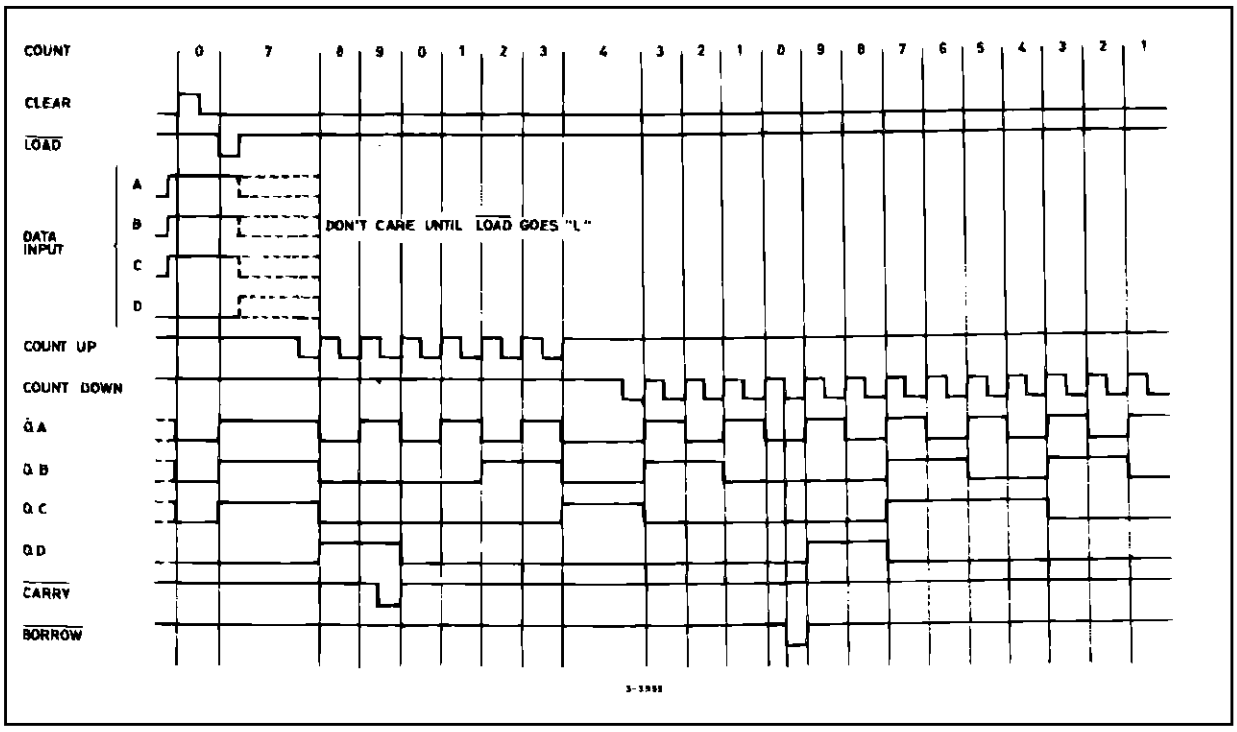
LOGIC DIAGAM (HC192)



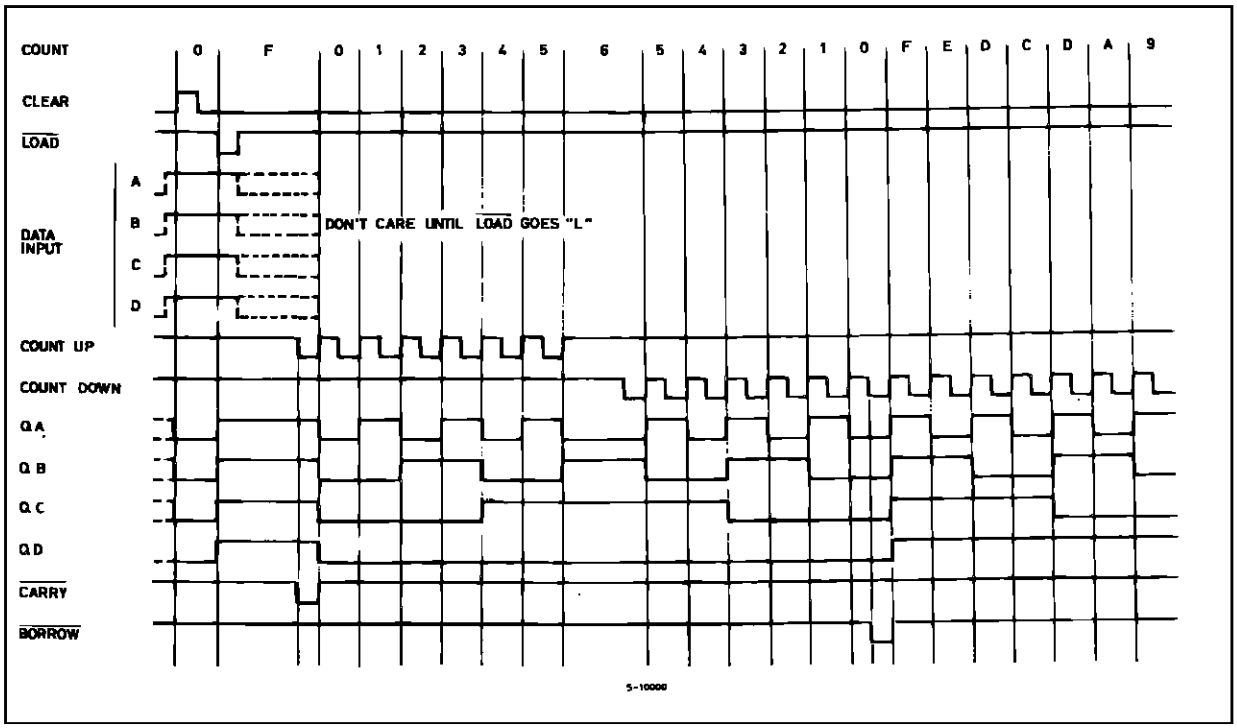
LOGIC DIAGAM (HC193)



TIMING DIAGRAM (HC192)



TIMING DIAGRAM (HC193)

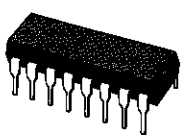


SGS-THOMSON MICROELECTRONICS

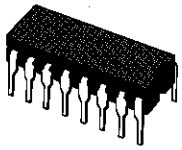
M54HC85
M74HC85

4-BIT MAGNITUDE COMPARATOR

- HIGH SPEED
  t_{PD} = 22 ns (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS85



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

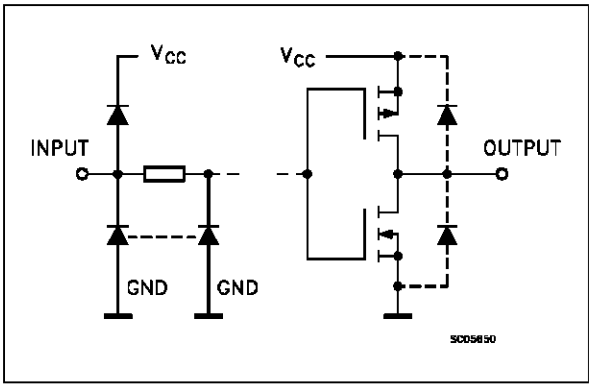
ORDER CODES :

M54HC85F1R M74HC85M1R
M74HC85B1R M74HC85C1R

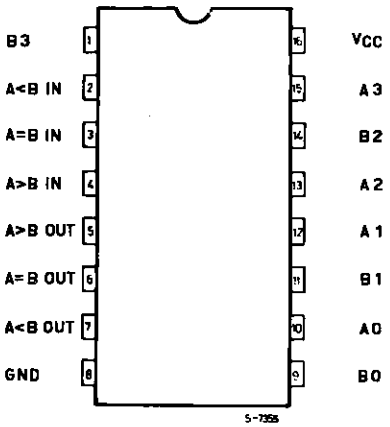
DESCRIPTION

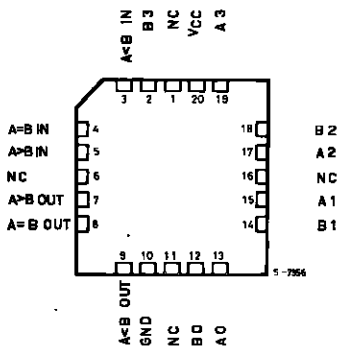
The M54/74HC85 is a high speed CMOS 4-BIT MAGNITUDE COMPARATOR fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This comparator compares two 4-bit words and provides a high voltage level on one of the A > B out, A = B out and A < B out outputs. The comparing bit number is easily expanded by cascading several devices as shown in the typical application. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



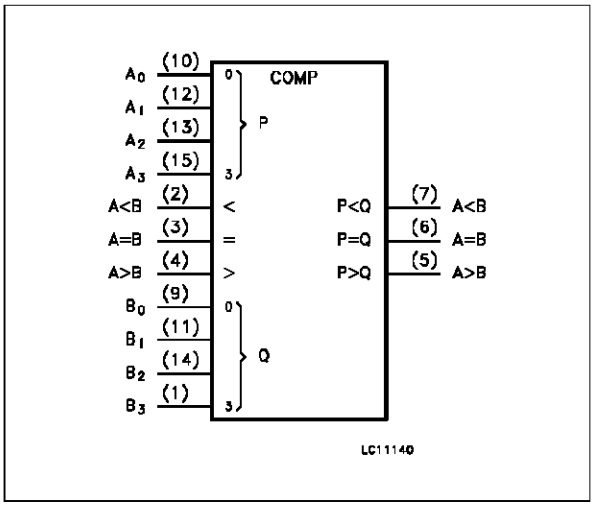


NC =
No Internal
Connection

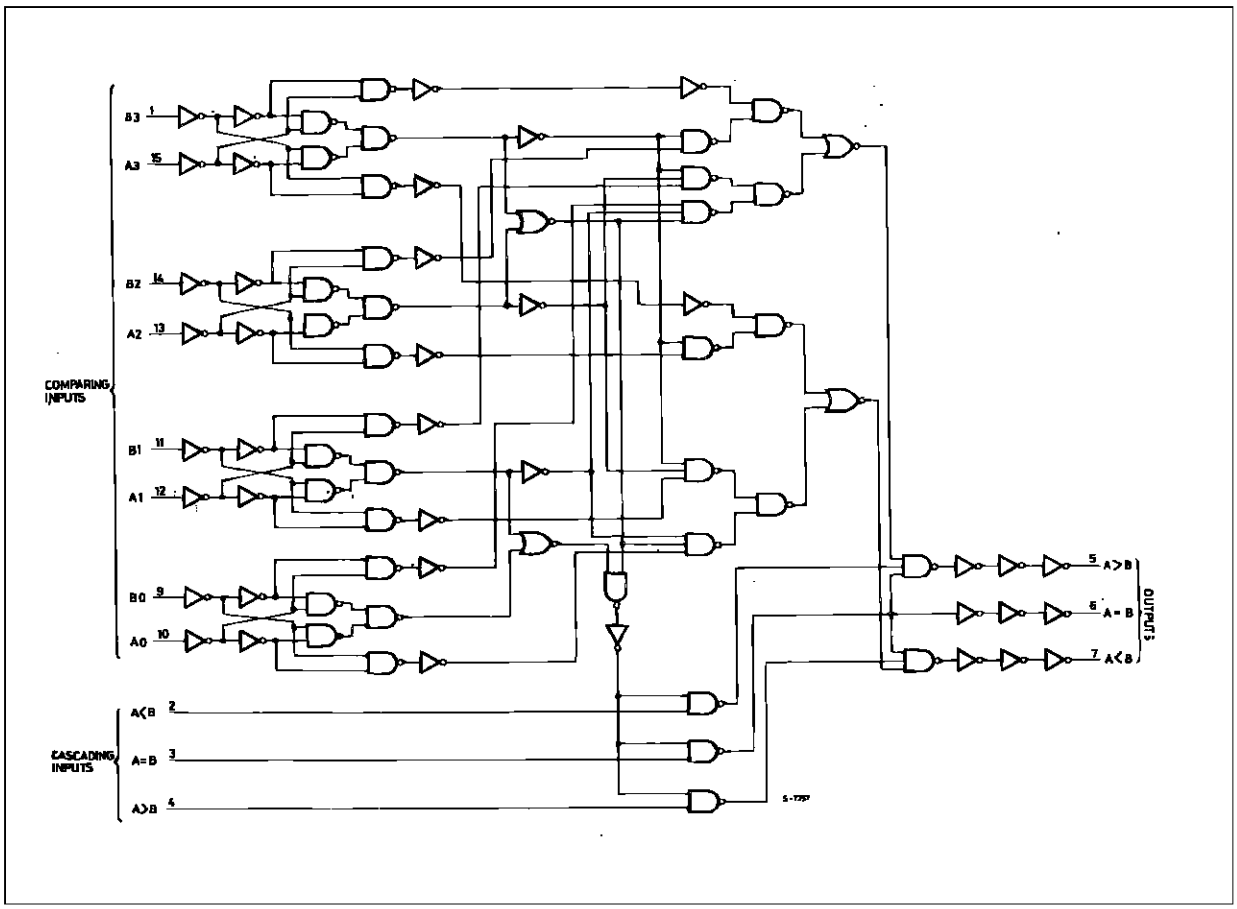
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
2	$IN_{A<B}$	A<B Expansion Input
3	$IN_{A=B}$	A=B Expansion Input
4	$IN_{A>B}$	A>B Expansion Input
5	$OUT_{A>B}$	A>B Expansion Output
6	$OUT_{A=B}$	A=B Expansion Output
7	$OUT_{A<B}$	A<B Expansion Output
9, 11, 14, 1	B_0 to B_3	Word B Inputs
10, 12, 13, 15	A_0 to A_3	Word A Inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOCIG DIAGRAM



TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
				A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L
				X	X	H	L	L	H
				L	H	L	L	H	L
				H	L	L	H	L	L
				H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3<B3	X	X	X	X	X	X	L	H	L

X: DON'T CARE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C