Monday		

7.30	60	Registration

8.30		Start Monday Morning Sessions

		Opening Session
8.30	10	Opening

Session 1:		Keynote session: Industrial Trends
8.40	30	Keynote: **Roadmap Challenges – There is More than Moore** ***A. J. van Roosmalen*** *Philips Semiconductors, Eindhoven, the Netherlands*
9.10	30	Keynote: **Opportunities and Challenges for Telecommunications Technology** ***J. Rantala*** *Nokia Research Center, Helsinki, Finland*
9.40	30	Keynote: **Trends in automotive electronics** ***H. Casier*** *AMI Semiconductor Belgium BVBA, Oudenaarde, Belgium*
10.10	30	Keynote: **Trends & Challenges in Microsystems Packaging** ***M. K. Iyer*** *Microsystems, Modules & Components Lab, Institute of Microelectronics (IME), Singapore*

10.40	30	Break

Session 2:		Keynote session: Technology Developments
11.10	30	Keynote: **Nano-electronics in Biological Applications** ***G. Borghs*** *IMEC, Leuven, Belgium*
11.40	30	Keynote: **Reliability Challenges and Recent Advances for Cu Interconnects** ***Paul S. Ho[a*], Ki-Don Lee[b], Sean Yoon[a], Guotao Wang[a]*** *[a]Laboratory for Interconnect and Packaging, University of Texas at Austin, USA* *[b]Silicon Technology Development, Texas Instruments, Inc., Dallas, USA*
12.10	30	Keynote: **From Macro-Cooling to Micro-Reliability** ***M.R.D. Davies*** *Stokes Research Institute, University of Limerick, Ireland*

12.40	100	Lunch

14.20		Monday Afternoon Sessions

	Parallel sessions				
14.20-15.50	Session 3		Session 4		Session 5
	Virtual Thermal Mechanical Prototyping		Thermal Mechanical Behavior on Wafer Level		Dynamic Compact Thermal and Electro-Thermal Models

Session 3:		Virtual Thermal Mechanical Prototyping
14.20	30	Keynote: **Modeling of Cure-Induced Warpage of Plastic IC Packages** ***D.G. Yang[1], K.M.B. Jansen[1], L.J. Ernst[1], G.Q. Zhang[2], W.D. van Driel, H.J.L. Bressers[3]*** *[1)]Delft University of Technology, The Netherlands,* *[2)]Philips-CFT, Eindhoven, The Netherlands* *[3)]Philips Semiconductors, Nijmegen, The Netherlands*
14.50	20	**Thermo-Mechanical Stress Modelling of MOS Device with Electro-thermal Considerations** ***P. Tounsi[*], J.P. Fradin[***], X. Chauffleur[***], Ph. Dupuy[**], J.M. Dorkel[*], A. Marty*, A. Deram[**]*** *[*)] LAAS/CNRS, Toulouse Cedex, France* *[**)] MOTOROLA Semiconducteurs SA, Toulouse Cedex, France* *[***)] EPSILON Ingénierie, California, Labège Cedex, France*
15.10	20	**FEM-based Method to Determinate Mechanical Stress Evolution during Process Flow in Microelectronics – Application to Stress-Voiding** ***S. Orain[1], J.C Barbé[2], X. Federspiel[1], P. Legallo[3], H. Jaouen[4]*** *[1)] PHILIPS semiconductors, Crolles cedex ; France* *[2)] CEA-DRT-LETI/DTS, Grenoble Cedex, France* *[3)] CEA-DRT/DTEN, Grenoble Cedex, France* *[4)] STMicroelectronics, Crolles Cedex, France*
15.30	20	**On Wire Failures in Micro-electronic Packages** ***W.D. van Driel[1], J.H.J. Jansen , G.Q. Zhang[2],M.A.J. van Gils[2], R.B.R. van Silfhout[2], L.J. Ernst[3]*** *[1)] ATO Innovation/Philips Semiconductors, Nijmegen, The Netherlands* *[2)] Center for Industrial Technology/Philips, Eindhoven, The Netherlands* *[3)] Delft University of Technology, 2628 CD Delft, The Netherlands*

Session 4:		Thermal Mechanical Behavior on Wafer Level
14.20	30	Keynote: **A Finite Element Study of Process Induced Stress in the Transistor Channel: Effects of Silicide Contact and Gate Stack** ***C.Torregiani[1,2], J. Liu[3], B.Vandevelde[1], D.Degryse[1], M.J.Van Dal[4], A. Benedetti, A.Lauwers[1], K.Maex[1,2].*** *[1)] IMEC, Leuven, Belgium* *[2)] E.E. Dept. K.U.Leuven, Leuven, Belgium* *[3)] E.E. Dept. Stanford University, Stanford, California, USA* *[4)] Philips Research Leuven, Leuven, Belgium*
14.50	20	**Effect of Metal Layout Design on Passivation Crack Occurrence using both Experimental and Simulation Techniques** ***R.B.R van Silfhout[1)], W.D. van Driel[2)], Y.Li[2)], M.A.J. van Gils[1)], J.H.J. Janssen[2)], G.Q. Zhang[1)], G. Tao[2)], J. Bisschop[2)], L.J. Ernst[3)]*** *[1)] Philips Centre for Industrial Technology, Eindhoven, The Netherlands* *[2)] Philips Semiconductors, ATO Innovation, Nijmegen, The Netherlands* *[3)]Delft University of Technology, The Netherlands*
15.10	20	**Probability of Silicon Fracture in Molded Packages** ***C. Bohm*, T. Hauck*, W. H. Müller**, A. Juritza*** *[*)] Motorola GmbH, Schatzbogen 7, 81829 München* *[**)] Technische Universität Berlin, Einsteinufer 5, 10587 Berlin*
15.30	20	**Interfacial Sliding and Plasticity in Back-end Interconnect Structures of Microelectronic devices** ***I. Dutta[1], D. Pan, C. Park[1], J. Vella[2]*** *[1)] Center for Materials Science and Engineering, Department of Mechanical Engineering, Naval Postgraduate School, Monterey, CA, USA* *[2)] Process and Materials Characterization Laboratory, Motorola, Tempe, AZ, USA*

Session 5:		**Dynamic Compact Thermal and Electro-Thermal Models**
14.20	**30**	**Keynote: Empirical Validation of Thermal Dynamics in a Silicon Microthruster: Influence of the Boundary Conditions** ***M. Salleras, I. García, J. Palacín, M. Puig, J. Samitier, S. Marco*** *Sistemes d'Instrumentació i Communicacions, Departament d'Electrònica, Universitat de Barcelona, Spain*
14.50	**20**	**Compact Electro-thermal Models of Semiconductor Devices with Multiple Heat Sources** ***C. Bohm, T. Hauck, E.B. Rudnyi, J. G. Korvink*** *Motorola, Germany IMTEK, University of Freiburg, Germany*
15.10	**20**	**Electro-Thermal Transistor Models in the SISSI Electro-Thermal IC Simulator** *V.Székely, A.Poppe, G.Hajas* *Budapest University of Technology and Economics, Hungary*

15.50	**40**	**Break**

	Parallel sessions				
16.30-18.00	**Session 6**		**Session 7**		**Session 8**
	Experimental and Numerical Interaction		**Modeling and Designing of Advanced Packaging**		**Thermal Behavior Modeling and Characterization**

Session 6:		**Experimental and Numerical Interaction**
16.30	**30**	**Keynote: Computational Model Validation with Experimental Data from Temperature Cycling Tests of PBGA Assemblies for the Analysis of Board Level Solder Joint Reliability** ***R. Lee, D. Lau*** *Electronic Packaging Laboratory, Department of Mechanical Engineering* *Hong Kong University of Science & Technology, Hong Kong*
17.00	**20**	**PWB Warpage Analysis and Verification using an AP210 Standards-based Engineering Framework and Shadow Moiré** ***D. Zwemer[1], S. McCarron[1], A. Spradling[1],R. Peak[2], M. Bajaj[2],T. Thurman[3], M. Dickerson[4], L. Klein[5], G. Liutkis[5],K. Brady[6], J. Messina[6]*** *[1)] AkroMetrix LLC, USA* *[2)] Georgia Institute of Technology, USA* *[3)] Rockwell Collins, USA* *[4)] InterCAX LLC, USA* *[5)] LKSoft, USA* *[6)] NIST, USA*
17.20	**20**	**Novel Numerical and Experimental Analysis of Dynamic Responses under Board Level Drop Test** ***Tong Yan Tee [a], Jing-en Luan [a], Eric Pek [b], Chwee Teck Lim [b], Zhaowei Zhong [c]*** *[a] STMicroelectronics, Singapore* *[b] National University of Singapore, ME Dept, Singapore.* *[c] Nanyang Technological University, School of MPE, Singapore.*
17.40	**20**	**Finite Element Modelling of Crack Detection Tests** ***S Ridout[1] , M Dusek[2] , C Bailey[1], C Hunt[2]*** *[1)] Centre for Numerical Modelling and Process Analysis, University of Greenwich, Greenwich, UK* *[2)] NPL Materials Centre, National Physical Laboratory,, Teddington, UK*

Session 7:		**Modeling and Designing of Advanced Packaging**
16.30	**30**	**Keynote: Design, Fabrication and Comparison of Lead-Free/Eutectic Solder Joint Reliability of FlipChip Package** ***Chih-Tang Peng, Kuo-Ning Chiang, Terry Ku, Kenny Chang*** *National Tsing Hua University, Taiwan*
17.00	**20**	**Virtual Qualification of Moisture Induced Failures of Advanced Packages** ***M.A.J. van Gils[1], W.D. van Driel[2], G.Q. Zhang[3], H.J.L. Bressers[2], R.B.R. van Silfhout[1], X.J. Fan[4], J.H.J. Janssen[2]*** *[1)] Philips Center for Industrial Technology, Eindhoven, The Netherlands* *[2)] ATO Innovation/Philips Semiconductors, Nijmegen, The Netherlands* *[3)] Technical University of Eindhoven, Eindhoven, The Netherlands* *[4)] Philips Research-USA, Briarcliff Manor, New York, USA*
17.20	**20**	**Finite Element Analysis of an Improved Wafer Level Package using Silicone Under Bump (SUB) Layers** ***M. Gonzalez[1], M. Vanden Bulcke[1], B. Vandevelde[1], E. Beyne[1], Y. Lee[2], B. Harkness[2], H. Meynen[2]*** *[1]IMEC, Leuven, Belgium* *[2]Dow Corning Corporation*
17.40	**20**	**Crack and Delamination Risk Evaluation of Thin Silicon Applications based on Fracture Mechanics Approaches** ***J. Auersperg [1,2], D. Vogel[1], B. Michel[1]*** *[1)] Fraunhofer Institute for Reliability and Microintegration Berlin (IZM), Dept. Mechanical Reliability and Micro Materials, Berlin, Germany* *[2)] AMIC Angewandte Micro-Messtechnik GmbH, Berlin, Germany*

Session 8:		**Thermal Behavior Modeling and Characterization**
16.30	**30**	**Keynote: Numerical Simulation and Experimental Verification of the Thermal Contact Properties of the Polymers Bonds** ***T. Falat, A. Wymyslowski, K. Friedel, J.Felba*** *Wroclaw University of Technology, Poland*
17.00	**20**	**Experiments on Behaviour of Power Silicon PN Junctions under Reverse Bias Voltage at High Temperature** ***V.V.N. Obreja[1], C. Codreanu[1], K. Nuttall[2], O. Buiu[2]*** *[1)] National R&D Institute for Microtechnology, Romania* *[2)] Liverpool University, UK*
17.20	**20**	**Parameter Calibration on Post-ion-implantation Dopant Diffusions** ***J. Fu , W.Crans[2], W.J. Eijsenga[2]*** *[1)] X-FAB Semiconductor Foundries, Erfurt, Germany* *[2)] TU Delft, ITS-Faculty/DIMES, Electronic Components, Technology and Materials (ECTM)-Lab, Delft, The Netherlands*

18.00		**End of 1st day Technical Sessions**

Tuesday

8.30		**Start Tuesday Morning Sessions**

	Parallel sessions		
8.30-10.20	**Session 9**		**Session 10**
	Advanced Numerical Simulation Methodologies		**Small Scale Thermal and Fluid Aspects in Microsystems**

Session 9:		**Advanced Numerical Simulation Methodologies**
8.30	**30**	**Keynote: Automated FEM Mesh Optimization for Nonlinear Problems Based on Error Estimation** ***S. Rzepka*** *Infineon Technologies SC 300 Dresden, MDC RM, Dresden, Germany*
9.00	**20**	**Advanced Numerical Prototyping Methods in Modern Engineering Applications** ***W.D. van Driel[1], J. van de Peer[3], N. Tzannetakis[3], A. Wymyslowski[4], G.Q. Zhang[2]*** *[1)] ATO Innovation/Philips Semiconductors, Nijmegen, The Netherlands* *[2)] Center for Industrial Technology/Philips, Eindhoven, The Netherlands* *[3)] Noesis, Leuven, Belgium* *[4)] Wroclaw University of Technology, Wroclaw, Poland*
9.20	**20**	**Reliability-Based Design Optimization for Land Grid Array Solder Joints Under Thermo-Mechanical Load** ***Zhenxue Han[1], Bo Wang[1], Leon Xu[2], Tommi Reinikainen[2],Ren Wei[2]*** *[1)] University of Texas at Arlington, USA* *[2)] Nokia, USA*
9.40	**20**	**Finite Element Analysis of Ultra Thin BGA Package: First and Second Level Reliability** ***P. Limaye[1], B. Vandevelde[1], H. deVries[2], D. Degryse[1], K. Slob[2], C. van Veen[2], R. Labie[1]*** *[1)] IMEC, Leuven, Belgium* *[2)] Philips CFT (Eindhoven), The Netherlands*
10.00	**20**	**Application of Simulation-based Decision Making in Product Development of an RF Module** ***M. Lindgren[1,2], I. Belov[2], M. Törnvall[1], P. Leisner[2,3],*** *[1)] Kitron Development AB, Jönköping, Sweden* *[2)] School of Engineering, Jönköping university, Sweden* *[3)] Acreo AB, Jönköping, Sweden*

Session 10:		**Small Scale Thermal and Fluid Aspects in Microsystems**
8.30	**30**	**Keynote: Data on the Velocity Slip and Temperature Jump Coefficients** *F. Sharipov* *Universidade Federal do Paran´a, Brazil*
9.00	**20**	**Shear Driven Micro-Flows of Gaseous Mixtures** *D. Valougeorgis, S. Naris* *University of Thessaly, Greece*
9.20	**20**	**Effect of Slip on Transient Liquid Flow Development in Micro-Channels** *M.N. Sabry[1], A.R. Abdel-Rahim[2], M.H. Mansour[2]* *[1]) Université Française d'Egypte, Egypt* *[2]) Mansoura University, Egypt*
9.40	**20**	**Model Order Reduction of 3D Electro-Thermal Model for a Novel Micromachined Hotplate Gas Sensor** ***T. Bechtold[1], J. Hildenbrand[1], J. G. Korvink[1], J. Wollenstein[2]*** *[1)] IMTEK, University of Freiburg, Germany* *[2)] Institute for Physical Measurement Techniques, Germany*
10.00	**20**	**Non-contact Thermal Conductivity Measurements of P-doped and N-doped Gold Covered Natural and Isotopically-Pure Silicon and their Oxides** *M. G. Burzo, P. L. Komarov, P. E. Raad* *Southern Methodist University, Dallas*

10.20	**20**	**Break**

	Parallel poster sessions				
10.40-11.30	**Session 11**		**Session 12**		**Session 13**
	Modeling in Micro Technology		**Designing for Reliability**		**Material Characterization and Modeling**

Session 11:		**Poster session: Modeling in Micro Technology**
10.40	**50**	**Design and analysis of novel glass WLCSP structure** ***Chang-Ann Yuan , Cheng Nan Han, Kou-Ning Chiang*** *Department of Power Mechanical Engineering, National Tsing Hua University, HsinChu, Taiwan*
		State of the Art in Prediction of Mechanical Behaviour of Microsystems ***M. Lishchynska, N. Cordero, O. Slattery*** *NMRC, Lee Maltings, Prospect Row, Cork, Ireland*
		Behavioral VHDL-AMS Modeling of Nuclear Magnetic Resonance Sensor ***S. Megherbi[1], J.-C. Ginefri[2], L. Darrasse[2], G. Raynaud[1], J.-F. Pône[1]*** *[1)] Institut d'Electronique Fondamentale, France* *[2)] Unité de Recherche en Résonance Magnétique Médicale, University of Paris-Sud, france*
		3D-FEM Modelling of an Electro-Optical Micro-Shutter ***P. Roux[1], E. Woirgard[1], M. Pizzi[2]*** *[1)]IXL Laboratory, University of Bordeaux, Talence, France* *[2)]Centro Ricerche Fiat (CRF), Orbassano, Italia*
		Novel 2D Micronib Ionization Sources for Nano Electrospray-Mass Spectrometry (ESI-MS) ***S. Le Gac,[1] S. Arscott[1,2], C. Rolando[1]*** *[1)] USTL, UPRESA CNRS 8009, Villeneuve d'Ascq Cedex, France* *[2)] IEMN, UMR CNRS 8520, Villeneuve d'Ascq Cedex, France.*

Session 12:		**Poster session: Designing for Reliability**
10.40	**50**	**A Study of Cyclic Bending Reliability of Bare-die-type Chip-scale Packages** ***Yi-Shao Lai1, Tong Hong Wang, Han-Hui Tsai, Jenq-Dah Wu*** *Stress Characterization Laboratory, Advanced Semiconductor Engineering, Inc., Nantze, Kaohsiung, Taiwan*
		Three-Dimensional Stress Analysis of Ink Marking Process ***Chang-Lin Yeh1, Yi-Hsien Lin, Yi-Shao Lai, Hsiao-Chuang Chang, Jenq-Dah Wu*** *Advanced Semiconductor Engineering, Inc., Nantze, Kaohsiung, Taiwan*
		Microprocessor Packaging Strategy: Reliability of various Flip Chip BGA Packages on different Printed Circuit Boards *A. Guilhaume[1], C. Munier[1], C. Allégret[2], M. Michaud[2]* *[1)] EADS CCR, Service DCR/EP/EO, SURESNES Cedex, France* *[2)] MBDA, Vélizy Villacoublay, France*
		Mechanism-Based Delamination Prediction During Reflow with Moisture Preconditioning ***X.J. Fan[4], L.J. Ernst[1], G.Q.Zhang[2], W. van Driel[3]*** *[1)]Delft University of Technology, Delft, The Netherlands* *[2)]Philips Cft, Eindhoven* *[3)]ATO Innovation/Philips Semiconductors, Nijmegen, The Netherlands* *[4)]Philips Research USA, New York, USA*
		Microstructural Stability and Failure Modes in Eutectic Sn-Ag-Cu Solder ***M. A. Matin, W. P. Vellinga, and M. G. D. Geers*** *Division of Materials Technology, Department of Mechanical Engineering, Eindhoven University of Technology, Eindhoven, The Netherlands*
		Analysis of Thermal-Moisture Induced Failure of Pb-free Soldered IC Packages in SMT Reflow Soldering Process ***Ning Sun[1], Dachuan Lin[1], Daoguo Yang[1,2]*** *[1)] Guilin University of Electronic Technology, Guilin, China* *[2)] Delft University of Technology, The Netherlands*

Session 13:		**Poster session: Material Characterization and Modeling**
10.40	**50**	**Rupture Test on Polysilicon Films Through Electrostatic Actuation** ***F. Cacchione[1], B. De Masi[2], A. Corigliano[1], M. Ferrera[2]*** *[1)] Department of Structural Engineering. Politecnico di Milano, Milano, Italy* *[2)] MEMS Business Unit. STMicroelectronics, Cornaredo, (Milano), Italy*
		Evaluation of the Primary and Secondary Creep of SnPb Solder Joint Using a Modified Grooved-lap Test Specimen. ***S. Déplanque[1], W. Nüchter[1], B. Wunderle[2], H. Walter[2], B. Michel[2]*** *[1)] Robert BOSCH GmbH, Stuttgart, Germany* *[2)] IZM Fraunhofer Institut Zuverlässigkeit und Mikrointegration, Berlin, Germany*
		Numerical Simulation and Experimental Verification of the Piezoresistivity Phenomenon for the Printed Thick-Film Piezoresitors ***A. Wymyslowski[1], M. Santo – Zarnik[2,3], K. Friedel[1], D. Belavic[2,3]*** *[1)] Wroclaw University of Technology, Wroclaw, Poland* *[2)] Jožef Stefan Institute, Ljubljana, Slovenia* *[3)] HIPOT-R&D, Šentjernej, Slovenia*
		Void Formation in a Copper-Via-Structure Depending on the Stress Free Temperature and Metallization Geometry ***K. Weide[1], D. Dalleau[1], Y. Danto[2], H. Fremont[2]*** *[1)] Laboratorium für Informationstechnologie, University of Hannover,, Germany* *[2)] IXL, Universite Bordeaux I, Talence, France*
		Mechanical Characterisation of SiLK by Nanoindentation and Substrate Curvature Techniques ***V. Gonda[1], K.M.B. Jansen[1], L.J. Ernst[1], Jaap den Toonder [1], G.Q. Zhang[3]*** *[1)] Delft University of Technology, Delft, The Netherlands* *[2)] Philips Research Laboratories, Eindhoven, The Netherlands* *[3)] Center for Industrial Technology/Philips, Eindhoven, The Netherlands*
		Cantilever Microbeams: Modelling of the Dynamical Behaviour and Material Characterization ***R. Yahiaoui, A. Bosseboeuf*** *Institut d'Electronique fondamentale, University of Paris-sud Orsay, Orsay, France*
		A Novel Tool for Cure Dependent Viscoelastic Characterization of Packaging Polymers ***C. van 't Hof[1], L.J. Ernst[1], K.M.B. Jansen[1], D.G. Yang[1], H.J.L. Bressers[2], G.Q. Zhang[3]*** *[1)]Delft University of Technology, Delft, The Netherlands* *[2)]Philips Semiconductors, Nijmegen, The Netherlands* *[3)] Center for Industrial Technology/Philips, Eindhoven, The Netherlands*

	Parallel sessions		
11.30-12.40	**Session 14**		**Session 15**
	Modeling of MEMS and Optical Devices		**Simulation-Based Thermal Design Strategies**

Session 14:		**Modeling of MEMS and Optical Devices**
11.30	**30**	**Keynote: Hardware Description Language Modeling of an Electrostatically Actuated bi-axial Micromirror** ***F. Parrain[1], S. Megherbi[1], G. Raynaud[1], H. Mathias[1], J. Gilles[1], A. Bosseboeuf[1], G. Schröpfer[2], P. Cusin[3], N. Faure[3]*** *[1)] Institute d'Electronic Fondamentale UMR8622 – Université Paris-Sud, Orsay Cedex, France* *[2)] Coventor Sarl, Villebon, France* *[3)] Colibris SA, Neuchâtel, Switserland*
12.00	**20**	**Polymer Waveguide and VCSEL Array Multi-Physics Modelling for OECB Based Optical Backplanes** ***D. Gwyer[1], P. Missebrook[2,3], C. Bailey[1], P.P. Conway[3], K. Williams[3]*** *[1)] Centre for Numerical Modelling and Process Analysis, University of Greenwich, London, UK* *[2)] Celista, Stoke-on-Trent, UK* *[3)] Interconnection Group, Loughborough University, Loughborough, UK*
12.20	**20**	**Determination of Residual Stress in Glass Frit Bonded MEMS by Finite Element Analysis** ***M. Ebert, J. Bagdahn*** *Fraunhofer- Institute for Mechanics of Materials Halle, Germany*

Session 15:		**Simulation-Based Thermal Design Strategies**
11.30	**30**	**Keynote: A Computer-Architecture Approach to Thermal Management in Computer Systems: Opportunities and Challenges** ***K. Skadron, M.R. Stan, W. Huang, Zhijian Lu, K. Sankaranarayanan, J. Lach*** *University of Virginia, USA*
12.00	**20**	**Tri-dimensional reduced-order Thermal Model of Stacked Electronic Structures** ***V. Feuillet[1], V. Gatto[1], Y. Scudeller[2], Y. Jarny[1]*** *1) Laboratoire de Thermocinétique* *2) Laboratoire de Génie des Matériaux* *Ecole polytechnique de l'université de Nantes, Nantes, France*
12.20	**20**	**Thermal Modeling for Power MOSFETs in DC-DC Applications** ***Y. Bulut, K. Pandya*** *Vishay Siliconix, USA*

12.40	**100**	**Lunch**

14.20		**Start Tuesday Afternoon Sessions**

14.20		**Start Tuesday Afternoon Sessions**

	Parallel sessions		
14.20-16.10	**Session 16**		**Session 17**
	Solder Reliability Behavior		**CFD and FE Modelling of Thermal Performance**

Session 16:		**Solder Reliability Behavior**
14.20	**30**	**Keynote: Reliability of SnPb and Pb-Free Flip-Chips under Different Test Conditions** ***M. Spraul[1], W. Nüchter[1], A. Möller[1], B. Wunderle[2], B. Michel[2]*** *[1)] Robert Bosch GmbH, Germany* *[2)] Fraunhofer-IZM, Berlin, Germany*
14.50	**20**	**Microstructural and Mechanical Characterization of 95.5Sn-4Ag-0.5Cu Solder Balls by Nano-Indentation** ***M. Erinç[1], P. Schreurs[1], G.Q. Zhang[1], W. D. van Driel[2], M. Geers[1]*** *[1)] Technical University of Eindhoven, Eindhoven, The Netherlands* *[2)] ATO Innovation/Philips Semiconductors, 6534 AE Nijmegen, The Netherlands*
15.10	**20**	**Modeling Stress Strain Curves For Lead Free 95.5Sn-3.8Ag-0.7Cu Solder** ***J.H.L. Pang, B.S. Xiong and T.H. Low*** *Nanyang Technological University, School of Mechanical and Production Engineering, Singapore*
15.30	**20**	**Effect of Different Temperature Cycle Profiles on the Crack Propagation and Microstructural Evolution of Real Lead Free Joints of Different Electronic Components** ***C. Andersson[1,2], D. Andersson[1,3], P-E Tegehall[1,3], Johan Liu[1,2,3]*** *[1)] Swedish Microsystem Integration Technology (SMIT) Center* *[2)] Division of Electronics Production, Chalmers University of Technology, Mölndal, Sweden* *[3)] IVF Industrial Research and Development Corporation, Sweden*
15.50	**20**	**A Review of Creep Fatigue Failure Models in Solder Material - Simplified Use of a Continuous Damage Mechanical Approach** ***G. Massiot, C. Munier*** *EADS Corporate Research Center, Suresnes cedex, France*

Session 17:		**CFD and FE Modeling of Thermal Performance**
14.20	**30**	**Keynote: Thermal and Flow Analysis of SiC-Based Gas Sensors for Automotive Applications** *I. Below[1], P. Leisner[1], H. Wingbran[2], A.L. Spetz[2], H. Sundgren[2], B. Thuner[2], H. Svenningstorp[3], P. Leisner[4]* *[1)] Jönköping University, Sweden* *[2)] Linköping University, Sweden* *[3)] Volvo Technology Corporation, Sweden* *[4)] Acreo, Sweden*
14.50	**20**	**Low Reynolds Number Turbulence Models for Accurate Thermal Simulations of Electronic Components** *K Dhinsa, C Bailey, K Pericleous* *University of Greenwich, UK*
15.10	**20**	**Thermal Testing of a 3-Die Stacked Chip Scale Package Including Evaluation of Simplified and Complex Package Geometry Finite Element Models** *B.A. Zahn* *ChipPAC, USA*
15.30	**20**	**Thermal Analysis of QFN Packages Using Finite Element Method** ***C.L. Chang, Y.Y. Hsieh*** *National Yunlin University of Science and Technology, Taiwan*
15.50	**20**	**Experimental Study on Visualization of a Longitudinal Heat Sink with Top-mounted Fan by Particle Tracking** *J.H. Jang* *Kuang-Wu Institute of Technology, Taiwan*

16.10	**20**	**Break**

		Special Exhibitor session
16.30		

18.00		**End of 2nd day Technical Sessions**

Wednesday

8.30		**Start Wednesday Morning Sessions**

Session 18:		**Keynote session: Micro- to Macro-Scale Thermal Design Challenges in Microelectronics**
8.30	**30**	**Keynote: Modeling Heat Transfer and Liquid Flow in Micro-Channels** ***M.N. Sabry[1]***, *B.O. Djebedjian[2], S.H. Saleh[2], M.M. Mahgoub[2]* *[1]) Université Francaise d'Egypte, Egypt* *[2]) Mansoura University, Egypt*
9.00	**30**	**Keynote: Cooling Problems and Thermal Issues in High Power Electronics: a Multi-Faceted Design Approach** ***M. Behnia[1]***, *L. Maguire[2]* ,***G. Morrison[2]*** *[1]) The University of Sidney, Australia* *[2]) University of New South Wales, Australia*
9.30	**30**	**Keynote: Design Challenges for High-Performance Heat Sinks used in Microelectronic Equipment: Evolution and Future Requirements** ***P. Rodgers[1], V. Eveloy[2]*** *[1]) CALCE Electronic Products and Systems Center, University of Maryland, USA* *[2]) Electronics Thermal Management, Ltd., Ireland*

10.00	**40**	**Break**

	Parallel sessions		
10.40-12.30	**Session 19**		**Session 20**
	Solder Fatigue		**Characterization and Modeling of Polymer behavior**

Session 19:		**Solder Fatigue**
10.40	**30**	**Keynote: A Mechanics-Based Strain Gage Methodology for Direct Solder Joint Reliability Assessment** ***L.L. Mercado, S. Girouard, G. Hsieh*** *Intel, Chandler, USA*
11.10	**20**	**Microstructural Behaviour of Solder Alloys** ***R.L.J.M. Ubachs, P.J.G. Schreurs, M.G.D. Geers*** *Eindhoven University of Technology, Departement of Materials Technology, Eindhoven, The Netherlands.*
11.30	**20**	**Flip Chip Solder Joint Fatigue Analysis Using 2D and 3D FE Models** ***A. Yeo[1], C. Lee[1], J. H.L. Pang[2]*** *[1)] Infineon Technologies Asia Pacific Pte Ltd, Assembly & Interconnect Technology, Singapore* *[2)] *School of Mechanical and Production Engineering, Nanyang Technological University, Singapore*
11.50	**20**	**Thermal Fatigue Modelling for SnAgCu and SnPb Solder Joints** ***R. Dudek, H. Walter, R. Doering, B. Michel*** *Fraunhofer IZM, Berlin, Germany*
12.10	**20**	**Thermal Cycling Reliability of SnAgCu and SnPb Solder Joints: A Comparison for Several IC-Packages** ***B. Vandevelde, M. Gonzalez, P. Limaye, P. Ratchev, E. Beyne*** *IMEC, Leuven, Belgium*

Session 20:		Characterization and Modeling of Polymer behavior
10.40	**30**	**Keynote: Molecular Modeling Studies of IC Barrier Concerns.** ***N. Iwamoto,*** *Honeywell Specialty Materials, Morristown, USA*
11.10	**20**	**Molecular Simulation of Cu-SAM Adhesion Force** ***H. Fan, C.K. Wong, M.M.F. Yuen*** *Department of Mechanical Engineering, Hong Kong University of Science and Technology, Kowloon, Hong Kong*
11.30	**20**	**Cure, Temperature and Time dependent Constitutive Modeling of Moulding Compounds** ***K.M.B. Jansen[1], L. Wang[1], D.G. Yang[1], C. van 't Hof[1], L.J. Ernst[1], H.J.L. Bressers[2], G.Q. Zhang[3]*** *[1)]Delft University of Technology, Delft, The Netherlands* *[2)]Philips Semiconductors, Nijmegen, The Netherlands* *[3)]Philips CFT, Eindhoven, The Netherlands*
11.50	**20**	**Simulation of No-Flow Underfill Process for Flip-Chip Assembly** ***A. Kolbeck[1], T. Hauck[1], J. Jendrny[2], O. Hahn[2], S. Lang[3]*** *[1)] Motorola GmbH, Deutschland* *[2)] LWF, Universität Paderborn, Deutschland* *[3)] CADFEM Gmbh, Grafing, Germany*
12.10	**20**	**Mechanical Properties of Molding Compounds (MCs) under Different Moisture Conditions and in a Wide Temperature Range** ***W.H. Zhu, S. L. Gan, C.L. Toh*** *Assembly and Interconnect Technologies, Infineon Technologies Asia Pacific Pte Ltd, Singapore*

12.30	**90**	**Lunch**

14.00		**Start Wednesday Afternoon Sessions**

Session 21:		Keynote session: New Developments in Microelectronics Reliability
14.00	**30**	**Keynote: Challenges of Thermomechanical Design and Modeling of Ultra Fine-Pitch Wafer Level Packages** ***A. A. O. Tay*** *Department of Mechanical Engineering, Nano/Microsystems Integration Laboratory, National University of Singapore, Singapore*
14.30	**30**	**Keynote: Topography and Deformation Measurement under Thermomechanical Stress** ***R. Fayolle, J. Lecomte*** *Insidix, Seyssins, France*
15.00	**30**	**Keynote: Reliability of Interfaces for Lead-Free Solder Bumps** ***R.L.H. Shih[1], D.Y.K. Lau[2], R.W.M. Kwok[2*], M. Li[3], M.K.W. Sun[4]*** *[1)] Department of Chemistry, The Chinese University of Hong Kong, Shatin, N.T., Hong Kong* *[2)] Rohm and Haas Electronic Materials Asia Limited, 15 On Lok Mun Street, Fanling, N.T., Hong Kong* *[3)] Department of Electronic Engineering, The Chinese University of Hong Kong, Shatin, N.T., Hong Kong* *[4)] Department of Physics, The Chinese University of Hong Kong, Shatin, N.T., Hong Kong*
15.30	**30**	**Keynote: From Chemical Building Blocks of Polymers to Microelectronics Reliability** **H.J.L. Bressers[2], W.D. van Driel[3], K.M.B. Jansen[1], L.J. Ernst[1] and G.Q. Zhang[3]** *[1)]Delft University of Technology, Delft, The Netherlands* *[2)]Philips Semiconductors, Nijmegen, The Netherlands* *[3)]Philips CFT, Eindhoven, The Netherlands*

16.00		**End of Conference**