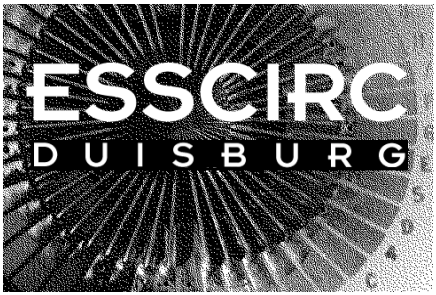

25th European Solid-State Circuits Conference

21 - 23 September 1999
Duisburg, Germany

Organised by:

Fraunhofer Institut
Mikroelektronische
Schaltungen und Systeme

and

Gerhard
Mercator
Universität
Gesamthochschule
Duisburg

with

Technical Co-Sponsorship of the
IEEE Solid-State Circuits Society

Conference Venue

The conference place will be located at the campus of the University of Duisburg, quite close to the Fraunhofer Institute of Microelectronic Circuits and Systems and not far from the centre of the city of Duisburg. It is very easy to reach from the centre by bus and tram and has also a lot of parking facilities for cars.

Address: Gerhard-Mercator-University GH Duisburg
Buildings LA and LB
Lotharstrasse
D-47057 Duisburg

Conference Secretariat

Mrs. Cornelia Metz
Fraunhofer IMS
Finkenstraße 61; D-47057 Duisburg, Germany
Phone: +49-203-37 83-210
Fax: +49-203-37 83-278
E-mail: metz@ims.fhg.de

Registration and Information

The registration desk is located in the Building LA.
During the ESSCIRC the conference desk will be open:

Monday, 20 September :	09:00 – 19:00
Tuesday to Thursday, 21 – 23 September:	8:00 until the end of the conference sessions
Friday, 24 September:	9:00 – 13:00

Sponsors

We gratefully acknowledge financial support from:

Stadtsparkasse Duisburg, ELMOS AG, Wacker Siltronic AG, BMW AG, Nokia, Intel, Infineon Technologies, Techniker Krankenkasse

ESSCIRC on Internet

http://www.esscirc.org

FOREWORD

It is our pleasure to welcome you to the ESSCIRC'99 in Duisburg, Germany. This year it is the 25th anniversary of the ESSCIRC conference series. Thus the conference is still young and reflects the dynamic development of the semiconductor industry. But at the same time it is known enough to attract papers of high excellence. Although European in name, the ESSCIRC is receiving more and more attendance from overseas, particularly from the U.S.A. and Far East and thus represents a truly international forum.

Bringing the ESSCIRC to Duisburg is also reflecting another trend, namely the fact that high tech is finally finding its way into an area formerly associated with steel and coal. Domestic and international companies are establishing their presence in and around Duisburg, many of them in microelectronics and related fields. This befits Duisburg to stage a major conference event in microelectronics.

This year's ESSCIRC features exactly 110 contributions including 8 invited papers. 63 regular papers and 39 posters have been carefully selected by renowned experts out of 195 submitted contributions. In addition, 2 workshops will devoted to up to date topics. Social events complement the technical programme and create the basis for informal meetings where spontaneous exchange of ideas can take place.

We hope that you will enjoy the programme the conference is offering and that this is not the last time you visit Duisburg.

Prof. Dr. rer. nat. G. Zimmer
Conference Chairman

Prof. B.J. Hosticka, Ph.D.
Technical Programme Chairman

VENUE

Duisburg

Duisburg with its interesting contrast between old industrial sites and modern appearance with lots of greens lies in the beautiful Rhine area in western Germany. It is very easy to reach either by car or train as well as by plane via Duesseldorf which is just half an hour away. As a bustling industrial and commercial centre located at the confluence of the Ruhr and Rhine rivers, Duisburg is a city of contrasts: on the one hand it is Europe's biggest iron and steel producer and world's largest river port, and on the other hand it is a city featuring a fine collection of museums, generous green areas dotted with lakes and lively cultural scene. New industries are also emerging, such as microelectronics. The largest of three facilities of the Fraunhofer Institute of Microelectronic Circuits and Systems is located in Duisburg. Duisburg also boasts a university named after the famous cartographer Gerhard Mercator who lived here more than 40 years.

The university campus can be reached by bus in less than ten minutes from the centre of the city of Duisburg where both, the Main Railway Station and most of the hotels are located. In the city you will also find a wide range of shops, exquisite restaurants, a beautiful theatre as well as the famous musical "Les Miserables", and, of course, enough possibilities to enjoy nightlife.

The conference reception given by the mayor of Duisburg will be held at the GTT Microelectronic Centrum, also close to the university and the Institute. The conference banquet is planned to take place in a unique leisure park in the northern part of Duisburg: this is an old industrial site that was closed down some time ago and converted into a facility offering leisure and relaxation. Here plants and wildlife mingle with decommissioned iron blast furnaces and power plants. One can walk or cycle around or watch theatre, dancing, or just listen to live music.

Course	
Monday	
09:00	Registration
10:45	M. Engels
11:30	Break
11:45	Presentation continued
12:30	Lunch
14:00	R. van de Plassche
14:45	Break
15:00	Presentation continued
16:00	A. Abidi
16:45	Break
17:00	Presentation continued
17:45	Wrap-up

Conference			
Tuesday			
08:00	Registration		
09:00	Opening		
	Best Paper '98		
09:20	Invited		
10:10	Coffee Break		
10:40	S1.1	S1.4	S1.7
12:20	Lunch		
14:00	Invited		
14:50	S1.2	S1.5	S1.8
15:40	Coffee Break		
16:10	S1.3	S1.6	S1.9
18:00	Reception		

Conference			
Wednesday			
08:30	Invited		
09:20	S2.1	S2.4	S2.7
10:10	Coffee Break		
10:40	Invited		
11:30	S2.2	S2.5	S2.8
12:20	Lunch		
14:00	Invited		
14:50	S2.3	S2.6	S2.9
15:40	Coffee Break		
16:00	Posters		
19:30	Conference Banquet		

Conference			
Thursday			
08:30	Invited		
09:20	ESSCIRC 2000		
09:25	S3.1	S3.4	S3.7
10:15	Coffee Break		
10:45	Invited		
11:35	S3.2	S3.3	S3.4
12:25	Lunch		
14:00	Invited		
14:50	S3.3	S3.6	S3.9
15:40	Young Sc. Award		
	Closing Session		

Workshop	
Friday	
08:30	Registration
09:00	Opening
09:15	S. Rusu
10:00	F.O. Witte
10:45	Coffee Break
11:15	J. v. Lammeren
12:00	Panel Discussion
12:30	End of Workshop

TECHNICAL PROGRAMME

Workshops

Two workshops will be given:

Monday, 20 September 1999

RF-Circuits
Organiser: Ton Wagemans, Philips, Eindhoven, The Netherlands

Friday, 24 September 1999
Integrated Systems
Organiser: H.-L. Fiedler, Fraunhofer IMS, Duisburg, Germany

Conference (Tuesday, Wednesday, Thursday)

Invited: Seven speakers and one keynote speaker have been invited.

Regular: 63 papers will be orally presented.

Posters: 39 posters will be presented on Wednesday afternoon during which time the authors will be present to answer questions. The posters will be displayed throughout the three conference days.

Awards

Best Paper Award '98

The Best Paper Award'98 will be presented by the last year's Programme Chairman, Mr. A. H. M. van Roermund, at the opening of this year's conference.

Best Paper Award '99

The participants will be invited to select the Best Paper from the contributed papers presented this year. The Award will be presented at ESSCIRC'2000.

Best Poster Award '99

The Best Poster Award'99 will be presented during the closing session of the conference.

Poster Session

Poster Session on Wednesday, 22 September 1999, from 16:00 – 18:00.

Visit of Fraunhofer IMS

Fraunhofer IMS offers a lab tour on Thursday, 23 September 1999, at 16:00. Please register at the conference desk. For individual arrangements please contact the conference secretary.

PROCEEDINGS

Conference Proceedings

Each registered participant will receive a copy of the conference proceedings. Additional copies may be purchased during the conference. After the conference, please contact:

Editions Frontières
20, Rue d'Armenonville
F-92200 NEUILLY/SEINE
Phone: +33-1–47 22 59 09
Fax: +33-1–47 47 07 57
E-Mail: frontier@club-internet.fr

Workshops Proceedings

Each registered participant of the workshop will receive a copy of proceedings of the workshop he or she registered for.

Social Programme

Welcome Reception at the Microelectronic Centrum

The reception takes place at the GTT Microelectronic Centrum in Duisburg. In the Centrum a number of start-up companies are located that are involved in microelectronics and related fields. The building has been designed by the famous British architect Sir Norman Foster. The reception is hosted by the mayor of Duisburg.

Conference Banquet

The conference banquet will be held at the Landschaftspark Duisburg-Nord which is an old industrial setting now used for cultural and social events.

Accompanying Persons Programme

Upon request and depending on sufficient number of entries, we will offer a special programme to accompanying persons. Further details can be obtained at the conference desk.

Useful Hints

Banks

The Building LB on the campus of the University has a cash dispenser. In the centre of the city of Duisburg you will find representatives of all major banks.

Shopping

Shops are opened, Monday through Friday, from 10:00 until 20:00.

Tourist Information

You can reach the Tourist Information of City of Duisburg for further information as follows: Phone: +49-203-2 85 44 11
Fax: +49-203-2 85 44 44

Registration and Accommodation Booking

Registration

Registration for the conference and workshops should be made by returning the completed registration form. This form can be found in this programme or can be printed from our Internet site.

The full registration fee includes attendance of the conference (Tuesday, Wednesday, Thursday), lunches, and coffee breaks, the welcome reception at the GTT Microelectronic Centrum, conference proceedings, and the conference banquet.

The student registration fee (only for B.Sc. and M.Sc. students) includes all of the above except the conference proceedings and the conference dinner. It is possible to register for conference banquet separately.

No registration will be confirmed until full payment has been received by the Conference Secretariat. Substitutions can be accepted at any time before the start of the conference. Payments should be made in advance. Payment for early registration should be received not later than **10 August 1999**.

Accommodation

The participants of the ESSCIRC'99 have to book their accommodation directly with the hotel. Hotels listed below are located in the city centre. A sufficient number of rooms have been reserved for those participants who register early.

Category 1

STEIGENBERGER DUISBURGER HOF
Neckarstraße 2, D-47051 Duisburg
Phone: +49-203-3 00 70
Fax: +49-203-3 00 7-400
Single room - DEM 165,-

PLAZA
Düsseldorfer Straße 54, D-47051 Duisburg
Phone: +49-203-2 82 20
Fax: +49-203-2 82 23 00
Single room – DEM 169,-

REGENT
Dellplatz 1, D-47051 Duisburg
Phone: +49-203-29 59 00
Fax: +49-203-2 22 88
Single room - DEM 149,-

Category 2

NOVOTEL
Landfermannstraße 20, D-47051 Duisburg
Phone: +49-203-30 00 30
Fax: +49-203-30 00 35 55
Single room - DEM 125,-

IBIS
Mercatorstraße 15, D-47051 Duisburg
Phone: + 49-203-30 00 50
Fax: + 49-203-34 00 88
Single room - DEM 124,-

HAUS FRIEDRICHS
Neudorfer Straße 35, D-47051 Duisburg
Phone: +49-203-35 57 37
Fax: +49-203-35 20 57
Single room - DEM 100,-

Category 3

ETAP
Falkstraße 61, D-47058 Duisburg
Phone: +49/203/3 01 99 20
no fax no. available
Single room - DM 80,-

RHEINISCHER HOF
Mülheimer Straße 119, D-47057 Duisburg
Phone: +49/203/33 24 46
Fax: +49/203/34 01 24
Single room – DEM 80,-

If you have any further questions concerning the accommodation (e.g. double occupancy rates etc.) please contact the hotel. More hotel addresses can be provided upon request by the Tourist Information of City of Duisburg: phone: +49-203-2 85 44 11, fax: +49-203-2 85 44 44

Payment

Pre-Payment of the conference fees may be made by credit card (Visa, Eurocard, or American Express) or by bank transfer. On-site payment may be made by credit card, Eurocheque or cash.

Payment should be accompanied by the paper registration form (either fax or by mail).

Bank Connection

Deutsche Bank München

Account No. 75-21933

Bank Code No. 70070010

Reference: ESSCIRC'99, No. 900060

Cancellation

All request refunds must be submitted in writing to the conference secretary before 29 August 1999. The registration fee minus 10% processing charge will be refunded.

Liability

The conference organisation accepts no responsibility for accidents to conference delegates or for damage to, or loss of their personal property during the conference.

INVITED PAPERS

Digital Processing – Future aspects of the semiconductor business
Soenke Mehrgardt, Infineon Technologies AG, Munich, Germany

Looking at the landscape of processor architectures and system solutions that have come up during the past, various architectural concepts were introduced to meet the requirements of complex future applications. The question is how an architecture fits optimally to a specific application in terms of efficiency and system cost.

The answer is to give programmers a general architecture together with the opportunity to optimize and configure processor instructions on their own in order to reach the different application targets. Additionally today's market requires System-on-a-chip solutions with flexible configuration and integration of cores, memories, and peripherals, also adding application specific designs and customer IP under a common strategy. This second level of a platform approach will only be possible if it is based on a flexible HW/SW co-design.

VLSI Memory Technology: Current Status and Future Trends
Kiyoo Itoh, Hitachi Ltd. Tokyo, Japan

In this presentation, first, newly developed state-of-the-art VLSI memory chips, exemplified by DRAM, SRAM, and Flash memory, are discussed. Second, technology trends concerning standard DRAM's, embedded memories, and low-voltage memories are reviewed. For standard DRAM's, memory cells with high cell capacitance, high-speed subsystem technologies (such as synchronous operations pipelining/prefetching, and use of packet protocols), and small-swing interfaces are investigated. And regarding embedded-memories, the advantages and the challenges involved in reducing process costs are presented. Moreover, the use of special circuits to reduce subthreshold current in low-voltage memories is summarized, citing examples of recent advancements.

Finally, it is emphasized that a unified memory cell ,such as a gain cell (which includes all the advantages of the existing memory cells) must be developed in the near future.

Highly integrated RF-ICs for GSM, DECT and UMTS Systems. A Status Review and Development Trends
Josef Fenk, Infineon Technologies, Munich, Germany

TDMA based digital systems like GSM for cellular and DECT for cordless application have created since 1992 an increasing market within Europe and gained widespread acceptance also outside Europe. In the meantime the cellular based GSM network is coming already in some megalopolis to it's limits. The WCDMA based UMTS system will in future increase reasonably the available bandwidth and enable throughputs for data services up to 2.048 MBit. This presentation gives an overview of these systems. The system requirements and their influences on highly integrated RF ICs for GSM, DECT and UMTS are discussed. The various trends of progresses in integration will be shown, with the different advantages and disadvantages of the concepts in use. The challenges of increasing the level of integration and an outlook of the future will be presented.

The rapid increase in the capacity of the optical fiber
Lars Thylen, University of Stockholm, Sweden

The rapid increase in the demonstrated capacity of the optical fiber, with aggregate bitrates well in excess of 1 Tb/s, and the equally rapid development in high speed electronics raise the question how the two technologies can be best combined. In principle the statement that "optics is good for transmission and electronics for information processing " in essence holds true, partly for basic physical reasons. The consequence has been that electronics has been used for regenerators, multiplexers etc in fiberoptics systems, the all optical alternatives by and large so far being noncompetitive or nonexistent. Over the recent years, however, several groups have reported all optical systems with the mentioned functions operating at speeds up to several 100 Gb/s. One interesting question is, given a certain complexity of a circuit, when the optical implementation will be superior in speed, as the nonlinearities in certain photonic devices have response times well below 1 ps. Another question is in which applications such speeds could be utilized. Still another question pertains to basic characteristics such as switch power of electronic and optoelectronic gates. The talk will address the challenges to electronics brought about by the development in fiber optics.

High Speed Electronics Interfacing Fibre Networks.
Christer Svensson, Linköping University, Sweden

The high data rates facilitated by photonic networks call for 10-100 Gb/s electronic interfaces, protocol processing and switching. Two needs are identified, high absolute speed and high throughput. The basic speed limitations of transistors in different techniques, wires and circuits are discussed. Several examples of the implementation of key functions demanding high absolute speed, using bipolar techniques, and high throughput, using CMOS techniques, respectively, are demonstrated. Examples of real implementations are shown. Finally, future prospects are discussed.

Automotive Semiconductor Technologies for the New Millennium
Bruno Murari, STMicroelectronics, Italy

Over the next few years the electronic content of the automobile will expand dramatically, driven by the need to enhance safety, increase energy efficiency and make the experience of road travel more enjoyable for both drivers and passengers. New safety features like anti-collision radar and night vision devices will emerge from the laboratory while existing safety systems such as airbags will become more effective through the use of more sophisticated electronic controls. Electric power steering and electric engine valve subsystems will help reduce the overall energy consumption to meet the demanding goals of new regulations. Multimedia systems will bring back seat passengers DVD movie players and videogames, while in the front seat new convergence products will unite navigation, information and communications functions. To make all of these applications cost effective semiconductor suppliers will need to deliver advanced solutions using very competitive technologies that are sufficiently robust to survive in the hostile automotive environment. New power ICs with embedded processors will be needed in body applications like doorlocks, mirror controls and seat motors, complex system-on-chip devices will be required for engine controls and multimedia bus nodes, high voltage chips will be needed for new technology lamps and low-cost micromachined silicon sensors will be needed in applications like airbag and navigation systems, radio frequency IC technology will be needed in both communication and navigation sytems.

CMOS or CCD image sensors for digital still applications?
Albert J.P. Theuwissen, Philips Imaging Technology, Eindhoven, The Netherlands

In this paper an in-depth comparison will be made between the good old Charge-Coupled Devices and the challenging CMOS image sensors as far as the digital still applications are considered. CMOS image sensors have the advantage of being cheaper, consuming less power and containing more electronics on-chip than the CCDs. On the other hand CCDs show superior image quality. What are the trade-offs between both technologies and are there other shortcomings when the devices are applied into a digital still application?

Sensor Systems – Interface between Environment and Application
D. Hammerschmidt, Fraunhofer Institut für mikroelektronische Schaltungen und Systeme, Duisburg, Germany

The rapidly growing market for sensor systems on the one hand boosts the development of new sensor principles and technologies, on the other hand the increasing fields of use require an integration of these sensors on system level under a wide spread of application conditions. This paper will discuss the main tasks that have to be solved by the electronic system, which interfaces the sensor and the application environment. On side of the sensor physical points of view dominate the requirements, which, e.g., call for low noise readout, high gain, minimum sensor loading and compensation of cross-sensitivities. The application requires completely different considerations, like compatibility with former solutions, standardized interfaces, low power consumption or networking capability as well as cost efficiency. Between these completely different classes of requirements electronic circuitry operates as a mediator featuring sophisticated readout electronics for each type of sensor, intermediate signal-processing layers and customizable interfaces that are usable for all kinds of sensors. After the general consideration of the above topics some examples of sensor systems will be presented discussing the individual solutions of the mentioned challenge from the circuit designers point of view. At last some approaches for future developments of sensor systems will be presented.

Monday, 20.09.99

Software mobile radio design, from antenna to baseband

Organiser: Ton Wagemans
Philips, Eindhoven, The Netherlands

Standards for mobile telecommunications have proliferated across the globe since the beginning of the nineties. IS95, IS136, GSM and PCS for example, are commonplace but only applicable for well-defined geographical regions. In addition, RF frequency bands for said systems often do not overlap due to legislative issues. To compound matters cordless telephony standards such as DECT, CT2 and PHS are different yet again. So a mobile user will end up needing to carry a number of telephones to guarantee seamless roaming from his home to somewhere abroad.
A solution is to unify all standards into a single world-wide accepted standard, but this is challenging to say the least. As a first step industry is reacting to the problem by offering dedicated dual or triple mode terminals.
A software mobile radio is a communications terminal which can be programmed to comply to any of today's standards. In this workshop circuits and architectures which can be used towards building such a terminal will be treated in detail by leading experts in the field.
There are three main areas which will be addressed separately: The radio frontend: Adaptive multi-mode radio RF transceivers Interface analogue/digital domain: specifications for data converters and their position in the conversion chain Reconfigurable software: implementation strategies of the baseband part.

Lecturers and affiliation:

Is software optimal for software mobile radio?
Dr. Marc Engels
IMEC DESICS, Leuven, Belgium

Wide-band and band-pass data converters for telecom applications
Dr. Rudy van de Plassche
Broadcom Netherlands B.V., Bunnik, The Netherlands

RF and IF CMOS Circuits for Multi-mode Radios
Professor Asad A. Abidi
Electrical Engineering Department, University of California, Los Angeles, CA, USA

Schedule

09:00 – 19:00	Registration
10:45 - 11:30	Is software optimal for software mobile radio?
11:30 - 11:45	Break
11:45 - 12:30	First presentation continued
12:30 - 14:00	Lunch
14:00 - 14:45	Wide-band and band-pass data converters for telecom applications
14:45 - 15:00	Break
15:00 - 15:45	Second presentation continued
16:00 - 16:45	RF and IF CMOS Circuits for Multi-mode Radios
16:45 - 17:00	Break
17:00 - 17:45	Third presentation continued
17:45 - 18:00	Wrap-up

Tuesday, 21.09.99 Audimax (Building LA)

08:00 to 09:00 Registration
09:00 to 09:15 Opening
09:15 to 09:20 ESSCIRC 98 Best Paper Award

09:20 Keynote Invited Paper
Digital Processing - Future aspects of the semiconductor business
S. Mehrgardt, Infineon Technologies AG, Munich, Germany

10:10 to 10:40 Coffee Break

Session 1.1: Filters
Chairman: W. Brockherde
Fraunhofer IMS, Duisburg, Germany

10:40 A 40µw, 75dB Dynamic Range, 70kHz Bandwidth Biquad Filter based on Complementary MOS Transconductors
D.G. Python[1], C.C. Enz[2]
[1]Swiss Federal Institute of Technology, Lausanne, Switzerland
[2]Centre Suisse d`Electronique et de Microtechnique, Neuchâtel, Switzerland

11:05 A 100MHz Partial Analog Adaptive Equalizer for use in Wired Data Transmission
J. Cheng, D.A. Johns
University of Toronto, Canada

11:30 A 60-350 MHz Programmable Analog Filter in a Digital CMOS Process
S. Pavan[1], Y. Tsividis[2], K. Nagaraj[1]
[1]Texas Instruments, Warren, NJ, USA
[2]Columbia University, New York, NY, USA

11:55 An Eighth-Order Lowpass Filter with 5-100 MHz Tuning Range and Programmable Boost
G. Bollati[1], R. Alini[1], R. Castello[2], M. Demicheli[1], S. Portaluri[1]
[1]STMicroelectronics, Cornaredo, Milan, Italy
[2]University of Pavia, Italy

12:20 to 14:00 Lunch Break

Tuesday, 21.09.99 Audimax (Building LA)

14:00 Invited Paper
VLSI Memory Technology: Current Status and Future Trends
K. Itoh, S. Kimura, T. Sakata, Hitachi Ltd., Tokyo, Japan

Session 1.2: Amplifiers 1
Chairman: B. Nauta
University of Twente, Enschede, The Netherlands

14:50 A Chopper Modulated Instrumentation Amplifier with First Order Low-pass Filter and Delayed Modulation Scheme
C. Menolfi, Q. Huang
Swiss Federal Institute of Technology, Zurich, Switzerland

15:15 Integrated Lock-In Amplifier for Sensor Applications
A. Gnudi, L. Colalongo, G. Baccarani
Università di Bologna, Italy

15:40 to 16:10 Coffee Break

Session 1.3: Amplifiers 2
Chairman: B. Nauta
University of Twente, Enschede, The Netherlands

16:10 A 500MHz Write Amplifier for Hard Disk Drives with Low Output Impedance
L. Le[1], E. Pieraerts[1], F. de Jong[2]
[1]Philips Composants et Semiconducteurs, Caen, France
[2]Philips Research Laboratories, Eindhoven, The Netherlands

16:35 A High Speed Low Noise CMOS MR Preamplifier for Disk Drives
J. Kuehlwein[1], R. Harjani[2]
[1]VTC, Inc., Bloomington, MN, USA
[2]University of Minnesota, Minneapolis, MN, USA

17:00 Low-Power BiCMOS Op Amp with Integrated Current Mode Charge Pump
R. St. Pierre
Gain Technology Corporation, Tucson, AZ, USA

18:00 to 20:00 Reception

Tuesday, 21.09.99 HS 104 (Building LB)

Session 1.4: Sigma-Delta Converters
Chairman: B. Redman-White
Philips Semiconductors, Southampton,
United Kingdom

10:40 A 200MHz IF, 11 bit, 4th order Band-Pass Delta-Sigma ADC in SiGe
R. Maurino, P. Mole
Nortel Networks, Essex, United Kingdom

11:05 A 3.3V CMOS 10.7MHz 6th-order bandpass Sigma-Delta modulator with 78dB dynamic range
D. Tonietto[1], P. Cusinato[1], F. Stefani[1], A. Baschirotto[2]
[1]STMicroelectronics, Cornaredo, Milan, Italy
[2]University of Lecce, Italy

11:30 14-bit, 2.2MS/s Sigma Delta ADCs
J. Morizio[1], M. Hoke[1], T. Kocak[1], C. Geddie[1], C. Hughes[1], J. Perry[1], S. Madhavapeddi[1], M. Hood[1], G. Lynch[1], H. Kondoh[2], T. Kumamoto[2], T. Okuda[2], H. Noda[2], M. Ishiwaki[2], T. Miki[2], M. Nakaya[2]
[1]Mitsubishi Electronics America, Durham, NC, USA
[2]Mitsubishi Electric Corporation, Hyogo, Japan

11:55 A 13.5-Bit Cost Optimized Multi-Bit Delta-Sigma ADC for ADSL
A. Wiesbauer, H. Weinberger, M. Clara, J. Hauptmann
Infineon Technologies Austria, Villach, Austria

12:20 to 14:00 Lunch Break

Session 1.5: Smart Power
Chairman: W. Pribyl
Austria Mikrosysteme International AG, Unterpremstätten, Austria

14:50 A Low Power ASIC for the Control of a Mobile Micro-Actuator Array
D. Ruffieux
Centre Suisse d`Electronique et de Microtechnique SA, Neuchâtel, Switzerland

15:15 Single Chip, Self Supplied, Voltage and Charge Mode Double 80 V Piezoelectric Actuator Driver
L. Fontanella[1], G. Frattini[1], G. Ricotti[1], G. Pedrazzini[2]
[1]STMicroelectronics, Cornaredo, Milan, Italy
[2]STMicroelectronics, Laguna Niguel, CA, USA

15:40 to 16:10 Coffee Break

Session 1.6: Digital Processors
Chairman: T.G. Noll
RWTH Aachen, Germany

16:10 Electronic Processing for 10Gbit/s Dispersion Supported Transmission Systems
K. Köffers[1], F. Martini[2], W. Pöhlmann[1], B. Wedding[1]
[1]Alcatel SEL AG, Stuttgart, Germany
[2]Alcatel, Italy

16:35 A 1.3 GOPS Parallel DSP for High Performance Image Processing Applications
W. Hinrichs, J.P. Wittenburg, H. Lieske, H. Kloos, M. Ohmacht, J. Kneip, K. Rönner, P. Pirsch
Universität Hannover, Germany

17:00 2.44 GFLOPS 300MHz floating-point vector processing unit for high performance 3D graphics computing
N. Ide[1], M. Hirano[1], Y. Endo[1], S. Yoshioka[1], H. Murakami[1], A. Kunimatsu[1], T. Sato[1], T. Kamei[1], T. Okada[2], M. Suzuoki[2]
[1]Toshiba Corporation, Kawasaki, Japan
[2]Sony Computer Entertainment Inc., Japan

Tuesday, 21.09.99 HS 134 (Building LB)

Session 1.7: Low Power Circuit Techniques
Chairman: J.L. Huertas
University of Sevilla, Spain

10:40 Investigation on Low Voltage, Low Power Silicon Bipolar Design Topology for High Speed Digital Circuits
G. Schuppner, C. Pala, M. Mokhtari
Royal Institute of Technology, Kista, Sweden

11:05 A Low-Voltage Energy Scalable Static Differential Logic (ES²DL) Family
A.M. Fahim, M.I. Elmasry
University of Waterloo, Canada

11:30 Dual Threshold Voltage Domino Logic
J. Kao
Massachusetts Institute of Technology, Beaverton, OR, USA

11:55 Split Gates: A low swing technique for reducing power for high fanout gates
D. Somasekhar, K. Roy
Purdue University, West Lafayette, IN, USA

12:20 to 14:00 Lunch Break

Session 1.8: Memory Techniques
Chairman: H. Klar
TU Berlin, Germany

14:50 Area-Efficient Multiport Memories for the Tb/s Bandwidth Era
H.J. Mattausch, Y. Tatsumi, K. Kishi, T. Gyoten, K. Yamada
Hiroshima University, Higashi-Hiroshima, Japan

15:15 A 32Mb-4b/cell Analog Flash Memory Supporting Variable Density with 3V-Only Supply and Serial I/O
P.L. Rolandi, M. Pasotti, G. Campardo, R. Canegallo, G. De Sandre, G. Guaitini, C. Issartel, F. Lhermet, A. Maurelli, A. Rocchi, A. Kramer
STMicroelectronics, Agrate Brianza (MI), Italy

15:40 to 16:10 Coffee Break

Tuesday, 21.09.99 HS 134 (Building LB)

Session 1.9: High Speed Digital Circuits
Chairman: S. Rusu
Intel Corporation, Santa Clara, CA, USA

16:10 A Low-Jitter Mixed DLL for High-Speed DRAMs
J.J. Kim[1], B. Kim[1], S. Lee[2], S.-I. Cho[2]
[1]KAIST, Taejon, Korea (South)
[2]Samsung Electronics, Co. Ltd., Korea (South)

16:35 High Speed Capacitive Coupled Interface for Multipoint Connections
A. Schmidt[1], K. Hoffman[1], O. Kowarik[1], R. Pfeiffer[1], M. Moyal[2]
[1]Universität der Bundeswehr München, Neubiberg, Germany
[2]Infineon Technologies, Munich, Germany

17:00 A 5.3 GHz Programmable Divider for HiPerLAN in 0.25µm CMOS
N. Krishnapura, P. Kinget
Bell Laboratories, Murray Hill, NJ, USA

Wednesday, 22.09.99 Audimax (Building LA)

08:30 Invited Paper
Highly integrated RF-ICs for GSM, DECT and UMTS Systems. A Status Review and Development Trends.
J. Fenk
Infineon Technologies, Munich, Germany

Session 2.1: Oscillators
Chairman: J.L. Huertas
University of Sevilla, Spain

09:20 An improved low power crystal oscillator
W. Thommen
Microdul AG, Zurich, Switzerland

09:45 A Monolithic 0.4 mW SOA LC Voltage-Controlled Oscillator
J. van der Tang, S. Hahn
Philips Research Laboratories, Eindhoven, The Netherlands

10:10 to 10:40 Coffee Break

10:40 Invited Paper
The rapid increase in the capacity of the optical fiber
L. Thylen
University of Stockholm, Sweden

Session 2.2: Analogue Techniques 1
Chairman: K. Halonen
Helsinki University of Technology, Espoo, Finland

11:30 Reducing MOSFET 1/f Noise and Power Consumption by "Switched Biasing"
S.L.J. Gierkink, E.A.M. Klumperink, E. van Tuijl, B. Nauta
University of Twente, Enschede, The Netherlands

11:55 A 500MS/sec -54dB THD S/H Circuit in a 0.5µm CMOS Process
K. Hadidi[1], D. Muramatsu[2], T. Oue[2], T. Matsumoto[2]
[1]Urmia University, Iran
[2]Waseda University, Tokyo, Japan

12:20 to 14:00 Lunch Break

Wednesday, 22.09.99 Audimax (Building LA)

14:00 Invited Paper
High Speed Electronics Interfacing Fibre Networks
C. Svensson
University of Linköping, Sweden

Session 2.3: Analogue Techniques 2
Chairman: K. Halonen
Helsinki University of Technology, Espoo, Finland

14:50 A 0.5µm CMOS Analog RAM Chip for Real-Time Video Processing
R. Carmona, A. Rodríguez-Vázquez, S. Espejo,
R. Domínguez-Castro
Universidad de Sevilla, Spain

15:15 An Analog Baseband Circuitry for a WCDMA Direct Conversion Receiver
J. Jussila, A. Pärssinen, K. Halonen
Helsinki University of Technology, HUT, Finland

15:40 to 16:00 Coffee Break

16:00 to 18:00 Poster Session

19:30 to 22:30 Conference Banquet

Wednesday, 22.09.99 HS 104 (Building LB)

Session 2.4: Pipelined A/D Converters
Chairman: J.H. Huijsing
Delft University of Technology, The Netherlands

09:20 A 15-bit Pipelined Floating-Point A/D Converter
D.U. Thompson, B.A. Wooley
Stanford University, Stanford, CA, USA

09:45 An 8-bit Low-Voltage Pipelined ADC Utilizing Switched-Opamp Technique
M. Waltari, K. Halonen
Helsinki University of Technology, HUT, Finland

10:10 to 10:40 Coffee Break

Session 2.5: Low Power A/D and D/A Converters
Chairman: J.E. da Franca
Instituto Superior Tecnico, Lisboa, Portugal

11:30 A 1mW Delta-Sigma ADC with Fully Integrated Baseband Module for GSM application
Y. Kobayashi, K. Furukawa, K. Yamakido
Hitachi Ltd., Tokyo, Japan

11:55 A 1.8-3.3V High Speed Current Steering DAC Embedded Core
C. Neron, J.-Y. Michel
VLSI Technology Inc., Valbonne, France

12:20 to 14:00 Lunch Break

Session 2.6: Characterization of Submicron Effects
Chairman: C. Svensson
Linköping University, Sweden

14:50 Modeling of Digital Substrate Noise Generation and Experimental Verification Using a Novel Substrate Noise Sensor
M. van Heijningen, J. Compiet, P. Wambacq, S. Donnay, M. Engels, I. Bolsens
IMEC, Leuven, Belgium

15:15 Circuit Technique for Accurate Soft Error Rate Measurements
P. Hazucha, C. Svensson
Linköping University, Sweden

15:40 to 16:00 Coffee Break

16:00 to 18:00 Poster Session

Wednesday, 22.09.99 HS 134 (Building LB)

Session 2.7: Integrated VCOs 1
Chairman: A.H.M. van Roermund
Delft University of Technology, The Netherlands

09:20 Low supply voltage fully integrated CMOS VCO with Three terminals spiral inductor
N. Itoh[1], B. De Muer[2], M. Steyaert[2]
[1]Toshiba Corporation, Kawasaki, Japan
[2]Katholieke Universiteit Leuven, Belgium

09:45 Fully-Integrated Low Phase Noise Bipolar Differential VCOs at 2.9 and 4.4 GHz
A.M. Niknejad[1], R.G. Meyer[1], J.L. Tham[2],
[1]University of California, Berkeley, CA, USA
[2]Maxim Integrated Products

10:10 to 10:40 Coffee Break

Session 2.8: Integrated VCOs 2
Chairman: A.H.M. van Roermund
Delft University of Technology, The Netherlands

11:30 Impact of Indirect Stability on Phase Noise Performance of Fully-Integrated LC Tuned VCOs
C. Samori[1], A.L. Lacaita[1], A. Zanchi[1], S. Levantino[1], F. Torrisi[2]
[1]Politecnico di Milano, Italy
[2]STMicroelectronics, Catania, Italy

11:55 A fully integrated 2 GHz LC-VCO with phase noise of -125 dBc/Hz at 600 kHz
B. De Muer, C. De Ranter, M. Steyaert
Katholieke Universiteit Leuven, Belgium

12:20 to 14:00 Lunch Break

Session 2.9: RF-Oscillator Techniques
Chairman: A. Kaiser
IEMN - ISEN, Lille, France

14:50 A 2.7V, 2.64 Hz Fully Integrated Synchronous Oscillator for WLAN Applications
F. Badets, Y. Deval, J.-B. Bégueret, A. Spataro, P. Fouillat
Laboratoire IXL, Talence, France

15:15 A Wideband Linearisation Technique for Non-Linear Oscillators using a Multi-Stage Polyphase Filter
C. De Ranter, M. Borremans, M. Steyaert
Katholieke Universiteit Leuven, Belgium

15:40 to 16:00 Coffee Break

16:00 to 18:00 Poster Session

Wednesday, 22.09.1999 (Building LA)

16:00 – 18:00 Posters

A High-Speed CMOS On-Chip Temperature Sensor
L. Luh, J. Choma, Jr., J. Draper, H. Chiueh
University of Southern California, Los Angeles, CA, USA

Integrated Optoelectronic Receiver for a Pulsed Time-of-Flight Laser Radar
P. Palojärvi, T. Ruotsalainen, J. Kostamovaara
University of Oulu, Finland

A 66 x 66 pixels analog edge detection array with digital readout
J. Schemmel, M. Loose, K. Meier
Heidelberg University, Germany

A Low-Cost High-Accuracy CMOS Smart Temperature Sensor
A. Bakker, J.H. Huijsing
Delft University of Technology, The Netherlands

An Adaptive Bio-inspired Analog Silicon Retina
G. Sicard[1], G. Bouvier[1], V. Fristot[1], A. Lelah[2]
[1]Laboratoire des Images et des Signaux, Grenoble, France
[2]CNET, DTM/CET, Meylan, France

An 8-bit and a 10-bit Low power High-Speed Neuron MOS Digital-to-Analog Converter in 0.04 mm²
A. Rantala, P. Kuivalainen, M. Aberg
VTT Electronics, Finland

A CMOS 10Bit 37MS/s Pipelined A/D Converter with Code Regeneration and Averaging
B.W. Lee, G.H. Cho
Korea Advanced Institute of Science and Technology, Taejon, Korea (South)

Design for Optimum Performance-to-Power Ratio of a Continuous-time Sigma-Delta Modulator
L.J. Breems[1], E.J. van der Zwan[2], J.H. Huijsing[1]
[1]Delft University of Technology, The Netherlands
[2]Philips Research Laboratories, Eindhoven, The Netherlands

A Sigma-Delta Modulator with Extended Supply Voltages in 0.8µm SOI CMOS for Direct Ground Referred Instrumentation Interfacing
W. Redman-White[1], C. Easson[1], J. Benson[1], R.L. Rabe[2], M.J. Uren[3]
[1]The University of Southampton, United Kingdom
[2]Honeywell SSEC, Plymouth, MN, USA
[3]Defence Evaluation and Research Agency, Malvern, United Kingdom

A CMOS 12-bit 15 Msample/s Digitally Self-calibrated Pipelined A/D converter
R. Rombouts, S. Audenaert, L. Weyten
University of Gent, Belgium

An 1.1-GHz Packaged CMOS VCO with Phase Noise of -126 dBc/Hz at a 600-kHz Offset
C.-M. Hung, K.K. O
University of Florida, Gainesville, FL, USA

A Two-Bit Delta-Sigma-Modulator with 83dB SNDR for Digital Cellular Telephones
S. Lindfors, M. Länsirinne, T. Lindeman, K. Halonen
Helsinki University of Technology, Espoo, Finland

Algorithmic Design of A 900MHZ CMOS RF Power Amplifier Using SPICE-Smith Chart Method
A. Kheirkhahi, S.M. Fakhraie, M. Kamareie
University of Tehran, Iran

Second Order Distortion in CMOS Direct Conversion Receivers for GSM
S. Laursen
Aalborg University, Denmark

A 1.8GHz BiCMOS RF Receiver IC Taking into Account the Cross Modulation for CDMA Wireless Applications
B.-K. Ko, D.-B. Cheon, S.-W. Kim, J.-S. Ko, J.-K. Kim,
B.-H. Park
Samsung Electronics, Korea (South)

A Bandpass Sigma-Delta Demodulator For Digital Radio
A. Keady[1], C. Lyden[2]
[1]Silicon Systems Limited, Dublin, Ireland
[2]National Microelectronics Research Centre, Cork, Ireland

New High Performance and Wide Range Tunable Two-Stage 3GHz CMOS RF Hetero-Linked Oscillators
J.T. Hwang, S.H. Woo, J.Y. Ryu, K. Lee, G.H. Cho
Korea Advanced Institute of Science and Technology, Taejon,
Korea (South)

A 0.5µm CMOS 10^6 Transistors Analog Programmable Array Processor for Real-Time Image Processing
G. Linán, P. Foldsey, S. Espejo, R. Domínguez-Castro,
A. Rodríguez-Vázquez
Universidad de Sevilla, Spain

All-Analog Decoder for a Binary (18,9,5) Tail-Biting Trellis Code
F. Lustenberger[1], M. Helfenstein[1], G.S. Moschytz[1],
H.-A. Loeliger[2], F. Tarköy[2]
[1]ETH Zentrum, Zurich, Switzerland
[2]Endora Tech AG, Basel, Switzerland

A high resolution Time-to-Digital Converter for ultrasonic flow measurement

F. Riedel[1], R. Eusemann[2]
[1]Siemens Metering AG, Zug, Switzerland
[2]Landis & Staefa Produktion GmbH

A 1V Active RC Filter with On-Chip Frequency and Q Tuning

H. Huang, E.K.F. Lee
Iowa State University, Ames, Iowa, USA

A 100MHz CMOS g_m-C Bandpass Filter

P. Andreani[1], S. Mattisson[2]
[1]Lund University, Sweden
[2]Ericsson Mobile Communications AB, Lund, Sweden

A 1.5 V, 30 Msps, 9- to 10-bit equivalent Current-mode CMOS Sample-and-hold Circuit

Y. Sugimoto
Chuo University, Tokyo, Japan

A Low-Voltage CMOS Transconductor for Very High Frequencies

S. Celma, J. Sabadell, C. Aldea, P.A. Martínez
Universidad de Zaragoza, Spain

Programmable Voltage Multipliers for Pacemaker Output Pulse Generation in CMOS 0.8 µm Technology

A. Novo[1], A. Gerosa[1], A. Neviani[1], E. Zanoni[1], A. Mozzi[2]
[1]Università di Padova, Italy
[2]MEDICO S.p.A., Rubano (Padova), Italy

A 430MHz, -52dB THD, Single Transconductor, 3rd-Order Low-Pass Filter and its Extension to a 5th-Order, in a 0.5 µm CMOS Process

K. Hadidi[1], K. Eguchi[2], T. Matsumoto[2]
[1]Urmia University, Iran
[2]Waseda University, Tokyo, Japan

Robust Digitization and Digital Non-Uniformity Correction in a Single Chip CMOS Camera

I. Koren[1], U. Ramacher[1], H. Geib[1], S. Kirmser[1], C. Heer[1], J.-U. Schlüßler[2], J. Dohndorf[2], J. Werner[3]
[1]Infineon Technologies Inc., Munich, Germany
[2]Technische Universität Dresden, Germany
[3]AMI Inc.

Advanced CMOS and BiCMOS photonic receiver ICs

K. Kieschnick, T. Heide, A. Ghazi, H. Zimmermann,
P. Seegebrecht
Christian-Albrechts-Universität Kiel, Germany

A CMOS Nanosecond-to-Millivolt Converter

H. Leopold, H. Senn
Technische Universität Graz, Austria

A Low-power Truly-modular 1.8GHz Programmable Divider in Standard CMOS Technology

C. Vaucher, Z. Wang
Philips Research Laboratories, Eindhoven, The Netherlands

Design and Optimization of Sense-Amplifier-Based Flip-Flops

B. Nikolic[1], V.G. Oklobdzija[2]
[1]University of California, Davis
[2]Integration Corp., Berkeley, CA, USA

A Low-Power Quadtree Fractal Image Decoder

C.-H. Kim, H.-J. Park, L.-S. Kim
Korea Advanced Institute of Science and Technology, Taejon, Korea (South)

A Bootstrapped Latched CMOS Logic Family with Demand-on Boosting for Low-Power Application

B.-S. Kong, D.-O. Kang, Y.-H. Jun
LG Semicon Co., Ltd., Seoul, Korea (South)

ECL-CMOS Logic LSI Technology using 20 GHz Latch with CMOS Test Circuits

S. Yabuki, A. Hayashi, Y. Ito, T. Maruyama, H. Okada, M. Usami, K. Higeta, M. Hamamoto, S. Isomura
Hitachi Ltd., Tokyo, Japan

A 250MHz Low Voltage Swing Bus Driver for Embedded Memory Logic

H.S. Lee, B.-S. Kim, S.-H. Chang, L.-S. Kim
KAIST, Taejon, Korea (South)

ASPRO: an Asynchronous 16-Bit RISC Microprocessor with DSP Capabilities

M. Renaudin[1], P. Vivet[2], F. Robin[2]
[1]TIMA - INPG, Grenoble, France
[2]France Telecom, Meylan, France

Distributed Active Clock Network

V. Gutnik, A. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA, USA

Production DC Screening Techniques for RF Performances of Bipolar ICs

S.-G. Lee[1], S.-O. Lee[2], J.-S. Ko[2]
[1]Information and Communications University, Taejon, Korea (South)
[2]Samsung Electronics, Korea (South)

A 5-Parameter Mismatch Model for Short Channel MOS Transistors

T. Serrano-Gotarredona, B. Linares-Barranco
National Microelectronics Center, Sevilla, Spain

Thursday, 23.09.99 Audimax (Building LA)

08:30 Invited Paper
Automotive Semiconductor Technologies for the New Millenium
B. Murari
STMicroelectronics, Italy

09:20 to 09:25 ESSCIRC 2000

Session 3.1: Mixed Signal Sensors
Chairman: G. Tröster
ETH, Zurich, Switzerland

09:25 Microelectronic Components for a Retina Implant System
S. Kolnsberg, T. Kneip, X. Lü, J. Huppertz, R. Hauschild, M. Schwarz, D. Hammerschmidt, B.J. Hosticka, L. Ewe, H.K. Trieu
Fraunhofer Institute of Microelectronic Circuits and Systems, Duisburg, Germany

09:50 A Fully Integrated Sensor Interface Chip
D. McCartney[1], A. Sherry[1], T. Meany[1], T. Cummins[1], D. Brannick[2], L. MacManus[3]
[1]Analog Devices B.V., Limerick, Ireland
[2]Accutron Ltd., Dublin, Ireland
[3]Trinity College, Dublin, Ireland

10:15 to 10:45 Coffee Break

10:45 Invited Paper
CMOS or CCD image sensors for digital still applications?
A.J.P. Theuwissen
Philips Imaging Technology, Eindhoven, The Netherlands

Session 3.2: Mixed Signal Interfaces 1
Chairman: J.H. Huijsing
Delft University of Technology, The Netherlands

11:35 A Multichannel CMOS Interface IC for Recording Car-Crash Conditions
C. Ji[1], J. Kernhof[1], R. Krenzke[1], H. Bacic[2], T. Grill[2], A. Hertzner[2], J. Wangler[2]
[1]Dialog Semiconductor GmbH, Kirchheim/Teck, Germany
[2]Mannesmann VDO AG, VS-Villingen, Germany

12:00 ASK 10% Demodulator for Contactless Smart Card IC
G. Nebel, A. Blum, D. Eichner, V. Güngerich, M. Melchior, R. Reiner, G. Schraud, U. Weder
Infineon Technologies, Munich, Germany

12:25 to 14:00 Lunch Break

Thursday, 23.09.99 Audimax (Building LA)

14:00 Invited Paper
Sensor Systems - Interface between Environment and Application
D. Hammerschmidt
Fraunhofer Inst. für Mikroelektronische Schaltungen und Systeme, Duisburg, Germany

Session 3.3: Mixed Signal Interfaces 2
Chairman: A. Rothermel
Universität Ulm, Germany

14:50 Asynchronous 250 Mbit/s Optical Receivers with Integrated Detector in Standard CMOS technology for Optocoupler Applications
C. Rooman, D. Coppée, M. Kuijk
University of Brussels, Belgium

15:15 164 Ms/s Tape Drive Channel IC with 4 Independent Digital Peak Detect Read/Write Channels and Automatic Tape Speed Tracking over a 3:1 Range
J. O´Dwyer[1], R. Maher[1], S. McDonagh[1], M. Looney[1], A. Dwyer[1], M. Jackson[1], C. Lynch[1], F. Severi[1], C. McAuliffe[1], D. Moloney[1], C. Gamble[2], S. Swanbeck[2]
[1]Silicon Systems Limited, Dublin, Ireland
[2]Hewlett-Packard Company, Boise, Idaho, USA

15:40 to 16:00 Young Scientists Award - Closing Session

Thursday, 23.09.99 HS 104 (Building LB)

Session 3.4: Image Sensors
Chairman: J.H. Huijsing
Delft University of Technology, The Netherlands

09:25 Vertically Integrated Sensors for Advanced Imaging Applications
S. Benthien[1], T. Lulé[1], B. Schneider[2], M. Wagner[1], M. Verhoeven[1], M. Böhm[1,2]
[1]Silicon Vision GmbH, Siegen, Germany
[2]Universität-GH Siegen, Germany

09:50 A High Dynamic Range CMOS Image Sensor for Automotive Applications
M. Schanz[1], C. Nitta[1], T. Eckart[1], B.J. Hosticka[1], R. Wertheimer[2]
[1]Fraunhofer Institute of Microelectronic Circuits and Systems, Duisburg, Germany
[2]Bayerische Motoren Werke AG, Munich, Germany

10:15 to 10:45 Coffee Break

Session 3.5: Integrated Mechanical Sensors
Chairman: F. Maloberti
University of Pavia, Italy

11:35 A Low Noise Accelerometer with Digital PID-type Controller and Multibit Force Feedback
C. Lang, R. Tielert
University of Kaiserslautern, Germany

12:00 An Absolute Air Pressure Smart Sensor Family with 2 Dimensional Calibration
D. Weiler, O. Machul, J. Amelung, D. Hammerschmidt, B.J. Hosticka
Fraunhofer Institute of Microelectronic Circuits and Systems, Duisburg, Germany

12:25 to 14:00 Lunch Break

Session 3.6: Smart Optical Sensors
Chairman: F. Maloberti
University of Pavia, Italy

14:50 A 256x256-pixel Smart CMOS Image Sensor for Line based Stereo Vision Applications
Y. Ni, J.H. Guan
Institut National des Télécommunications, Evry, France

15:15 Design of an integrated photo detector circuit for laser Doppler blood flow monitoring
J. Nieland, H. Van Kranenburg, H. Wallinga, A. Serov, W. Steenbergen, F.F.M. de Mul
University of Twente, Enschede, The Netherlands

Thursday, 23.09.99 HS 134 (Building LB)

Session 3.7: Transceiver Circuits 1
Chairman: M. Steyaert
ESAT MICAS, Heverlee, Belgium

09:25 An 85 MHz IF Bandpass Sigma-Delta Modulator for CDMA Receivers
S. Bazarjani, S. Younis, J. Goldblatt, D. Butterfield, G. McAllister, S. Ciccarelli
QUALCOMM Inc., San Diego, CA, USA

09:50 A 170MHz Quadrature Down-Converter in 0.8µm BiCMOS for Very Low Power Pagers
P. Orsatti, Q. Huang
Swiss Federal Institute of Technology, Zurich, Switzerland

10:15 to 10:45 Coffee Break

Session 3.8: Transceiver Circuits 2
Chairman: M. Steyaert
ESAT MICAS, Heverlee, Belgium

11:35 A 200 MHz Sub-mA RF Front End for Wireless Hearing Aid Applications
A. Deiss, D. Pfaff, Q. Huang
Swiss Federal Institute of Technology, Zurich, Switzerland

12:00 RF Circuits Technique of Dual-band Transceiver IC for GSM and DCS1800 applications
K. Takikawa[1], T. Yamawaki[1], S. Tanaka[1], M. Kokubo[1], T. Wakuda[1], K. Irie[1], K. Hori[1], Y. Okabe[1], T. Hashimoto[1], M. Kasahara[1], B. Henshaw[2], J.R. Hildersley[2]
[1]Hitachi Ltd., Tokyo, Japan
[2]The Technology Partnership plc., United Kingdom

12:25 to 14:00 Lunch Break

Session 3.9: RF Power Amplifieres
Chairman: P.J. Mole
Nortel, Harlow, United Kingdom

14:50 A 200MHz IF BiCMOS Chip for Linear LINC Transmitters
B. Shi, L. Sundström
Lund University, Sweden

15:15 First Integrated Bipolar RF PA Family for Cordless Telephones
S. Weber
Siemens AG, Munich, Germany

Friday, 24.09.99

Integrated Systems

Organiser: H.-L. Fiedler
Fraunhofer IMS, Duisburg, Germany

Summary

The workshop focuses on the implementation of complex systems with highly integrated circuits. Three papers from different fields of applications will present „best practice“ examples and highlight not only technical details but also examine how to manage complex system designs, find optimal cost-performance tradeoffs and streamline the design process.

Contributed Papers

Circuit Design Challenges for Integrated Systems Design

Stefan Rusu
Intel Corporation, Santa Clara, United States

Abstract

Today's PC architecture is driven by the need for higher integration, lower cost and increasing performance. This paper will review integration trends in modern microprocessors and chipsets and highlight the circuit design challenges laying ahead. Specific focus areas include I/O interfaces with multiple voltage levels, memory latency reduction techniques and multiple clock domains generation and synchronization.

All Digital Receiver Chipset for Direct To Home Satellite Radio

Dr. Franz-Otto Witte
Micronas Intermetall, Freiburg, Germany

Abstract

A new digital satellite radio system for Africa, Asia and South America has been established recently. This 'WorldSpace' system uses QPSK-modulation, error correction and MPEG Layer 2.5 audio data compression. The presented chipset performs the full decoding chain from IF-conversion to analog audio output and is optimized for low-cost low-power consumer radio receivers.

The "Single Chip TV": an example of a technical and commercial successful implementation of an integrated system on silicon.

Joop van Lammeren
Philips Semiconductors, Nijmegen, The Netherlands

Abstract

The consumer electronics industry is strongly driven by the need to bring together more and more complex systems elements into less components in order to offer cheaper, more reliable and easier to produce products. The "Single chip TV" of Philips is an example of a complex IC, that has been designed to meet these goals. It is produced in large quantities, proving its success of acceptance in the TV industry. An overview is given about the considerations and choices made, that have lead to the conception, design and production of an integration of all main TV video processing elements on one single Integrated Circuit.

Schedule

8:30	Registration
9:00	Opening Introduction
9:15	Circuit Design Challenges for Integrated Systems Design S. Rusu, INTEL
10.00	All Digital Receiver Chipset for Direct To Home Satellite Radio F.O. Witte, Micronas Intermetall
10.45	Coffee Break
11.15	The "Single Chip TV": an example of a technical and commercial successful implementation of an integrated system on silicon. J. v. Lammeren, Philips Semiconductors
12.00	Panel Discussion „What are the key issues for successful integrated system design?“
12.30	End of Workshop

Conference Organisation

Chairman:	G. Zimmer, Fraunhofer IMS and University of Duisburg, Germany
Vice Chairmen:	K. Weyer, ELMOS, Germany W. Splettstößer, Siemens, Germany
Conference Secretary:	C. Metz, Fraunhofer IMS, Germany
Local Arrangements:	S. Roß, Fraunhofer IMS, Duisburg, Germany

Technical Programme Committee

Chairman: B. Hosticka, Fraunhofer IMS and University of Duisburg, Germany

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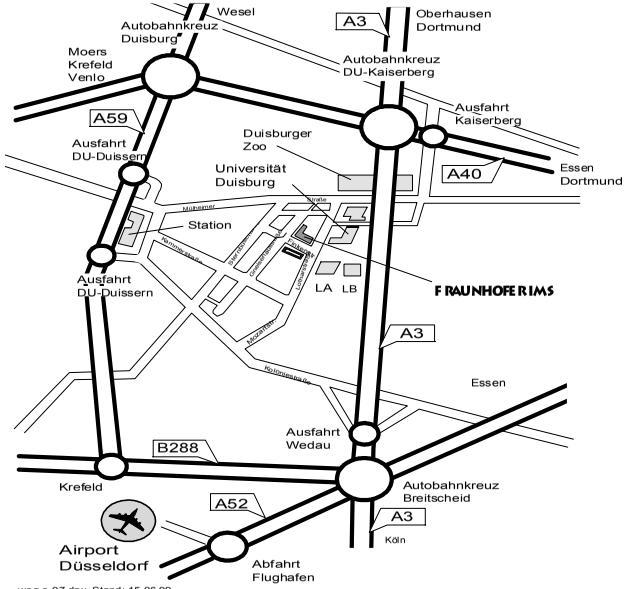
S. Rusu, Intel, USA

TRAVEL INFORMATION



weg-e-07.drw, Stand: 15.06.99

1. By Car

Motorway A 3
- Exit "Duisburg-Wedau"
- drive towards "Innenstadt" (Koloniestraße)
- at the traffic lights turn right into Mozartstraße running into Lotharstraße
- after about 800 meters turn right on the Campus of the University

Motorway A 40
- Exit "Duisburg-Kaiserberg"
- drive towards "Innenstadt", "Zoo" (Carl-Benz-Straße)
- After about 1000 meters turn right (towards "Innenstadt") into Mülheimer Straße and pass the zoo
- at the first crossroads with traffic lights turn left into Lotharstraße
- after about 800 meters turn left on the Campus of the University

2. By Train

Arrival at Duisburg Hbf. (main station)
a) Taxi (takes about 5 minutes)
b) Bus no. 924, 933 (towards "Zoo/Uni") or no. 936 (towards "Städtische Kliniken"), get off at "Universität" (takes about 10 minutes)
c) Underground line 901 (towards "Zoo/Uni", "Mülheim"), get off at "Zoo/Uni" (takes about 10 minutes)

3. By Plane

Arrival at Düsseldorf Airport
a) Taxi (takes about 20 minutes)
b) S-Bahn (station within airport terminal, takes about 25 minutes)
   - line S 21, get off at Duisburg Hbf. (trains run every hour)
   - line S 7, change at "Unterrath" into line S 1, get off Duisburg Hbf. (trains run every 40 minutes)
c) Car (takes about 20 minutes) on A 52 (towards "Essen"), change at intersection "Breitscheid" to A 3 (towards "Oberhausen"), exit "Duisburg-Wedau"; see point one.