15th EUROPEAN SYMPOSIUM RELIABILITY OF ELECTRON DEVICES, FAILURE PHYSICS AND ANALYSIS

Zürich — Switzerland
4 – 8 October 2004

with the technical co-sponsorship of :

IEEE - Electron Devices Society - Reliability Society

IEEE
Networking the World™

ELECTRON DEVICES SOCIETY®

ReliabilitySociety

with the support of:

ETH Zürich

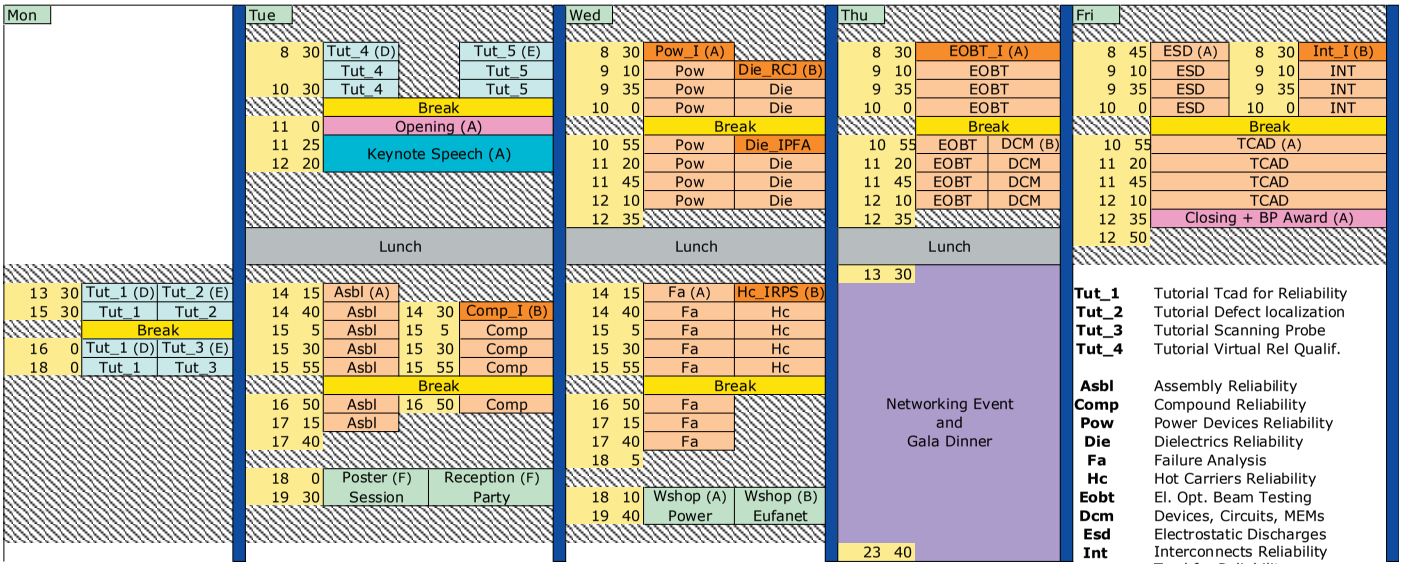
ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

in conjunction with :

EOBT (Electron and Optical Beam Testing)

organised by :

IIS Integrated Systems Laboratory
ETH Zürich



Session Rooms
A Auditorium Maximum
B D 7.2

Tutorial Rooms
D D 1.2
E D 7.2

Poster Session Gallery Floor F

Coffee Breaks Foyer Floor D

Exhibition Foyer Floor D

Lunch Mensa ETH

ESREF Steering Committee

X. Aymerich	Univ. of Barcelona	E
L. J. Balk	Univ. of Wuppertal	D
J. Bisschop	Philips	NL
M. Ciappa	ETH Zurich	CH
Y. Danto	Univ. of Bordeaux	F
F. Fantini	Univ. of Modena	I
J. P. Fortea	CNES	F
W. Gerling	Infineon	D
C. Lindsay	Marconi	UK
V. Loll	Nokia	DK
L. Lonzi	STMicroelectronics	I
G. Groesenecken	IMEC	B
J. Moeltoft	Technical Univ. of Denmark	DK
A. J. Mouthaan	Univ. of Twente	NL
N. Stojadinovic	Univ. of Nis	Y
R. Thomas	Technology Experts Network	USA
W. Wondrak	Daimler Chrysler	D

Program Committee

Wolfgang Fichtner	General Chair
Mauro Ciappa	Technical Program Chair
Dölf Aemmer	Local Organization Chair
Christine Haller	Conference Secretary
Bruno Fischer	Exhibition Officer
Anja Böhm	WEB officer

Technical Program Committee of ESREF 2004

Chair	Mauro Ciappa	ETH Zürich	CH

Sub-Com Circuits, Systems, and Assembly Reliability

Marcantonio Catelani	Univ. Firenze	I
Yves Danto	Univ. Bordeaux	F
Ward De Ceuninck	Univ. Limburgs	B
Jorgen Moeltoft	TU Denmark	DK
Andreas Preussger	Infineon	D
Robert Thomas	Experts Network	USA
Consolato Versace	STMicroelectronics	I
Paolo Cova	Univ. Parma	I
Christian Zardini	Univ. Bordeaux	F

Sub-Com ESD & Latch up

Antonio Andreini	STMicroelectronics	I
Marise Bafleur	LASS	F
Gianluca Boselli	Texas Instruments	USA
Horst Gieser	FhG	D
Ton Mouthaan	Univ. Twente	NL
Wolfgang Stadler	Infineon	D
Matthias Stecher	Infineon	D
Wolfgang Wilkening	Bosch	D
Lucia Zullino	STMicroelectronics	I

Reliability Dielectrics & Hot Carriers

Xavier Aymerich	Univ. Barcelona	E
Francis Balestra	ENSERG	F
Gérard Ghibaudo	ENSERG	F
Gabriella Ghidini	STMicroelectronics	I
Guido Groesenecken	IMEC	B
Giuseppe La Rosa	IBM	USA
Hans Reisinger	Infineon	D
James Stathis	IBM	USA
Nino Stojadinovic	Univ. Nis	Y

Interconnects Reliability

Barbara Zanderighi	STMicroelectronics	I
Andrea Scorzoni	Univ. Perugia	I
Fausto Fantini	Univ. Modena	I

Sub-Com TCAD for Reliability

Lars Bomholt	ISE AG	CH
Hervé Jaouen	STMicroelectronics	F
Gerhard Wachutka	TU Munich	D

Sub-Com Power Devices & Automotive Reliability

Giovanni Busatto	Univ. Cassino	I
Gérard Coquery	INRETS	F
Leonardo Lonzi	STMicroelectronics	I
Eckhardt Wolfgang	Siemens	D
Wolfgang Wondrak	Daimler-Chrysler	D
Raymond Zehringer	ABB	CH

Sub-Com Photonics & Compound Materials Reliability

Jean-Michel Dumas	Univ. Limoges	F
Mattia Borgarino	Univ. Modena	I
Hans Hartnagel	TU Darmstadt	D
Nathalie Labat	Univ. Bordeaux	F
Roberto Menozzi	Univ. Parma	I
Giulia Salmini	Pirelli	I
Bernd Witzigmann	ETH Zürich	CH
Enrico Zanoni	Univ. Padova	I

Sub-Com Failure Analysis Techniques

Christian Boit	TU Berlin	D
Jean-Pierre Fortea	CNES	F
Siegfried Görlich	Infineon	D
Philippe Perdu	CNES	F
Alan Street	Qualcomm	USA
Massimo Vanzi	Univ. Cagliari	I

Sub-Com EOBT

Peter de Wolf	Veeco	USA
Dionysz Pogany	TU Vienna	A
Ludwig Balk	Univ. Wuppertal	D
Ronald Cramer	Altis	F
Wolfgang Mertin	Univ. Duisburg	D
Jacob Phang	Univ. Singapore	Singapore

Sub-Com MEMs & Nanotechnology Reliability

Ingrid de Wolf	IMEC	B
Wilfrid Claeys	Univ. Bordeaux	F
Nico de Rooji	Univ. Neuchâtel	CH

ESREF 2004, the 15th European Symposium on Reliability of Electron Devices will take place in Zurich (Switzerland) from 4 to 8 October 2004.
This international symposium continues to focus on recent developments and future directions in quality and reliability Management of materials, devices and circuits in microelectronics. It provides an open forum to develop all aspects of reliability management and advanced analysis techniques for present and future semiconductor applications. ESREF 2004 also includes the former Electron and Optical Beam Test Conference (EOBT) and it is co-sponsored by the IEEE Electron Device and IEEE Reliability Societies.

Conference Site

The conference takes place at the

Swiss Federal Institute of Technology (ETH)
Main Building (Hauptgebäude)
Rämistrasse 101, CH-8092 Zurich, Switzerland
Phone +41 1 632 1111

Program Highlights

The Conference takes place from October 4 to 8, 2004 in the historical building of the Swiss Federal Institute of Technology (ETH) in Zurich, with the logistic support of the ETH and with the technical co-sponsorship of the IEEE Electron Device Society and of the IEEE Reliability Society.
The technical program of ESREF 2004 has been arranged to continue the tradition of the conference series while trying to identify the highlights of the fast evolving electronic device technology. In this perspective, the Symposium is opened by the keynote address of Shigeru Komatsu, Chief Knowledge and Technical Infrastructure Officer of the Toshiba Corp providing critical insight into the future of semiconductor manufacturing and related yield issues. Invited contributions address the state of the art of the R&D in fields of particular interest such as noise as reliability indicator, failures induced by cosmic radiation in power devices, time-resolved photon emission analysis, and as reliability challenges caused by ultra-low k interlevel dielectrics. Further subjects are covered by tutorial courses on the use of Technology Computer Aided Design (TCAD) in reliability, on capabilities and limits of scanning probe techniques for semiconductors, on the implementation of virtual reliability qualification procedures, and on ESD testing. Finally, additional hot topics such as the efficiency of the most recent failure analysis techniques, and the optimum thermal management in power devices are debated in dedicated Workshops.
The 103 papers presented at this conference all passed a two-step reviewing process by the Technical Committee composed by nearly 50 worldwide reputated specialists from industry and academy. The logistic constraints imposed a three-day conference program with 41 papers proposed as posters and 62 as oral presentations. Poster and oral contributions have been organized in 11 technical sessions: Assembly Reliability, Compound Device Reliability, Power Device Reliability, Dielectrics Reliability, Failure Analysis & Advanced Characterization Techniques, Hot Carrier Reliability, Electron & Optical Beam Testing, Device, Circuits & MEMs Reliability, Electrostatic Discharges, Interconnects Reliability, and TCAD for Reliability. The last session on the use of Technology Computer Aided Design tools for reliability has been proposed for the first time, due to the increasing role played by device and process simulation in the implementation of built-in reliability programs in microelectronics.
ESREF 2004 improved the existing links with the sister conferences in reliability worldwide. In fact, this year the recipients of the Best Paper Award of the International Reliability Physics Symposium (IRPS, USA), of the Reliability Center of Japan Symposium (RCJ, Japan), and of the International Symposium on Physical and Failure Analysis of Integrated Circuits (IPFA, Singapore) have been invited in Zurich to present their results.
Finally, special attention has been paid to promote the technical and the human contacts among the participants of the Symposium. A special half-day networking event has been proposed, where all the attendees could meet each other in a pleasant and informal alpine environment at the lake of Lucerne.
The Proceedings of ESREF 2004 will be published as a special issue of the journal Microelectronics Reliability by the publisher Elsevier.

Tutorials

Five tutorial courses are proposed before the beginning of the conference:

Monday October 4, 2004, 13:30 – 18:00 Room D 1.2

Tutorial 1. TCAD simulation tools for built in reliability in semiconductor devices

Chair: Chiara Corvasce, ETH Zürich

Speakers: Pavel Tichomirov and Lars Bomholt
Integrated Systems Engineering AG, Affolternstrasse 52, CH-8050 Zurich

Monday October 4, 2004, 13:30 – 15:00 Room D 7.2

Tutorial 2. Defect localization in ICs using laser techniques

Chair: Maria Stangoni, ETH Zürich

Speakers: Dean Lewis[a] and Philippe Perdu[b]
[a] IXL ENSEIRB CNRS UMR 5818 , Université Bordeaux, Talence France
[b] CNES- French Space Agency, Toulouse France

Monday October 4, 2004, 15:30 – 18:00 Room D 7.2

Tutorial 3. Applications of Scanning Probe Microscopy for Failure Analysis

Chair: Maria Stangoni, ETH Zürich

Speaker: Peter De Wolf
VEECO INSTRUMENTS SAS, Dourdan France

Tuesday October 5, 2004, 08:30 – 10:30 Room D 1.2

Tutorial 4. Virtual Reliability Qualification

Chair: Valter Loll, Nokia

Speaker: G.Q. Zhang
Technical University of Eindhoven and Philips Centre For Industrial Technology, Eindhoven, The Netherlands

Tuesday October 5, 2004, 08:30 – 10:30

Tutorial 5. ESD Testing: HBM to very fast TLP Room D 7.2

Chair: Luca Sponton, ETH Zürich

Speaker: Horst A. Gieser
Fraunhofer Institut für Zuverlässigkeit und Mikrointegration - IZM, München

Keynote Speech

A critical insight into the future semiconductor solutions

Shigeru Komatsu

Chief Knowledge & Technical Infrastructure Officer Toshiba Corporation, Japan

Invited contributions

Low frequency noise as a reliability diagnostic tool in compound semiconductor transistors

N. Labat, N. Malbert, C. Maneux, A. Touboul

IXL Laboratory - CNRS - ENSEIRB - University of Bordeaux, France

Reliability of power electronic devices against cosmic radiation-induced failure

G. Soelkner[a], W. Kaindl[b], H.-J. Schulze[a], G. Wachutka[b]

[a] Infineon Technologies, Germany
[b] Institute for Physics of Electrotechnology, Munich University of Technology, Germany

Time Resolved Photon Emission Processing Flow for IC Analysis

R. Desplats[a], G. Faggion[a], M. Remmach[a], F. Beaudoin[a], P. Perdu[a], D. Lewis[b]

[a] CNES-Thales Laboratory, French Space Agency, France
[b] IXL Laboratory, 351 cours de la Libération, 33405 Talence Cedex – France

Reliability Challenges with Ultra-Low k Interlevel Dielectrics

J.R. Lloyd, M.R. Lane, X.-H. Liu, E. Liniger, T.M. Shaw, C.-K. Hu, R. Rosenberg

IBM T.J. Watson Research Center, Yorktown Heights NY 10598, USA

The study of TDDB lifetime estimation for thin gate dielectrics (RCJ Best Paper Award)

Takeshi Shigeo, Kazuhiko Suzuki, Madoka Muta

System LSI Reliability Engineering Gr. System LSI Quality & Reliability Engineering Department, Toshiba Semiconductor Company, Japan

Negative Bias Temperature Instability in Triple Gate Transistors (IPFA Best Paper Award)

Shigenobu Maeda, Jung-A Choi, Jeong-Hwan Yang, You-Seung Jin, Su-Kon Bae, Young-Wug Kim, Kwang-Pyuk Suh

Technology Development Team, System LSI Division, Samsung Electronics, Korea

Comparison of Oxide Breakdown Progression in Ultra-Thin Oxide SOI and Bulk pMOSFETs (IRPS Best Paper Award)

C. T. Chan, C. H. Kuo, C. J. Tang, M. C. Chen, Tahui Wang, S. Huang Lu, H.C. Hu*, T.F. Chen*, C.K. Yang*, M.T. Lee*, D.Y. Wu*, J.K. Chen*, S.C. Chien*, S. W. Sun**

Department of Electronics Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan
*Technology and Process Development Division, UMC, Hsin-Chu, Taiwan

Conference Program

Tuesday, October 5

11:00 Opening

11:25 Keynote Speech — Auditorium Maximum

"A critical insight into the future semiconductor solutions"

Shigeru Komatsu
Chief Knowledge & Technical Infrastructure Officer Toshiba Corporation, Japan

12:20 Lunch

Session Assembly Reliability (Asbl) — Auditorium Maximum

Co-chairs: J. Moltoft, Technical Univ. of Denmark, W. Gerling, Consultant

14:15 Characterization and fatigue damage simulation in SAC solder joints

M.Erinc, P.J.G.Schreurs, G.Q.Zhang, M.G.D.Geers
Materials Technology, Department of Mechanical Engineering, Eindhoven University of Technology, The Netherlands

14:40 Effect of long and short Pb-free soldering profiles of IPC/JEDEC J-STD-020 on plastic SMD packages

P. Alpern[a], K.C. Lee[b] and R. Tilgner[a]
[a] Infineon Technologies, Corporate Assembly and Testing, Germany
[b] Infineon Technologies Asia Pacific, Product Reliability and Analysis, Singapore

15:05 Reliability of Low-Cost PCB Interconnections for Telecommunication Applications

G. Duchamp, F. Verdier, Y. Deshayes, F. Marc, Y. Ousten, Y. Danto
Laboratoire IXL – ENSEIRB – UMR CNRS 5818, 33405 Talence, France

15:30 Effect of bonding pressure on reliability of flip chip joints on flexible and rigid substrates

L. Frisk, A. Seppälä and E. Ristolainen
Institute of Electronics, Tampere University of Technology, 33101 Tampere, Finland

15:55 How to study delamination in plastic encapsulated devices

Hélène Frémont[a], Jean-Yves Delétage[a], Kirsten Weide-Zaage[b], Yves Danto[a]
[a] IXL - ENSEIRB - CNRS, University of Bordeaux, France
[b] Laboratorium für Informationstechnologie, University of Hannover, Germany

Break

16:50 Characterization and Modelling of Moisture Driven Interface Failures

M.A.J. van Gils[a], P.J.J.H.A. Habets[b], G.Q. Zhang[ab], W.D. van Driel[a], P.J.G. Schreurs[b]
[a] Philips, P.O. Box 218, 5600 MD, Eindhoven, The Netherlands
[b] Eindhoven University of Technology, The Netherlands

17:15 Metal migration in epoxy encapsulated ECL devices

C. Zhang, P. Yalamanchili, M. Al-Sheikhley and A. Christou
Materials Science and Engineering and Reliability Engineering Center, University of Maryland, USA

Tuesday, October 5

Session Compound Reliability (Comp) Room D 7.2

Co-Chairs: E. Zanoni, University of Padova, A. Touboul, University of Bordeaux

14:30 Low frequency noise as a reliability diagnostic tool in compound semiconductor transistors (INVITED)

N. Labat, N. Malbert, C. Maneux, A. Touboul
IXL Laboratory - CNRS - ENSEIRB, University of Bordeaux, France

15:05 Reliability Investigation of Gallium Nitride HEMT

A. Sozza[abc], C. Dua[a], E. Morvan[a] , B. Grimbert[d], V. Hoel[d] , S.L. Delag[ae], N. Chaturvedi[d], R. Lossy[d], J. Wuerfl[d]
[a] TRT/Tiger, France
[b] DEI, Università degli Studi di Padova, Italy
[c] IXL Laboratory, University of Bordeaux, France
[d] IEMN/Tiger, France
[e] FBH, Ferdinand-Braun-Institut fuer Hoechstfrequenztechnik, 12489 Berlin, Germany

15:30 Hot carrier aging degradation phenomena in GaN based MESFETs

F. Rampazzo[a], R. Pierobon[a], D. Pacetta[a], C. Gaquiere[b], D.Theron[b], B. Boudart[c], G. Meneghesso[a], E. Zanoni[a]
[a] University of Padova, Department of Information Engineering, and INFM - UdR Padova, Italy
[b] Institut d'Eletronique et de Microelectronique du Nord, CNRS 8520, Départment Hyperfréquences et Semiconducteurs, France
[c] Laboratoire Universitaire de Science Appliquées de Chebourg, France

15:55 Temperature-dependent breakdown and hot carrier stress of PHEMTs

P. Cova, N. Delmonte, G. Sozzi, R. Menozzi
Dipartimento di Ingegneria dell'Informazione, University of Parma, Italy

Break

16:50 On-wafer low frequency noise measurements of SiGe HBTs: Impact of technological improvements on 1/f noise

B. Grandchamp, C. Maneux, N. Labat, A. Touboul, T. Zimmer
IXL Laboratory - CNRS - ENSEIRB, University of Bordeaux, France

Tuesday, October 5

18:00 **Poster Session and Reception Party** Gallery Floor F

A. Assembly Reliability

Influence of the thermo-mechanical residual state on the power assembly modellization

Alexandrine Guédon-Gracia, Pascal Roux, Eric Woirgard, Christian Zardini
Laboratoire IXL - CNRS - ENSEIRB - University of Bordeaux, France

Study of influence of failure modes on lifetime distribution prediction of 1.55 µm DFB Laser diodes using weak drift of monitored parameters during ageing tests

L. Mendizabal[a], L. Bechou[a], Y. Deshayes[a], F. Verdier[a], Y. Danto[a], D. Laffitte[b], J.L. Goudard[b], F. Houé[b]
[a] IXL Laboratory, University of Bordeaux, France
[b] AVANEX-France, France

Comparative study of thermal cycling and thermal shocks tests on electronic components reliability

S. Moreau[ab], T. Lequeu[a], R. Jérisian[a]
[a] LMP, France
[b] STMicroelectronics, France

Integrated thermo-mechanical design and qualification of wafer backend structures

G.Q. Zhang[a] and J. Bisschop[b]
[a] Eindhoven University of Technology and Philips Centre for Industrial Technology, The Netherlands
[b] Philips Semiconductors, The Netherlands

Non destructive control of flip chip packages for space applications

M. Paillard[a], C. Schaffauser[a], C. Drevon[a], J.L. Cazaux[a], H.R. Schubach[b], F. Frese[b]
[a] Alcatel Space, 26 Avenue Champollion, BP1187, F-31037 Toulouse, France
[b] Dantec Ettemeyer GmbH, Kaessbohrer Str. 18, D-89077 Ulm, Germany

B. Failure Analyisis & Advanced Characterization Techniques

Current crowding in faulty MOSFET: optical and electrical investigation

A. Tosi[a], F. Stellari[b], F. Zappa[a]
[a] Politecnico di Milano, Dipartimento di Elettronica e Informazione, Italy
[b] IBM T.J. Watson Research Center, Yorktown Heights – NY 10598 (USA)

Gallium Artefacts on FIB-milled Silicon Samples

Joachim C. Reiner, Philipp Nellen, Urs Sennhauser
EMPA - Electronics/Metrology Laboratory, Switzerland

VCO phase noise improvement through direct passive component modification in the FIB

B. Domengès[a], B. Tiphaigne[b]
[a] LAMIP, laboratoire de microélectronique ISMRA-Philips, France
[b] STEPMIND OUEST, France

Failure analysis of vertical cavity surface emission laser diodes

F. Siegelin
Infineon Technologies, Germany

Failure analysis of RFIC Amplifiers

G. Mura[a], M. Vanzi[a], G. Micheletti[b]
[a] Department of Electric and Electronic Engineering DIEE-INFM , University of Cagliari, Italy
[b] Datalogic S.p.A, Bologna, Italy

Femtosecond Laser Ablation for Backside Silicon Thinning

F. Beaudoin[a], J. Lopez[b], M. Faucon[b], R. Desplats[a], P. Perdu[a]
[a] CNES-THALES Laboratory, France
[b] CELIA-PALA UMR 5107 University of Bordeaux, France

A Novel Automatic Polishing Technique for Micro-Controllers with 450 off Si <100> Rotation

I. Grimberg[a], H. Coulson[b], K. Williamson[b], J. Pohl[b], Z. Shafrir[a], E. Raz[a]
[a] Sagitta Ltd, Israel
[b] ATMEL, United Kingdom

AFM-based scanning capacitance techniques for deep sub-micron semiconductor failure analysis

Guenther Benstetter[a], Peter Breitschopf[a], Werner Frammelsberger[a], Heiko Ranzinger[a], Peter Reislhuber[a], Thomas Schweinboeck[c]
[a] University of Applied Sciences Deggendorf, Germany
[b] University of the West of England, Bristol, United Kingdom
[c] Infineon Technologies, Germany

On the Use of Neural Networks to Solve the Reverse Modelling Problem for the Quantification of Dopant Profiles Extracted by Scanning Probe Microscopy Techniques

Mauro Ciappa[a], Maria Stangoni[a], Wolfgang Fichtner[a], Elisa Ricci[b] and Andrea Scorzoni[b]
[a] Swiss Federal Institute of Technology (ETH) Zurich, Integrated Systems Laboratory, Switzerland
[b] University of Perugia, Faculty of Engineering, Italy

Investigation of SEU sensitivity of Xilinx Virtex II FPGA by pulsed laser fault injections

R. Desplats[a], S. Petit[c], S. Rezgui[d], C. Carmichael[d], P. Fouillat[b], D. Lewis[b]
[a] CNES- French Space Agency, 18, avenue Edouard Belin 31401 Toulouse – France
[b] IXL Laboratory, 351 cours de la Libération, 33405 Talence Cedex – France
[c] CONERA, 2, avenue Edouard Belin, 31400 Toulouse – France
[d] Xilinx, Group HI-REL, Aerospace & Defense Products, USA

Light Emission From Small Technologies. Are Silicon Based Detectors Reaching Their Limits?

M. Remmach[a], R. Desplats[a], P. Perdu[a], J. P. Roux[b], M. Vallet[b], S. Dudit[c], P. Sardin[c], D. Lewis[d]
[a] CNES - French Space Agency, France
[b] NPTest Inc, USA
[c] ST Microelectronics,France
[d] IXL Laboratory, France

Field Failure Mechanism Investigation of GaAs based HBT Power Amplifier Module (PAM)

Jae-Seong Jeong, Jong-Shin Ha, Sang-Deuk Park

Advanced Technology Group, CS Management Center, Samsung, Korea

C. Power Device Reliability

Reliability study of Power RF LDMOS for Radar application

H. Maanane[a], P. Bertram[b], J. Marcon[a], M. Masmoudi[a], M. Belaid[a], K. Mourgues[a], P. Eudeline[b] and K. Ketata[a]
[a] LEMI, University of Rouen, France
[b] THALES Air Defence, France

Experimental characterization of temperature distribution on Power MOS devices during Unclamped Inductive Switching

E. D'Arcangelo, A. Irace, G. Breglio and P. Spirito
Dipartimento di Ingegneria Elettronica e delle Telecomunicazioni,
Università degli Studi di Napoli "Federico II", Italy

Comparison Between the Behaviour of Punch-Through and Non-Punch-Through Insulated Gate Bipolar Transistors Under High Temperature Reverse Bias Stress

C. O. Maiga, H. Toutah, B. Tala-Ighil, B. Boudart
Site Universitaire, LUSAC, Cherbourg-Octeville, France.

Passivation schemes to improve power devices HAST robustness

L. Allirand[a], B. Regairaz[b]

[a] T&M organization ,Technology Solutions, FREESCALE SAS, France

[b] T&M organization, Die Manufacturing MOS20, FREESCALE SAS, France

Enhancement of breakdown voltage for Ni-SiC Schottky diodes utilizing field plate edge termination

T. Ayalew, A. Gehring , T. Grasser, and S. Selberherr

Christian-Doppler-Laboratory for TCAD in Microelectronics, Institute for Microelectronics, TU Vienna, Austria

Compare of SOI and SOS LIGBT structure for the thermal conductivity and self-heating characteristics

J. Y. Kim[a], S. W. Park[a], M. C. Jung[a], C. H. Kim[a], M. Y. Sung[a], D. H. Rhie[b], E. G. Kang[c], N. G. Kim[c], S. C. Kim[d]

[a] Department of Electrical Engineering, Korea University, Korea
[b] Department of Electrical Engineering, Suwon University, Korea
[c] Department of Electronic Enginnering, Far East University, Korea
[d] Korea Electrotechnology Search Institute, Korea

Analysis of wire bond and metallization degradation mechanisms in DMOS power transistors stressed under thermal overload conditions

Th. Detzel, M. Glavanovics, K. Weber

Infineon Technologies Austria AG, Siemensstrasse 2, A-9500 Villach

D. Dielectrics & hot carriers reliability

A new approach to the modeling of oxide breakdown on CMOS circuits

R. Fernández, R. Rodríguez, M. Nafría, X. Aymerich
Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, Spain

Standard and C-AFM tests to study the post-BD gate oxide conduction of MOS devices after current limited stresses.

M. Porti, S. Meli, M. Nafría, X. Aymerich
Dept. Enginyeria Electrònica, Universitat Autònoma de Barcelona, Spain

Time dependent dielectric breakdown in a low-k interlevel dielectric

J.R. Lloyd[a], E. Liniger[a] , S.T. Chen[b]
[a] IBM T.J. Watson Research Center, USA
[b] IBM Microelectronics, USA

On the defects introduced by AC and DC hot carrier stress in SOI PD MOSFETs

M.Exarchos[a], F.Dieudonne[b], J.Jomaah[b], G.J.Papaioannou[a] and F.Balestra[b]
[a] University of Athens, Physics Dept., Solid State Physics Section, Greece
[b] IMEP (UMR CNRS/INPG/UJF), France

Reduced Hot Carrier Effects in Self-Aligned Ground-Plane FDSOI MOSFET's

Se Re Na Yun[a], Chong Gun Yu[a], Seok Hee Jeon[a], Chung Kyue Kim[b], Jong Tae Park[a], and Jean Pierre Colinge[c]
[a] Department of Electronics Engineering, University of Incheon, Korea
[b] Department of Computer Engineering, University of Incheon, Korea
[c] Department of Electrical and Computer Engineering, University of California, USA

E. Device & circuit reliability

A new structure to monitor electrical transients during programming of EEPROM memory cells

N. Baboux[a], C. Plossu[a], P. Boivin[b]
[a] Laboratoire de Physique de la Matière, France
[b] STMicroelectronics, France

Evaluation of STI degradation using temperature dependence of leakage current in parasitic STI MOSFET

Oleg Semenov[a] , Michael Obrecht[b] and Manoj Sachdev[a]
[a] Dept. of Electrical and Computer Engineering, University of Waterloo, Canada
[b] Siborg Systems Inc., 24 Combermere Crescent, Canada

Reliability determination of aluminium electrolytic capacitors by the mean of various methods. Application to the protection system of the LHC

F. Perisse[a], P. Venet[b], G. Rojat[b]
[a] LEA Boulevard Marie & Pierre CURIE, France
[b] CEGELY UCB Lyon, France

Failure Analysis of RuO2 Thick Film Chip Resistors

S.Podda[a], G.Cassanelli[b], F.Fantini[b], M.Vanzi[a]
[a] Department of Electronic Engineering, University of Cagliari, Italy
[b] University of Modena e Reggio Emilia Dipartimento di Ingegneria dell'Informazione, Italy

First step in the reliability assessment of ultracapacitors used as power source in hybrid electric vehicles

W. Lajnef, J.M. Vinassa, S. Azzopardi, O. Briat, C. Zardini
IXL Laboratory, University of Bordeaux, France

F. Electrostatic discharges

Study and validation of a power-rail ESD clamp in BiCMOS process with a reduced temperature dependency of its leakage current

F. Barbier[ae], F. Blanc[a], A. Le Grontec[a], R. Colclaser[b], T. Smedes[c], M. Johnson[d], S. Bardy[a], P. Descamps[e]
[a] Philips Semiconductors Caen, France
[b] Philips Semiconductors Fishkill, USA
[c] Philips Semiconductors Nijmegen, The Netherlands
[d] Philips Semiconductors San Jose, USA
[e] LaMIP, Laboratoire de Microélectronique ENSI Caen-Philips, France

The Failure Analysis of High Voltage Tolerance IO Buffer under ESD

Tao Cheng, Y.S. Shyu
Media Tek Inc., Taiwan

Study of the ESD defects impact on ICs reliability

F. Essely[a], C. Bestory[c], N. Guitard[b], M. Bafleur[b], A. Wislez[c], E. Doche[c], P. Perdu[d], A. Touboul[a], D. Lewis[a]
[a] XL Laboratory, University of Bordeaux, France
[b] LAAS-CNRS, France
[c] LCIE, France
[d] CNES-Thales Laboratory, France

The Impact of CMOS technology scaling on MOSFETs second breakdown: Evaluation of ESD robustness

O. Semenov[a], H. Sarbishaei[a], V. Axelrad[b] and M. Sachdev[a]
[a] Dept. of Electrical and Computer Engineering, University of Waterloo, Canada
[b] Sequoia Design Systems, USA

A case study of ESD failures at random levels: analysis, explanation and solution

T. Wu[ab], T. Smedes[b], J.P. Lokker[b], S-N. Mei[c], J.W. Slotboom[a]
[a] Delft University of Technology, Mekelweg 4, 2628 CD Delft, the Netherlands
[b] Philips Semiconductors, Gerstweg 2, 6534 AE Nijmegen, the Netherlands
[c] Philips Semiconductors, Fishkill, 2070 Route 52, Hopewell Junction, NY, USA

A study of an abnormal ESD failure mechanism and threshold voltage caused by ESD current zapping sequence

Yong-Ha Song, Choong-Kyun Kim, Moo-Young Park, Bum-Suk Kye, Jeong-Il Seo, Dong-Soo Cho, Taek-Soo Kim, Gab-Soo Han
ASIC Development Team, System LSI Division, Semiconductor Business, Samsung, Korea

Wednesday, October 6

Session Power Device Reliability (Pow) Auditorium Maximum

Co-chairs: E. Wolfgang, Siemens, A. Hamidi, ABB

8:30 Reliability of power electronic devices against cosmic radiation-induced failure (INVITED)

G. Soelkner[a], W. Kaindl[b], H.-J. Schulze[a], G. Wachutka[b]
[a] Infineon Technologies, Automotive & Industrial, Germany
[b] Inst. for Physics of Electrotechnology, Munich University of Technology, Germany

9:10 The Role of the Parasitic BJT Parameters on the Reliability of New Generation Power MOSFET during Heavy Ion Exposure

F. Velardi[a], F. Iannuzzo[a], G. Busatto[a], A. Porzio[a], A. Sanseverino[b], G. Currò[c], A. Cascio[c], F. Frisina[c]
[a] D.A.E.I.M.I., Università degli Studi di Cassino, Italy
[b] D.I.E.T., Università degli Studi di Napoli, Italy
[c] ST-Microelectronics, Italy

9:35 Semiconductors in high temperature applications – a future trend in automotive industry

Michael Goroll[a], Reinhard Pufall[a], Werner Kanert[a], Boris Plikat[b]
[a] Infineon Technologies AG, Automotive & Industrial Division, Germany
[b] Infineon Technologies AG, Corporate Assembly & Test Division, Germany

10:00 Analysis of PowerMOSFET chips failed in thermal instability

A. Castellazzi[a], H. Schwarzbauer[b], D. Schmitt-Landsiedel[c]
[a] Institute of Physics of Electrotechnology, Munich University of Technology, Germany
[b] Siemens, Germany
[c] Institute of Technical Electronics, Munich University of Technology, Germany

Break

10:55 Partial Discharge Failure Analysis of AlN Substrates for IGBT Modules

J.-H. Fabian, S. Hartmann, A. Hamidi
ABB Switzerland Ltd, Corporate Research, CH-5405 Baden-Dättwil, Switzerland

11:20 Investigation of IGBT turn-on failure under high applied voltage operation

Masayasu Ishiko[a], Koji Hotta[b], Sachiko Kawaji[a], Takahide Sugiyama[a], Tomoyuki Shouji[a], Takeshi Fukami[b], Kimimori Hamada[b]
[a] Power Device Lab., Toyota Central R&D Labs., Japan
[b] Electronics Engineering Div. III, Toyota Motor Corporation, Japan

11:45 High reliable high power diode for welding applications

P. Cova[a], F. Fasce[b], P. Pampili[b], M. Portesine[b], G. Sozzi[a], P.E. Zani[b]
[a] Dipartimento di Ingegneria dell'Informazione, University of Parma, Italy
[b] POSEICO S.p.A, via N. Lorenzi, 8 - 16152 Genova, Italy

12:10 Analysis and optimisation through innovative driving strategy of high power IGBT performances/EMI reduction trade-off for converter systems in railway applications

G. Busatto[a], L. Fratelli[b], C. Abbate[a], R. Manzo[a], F. Iannuzzo[a]
[a] Dept. of Automation, Electromagnetism, Information Engineering and Industrial Mathematics, University of Cassino, Italy
[b] AnsaldoBreda Spa, Italy

Lunch

Wednesday, October 6

Session Reliability of Dielectrics (Die) Room D 7.2

Chair: G. Groesenecken, IMEC

9:10 The study of TDDB lifetime estimation for thin gate dielectrics (INVITED, Best Paper Award RCJ Symposium)

Takeshi Shigeo, Kazuhiko Suzuki, and Madoka Muta
System LSI Reliability Eng. Gr. System LSI Quality & Reliability Eng. Dept.,
Toshiba Semiconductor Company, Japan

9:35 Mie-Grüneisen Analysis of the Molecular Bonding States in Silica Which Impact Time-Dependent Dielectric Breakdown

J.W. McPherson
Silicon Technology Development, Texas Instruments, USA

10:00 Extraction of the trap distribution responsible for SILCs in MOS structures from measurements and simulations of DC and noise properties

A.Nannipieri[ab], G. Iannaccone[b], F. Crupi[c]
[a] ISE Integrated Systems Engineering AG, Switzerland
[b] Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica,Telecomunicazio ni, Universita' degli Studi di Pisa and IEIIT-CNR, Italy
[c] Dipartimento di Elettronica, Informatica e Sistemistica, University of Calabria, Italy

Break

10:55 Comparison of Oxide Breakdown Progression in Ultra-Thin Oxide SOI and Bulk pMOSFETs (INVITED, Best Paper Award IPFA)

C. T. Chan[a], C. H. Kuo[a], C. J. Tang[a], M. C. Chen[a], T. Wang[a], S. H. Lu[b], H. C. Hu[b], T. F. Chen[b], C. K. Yang[b], M. T. Lee[b], D. Y. Wu[b], J. K. Chen[b], S. C. Chien[b], and S. W. Sun[b]
[a] Department of Electronics Engineering, National Chiao-Tung University, Taiwan
[b] Technology and Process Development Division, UMC, Taiwan

11:20 Plasma Charging Damage Reduction in IC Processing by A Self-balancing Interconnect

Z. Wang[ab], J. Ackaert[b], C. Salm[a], F. G. Kuper[ab], E. De Backer[b]
[a] MESA+ Research Institute / University of Twente, Semiconductor Components Group, The Netherlands
[b] AMI Semiconductor, Belgium

11:45 Effect of Pre-Existing Defects on Reliability Assessment of High-K Gate Dielectrics

G. Bersuker, J. H. Sim, C. D. Young, R. Choi, P. M. Zeitzoff, G. A. Brown, B. H. Lee, R. W. Murto
International SEMATECH,USA

12:10 Reliability of High-K Dielectrics and Its Dependence on Gate Electrode and Interfacial / High-K Bi-Layer Structure

Y. H. Kim[a], R. Choi[a], R. Jha[b], J.. Lee[b], V. Misra[b],and J. C. Lee[a]*
[a] Microelectronics Research Center, Department of Electrical and Computer Engineering, The University of Texas, USA
[b] Dept. of ECE, North Carolina State University, USA
* now with IBM, USA

Lunch

Wednesday, October 6

Session Failure Analysis & Advanced Characterization Techniques (Fa) Auditorium Maximum

Co-chairs: M. Vanzi, University of Cagliari, A. Street, Qualcomm

14:15 Implementation of TRE systems into Emission Microscopes

A. Tosi[a], M. Remmach[b], R. Desplats[b], F. Zappa[a], P. Perdu[b]
[a] Politecnico di Milano, Dipartimento di Elettronica e Informazione, Italy
[b] CNES- French Space Agency, France

14:40 Overcoming Fault Test Coverage with Time-Resolved Emission (TRE) Probing

Steven Kasapi[a] and Bruce Cory[b]
[a] Credence Systems Corporation, 1421 California Circle Milpitas, CA 95035
[b] NVIDIA Corporation, 2701 San Tomas Expressway, Santa Clara, CA 95050

15:05 New trends in the application of Scanning Probe Techniques in Failure Analysis

T. Schweinböck[a], S. Schömann[a] , D. Alvarez[ab] , M. Buzzo[cd], W. Frammelsberger[ef], P. Breitschopf[e], G. Benstetter
[a] Infineon Technologies AG,Germany
[b] IMEC, Belgium
[c] Infineon Technologies AG, Austria
[d] Swiss Federal Institute of Technology (ETH) Zurich, Integrated Systems Laboratory, Switzerland
[e] University of Applied Sciences Deggendorf, Germany
[f] University of the West of England, UK

15:30 Quantitative 3D reconstruction from BS imaging

R. Pintus, S. Podda, F. Mighela and M. Vanzi
University of Cagliari, Department of Electrical and Electronic Engineering, Italy

15:55 Automated Diagnosis and Probing Flow for Fast Fault Localization in IC

D.Martin[a], R.Desplats[b], G.Haller[a], P.Nouet[c], F.Azaïs[c]
[a] ST Microelectronics, Z.I. de Rousset, 13106 Rousset, France
[b] CNES laboratory – bpi 141418, avenue Edouard Belin, 31401 Toulouse, France
[c] LIRMM, University of Montpellier, France

Break

16:50 Magnetic Microscopy for IC Failure Analysis: Comparative Case Studies using SQUID, GMR and MTJ systems

Olivier Crépel[a], Patrick Poirier[a], Philippe Descamps[a], Romain Desplats[b], Philippe Perdu[b], Gérald Haller[c], Abdelhatif Firiti[c]
[a] LaMIP, Philips Semiconductors, France
[b] CNES- French Space Agency, France
[c] ST Microelectronics, France

17:15 Study on electrostatic discharge (ESD) reliability improvement of ZnO-based multilayered chip varistor(MLV)

M. H. Ji, C. H. Choi, B. K. Jang, B. K. Kim
Central R&D Institue, Samsung Electro-Mechanics, Korea

17:40 Fail / Recover / Fail (F/R/F) failure mechanisms new trend

C. Ali, C. Charpentier
Texas Instruments France, France

Wednesday, October 6

Session Hot Carrier Reliability (Hc) Room D 7.2

Chair: N. Stojadinovic, University of Nis

14:15 Negative Bias Temperature Instability in Triple Gate Transistors (INVITED, Best Paper Award IRPS)

Shigenobu Maeda, Jung-A Choi, Jeong-Hwan Yang, You-Seung Jin, Su-Kon Bae, Young-Wug Kim, and Kwang-Pyuk Suh
Technology Development Team, System LSI Division, Samsung Electronics, Korea

14:40 Evidence for source side injection hot carrier effects on lateral DMOS transistors

S. Aresu[b], , W. De Ceuninck[ab], G. Van den bosch[c], G. Groeseneken[cd], P. Moens[e], J. Manca[ab], D. Wojciechowski[e], P. Gassot[e]
[a] Limburgs University Centre, Institute for Materials Research, Belgium
[b] IMEC vzw, division IMOMEC, Belgium
[c] IMEC vzw, Belgium
[d] Katholieke Universiteit Leuven, ESAT Departments, Belgium
[e] AMI Semiconductor Belgium BVBA, Belgium

15:05 Locating hot carrier injection in n-type DeMOS transistors by Charge Pumping and 2D device simulations

F. Bauwens and P. Moens
Technology R&D, AMI Semiconductor Belgium BVBA, Belgium

15:30 Effects of hot carrier and irradiation stresses on advanced excimer laser annealed polycrystalline silicon thin film transistors

D.N. Kouvatsos[a], V. Davidovic[b], G.J. Papaioannou[c], N. Stojadinovic[b], L. Michalas[c], M. Exarchos[c], A.T. Voutsas[d] and D. Goustouridis[a]
[a] Institute of Microelectronics, Greece
[b] Faculty of Electronic Engineering, University of Nis, Serbia and Montenegro
[c] Solid State Section, Physics Department, University of Athens, Greece
[d] LCD Process Technology Laboratory, Sharp Labs of America, Inc., USA

15:55 Effects of hot carrier stress on the RF performance in SOI MOSFETs

Byung-Jin Lee, Kyosun Kim, and Jong-Tae Park
Department of Electronics Engineering, University of Incheon, Korea

Break

18:10 Workshop Power Reliability Auditorium Maximum

Thermal management: How to get rid of the heat?
Coordinators: E. Wolfgang, Siemens AG, Germany
W. Wondrak, Daimler Chrysler, Germany

18:10 Workshop Eufanet Room D 7.2

Submicron 3D localization and imaging
Coordinator: P. Perdu, CNES

Thursday, October 7

Session Electron & Optical Beam Testing, Advanced Techniques (EOBT) Auditorium Maximum

Chair: L. Balk, University of Wuppertal

8:30 Time Resolved Photon Emission Processing Flow for IC Analysis (INVITED)

R. Desplats[a], G. Faggion[a], M. Remmach[a], F. Beaudoin[a], P. Perdu[a], D. Lewis[b]
[a] CNES-Thales lab. French Space Agency, ,France
[b] IXL Laboratory, France

9:10 Testing of Ultra Low Voltage VLSI Chips using the Superconducting Single-Photon Detector (SSPD)

Franco Stellari and Peilin Song
IBM T.J. Watson Research Center, USA

9:35 Interactive and non-destructive verification of SRAM-descrambling with laser

A. Stuffer
Department of Failure Analysis, Infineon AG, Munich

10:00 Understanding the effects of NIR Laser Stimulation on NMOS transistor

A. Firiti[a], F. Beaudoin[b], G. Haller[a], P. Perdu[b], D. Lewis[c], P. Fouillat[c]
[a] ST Microelectronics, 13106 Rousset, France
[b] CNES-Thales laboratory, France
[c] IXL Laboratory, France

Break

10:55 2D Dopant Profiling on 4H Silicon Carbide P+N Junction by Scanning Capacitance and Scanning Electron Microscopy

Marco Buzzo[ab], Markus Leicht[a], Thomas Schweinböck[c], Mauro Ciappa[b], Maria Stangoni[b], Wolfgang Fichtner[b]
[a] Infineon Technologies AG, Villach, Austria
[b] Swiss Federal Institute of Technology (ETH), Integrated Systems Laboratory, Switzerland
[c] Infineon Technologies AG, Munich, Germany

11:20 Transient interferometric mapping of smart power SOI ESD protection devices under TLP and vf-TLP stress

S. Bychikhin[a], V. Dubec[a], D. Pogany[a], E. Gornik[a], M. Graf[b], V. Dudek[b], W. Soppa[c]
[a] Institute for Solid State Electronics, Vienna University of Technology, Austria
[b] Atmel Germany GmbH Theresienstraße 2, 74025 Heilbronn, Germany
[c] FH Osnabrück, FB Elektrotechnik, Albrechtstraße 30, 49076 Osnabrück, Germany

11:45 A laser-based instrument for measuring strain in electronic packages using coherent fibre-bundles

Peter Dias-Lalcaca[a], Erwin Hack[a], Filippo Visintainer[b], Stefano Bernard[b], Urs Sennhauser[a]
[a] Swiss Federal Laboratories for Materials Testing and Research (EMPA), Electronics / Metrology Lab, Switzerland
[b] Centro Ricerche Fiat, CRF, Italy

12:10 Localization of FET Device Performance with Thermal Laser Stimulation

Sanjib K. Brahma[a], Christian Boit[a], Arkadiusz Glowacki[a], H. Suzuki[b]
[a] Berlin University of Technology, Einsteinufer 19, Sekr. E2, D-10587 Berlin, Germany
[b] Hamamatsu Photonics K.K., Japan

Lunch

Thursday, October 7

Session Device, Circuit & MEMs Reliability (DCM) Room D 7.2

Chair: Y. Danto, University of Bordeaux

10:55 Degradation of electrical performance and floating body effect in ultra thin gate oxide FD-SOI n-MOSFETs by 7.5-MeV proton irradiation

K. Hayama[a], K. Takakura[a], H. Ohyama[a], A. Mercha[b], E. Simoen[b], C. Claeys[bc], J.M. Rafi[d] and M. Kokkoris[e]
[a] Kumamoto National College of Technology, Japan
[b] IMEC Leuven, Belgium
[c] Electrical EEngineering Department, KU Leuven, Belgium
[d] Institut de Microelectrònica de Barcelona (CNM-CSIC), Spain
[e] Institute of Nuclear Physics, Tandem Accelerator, Greece

11:20 Reliability Evaluation and Redesign of LNA

Wei-Cheng Lin, Long-Jei Du, Ya-Chin King
Microelectronics Laboratory, Semiconductor Technology Application Research (STAR) Group, Department of Electrical Engineering, National Tsing-Hua University,Taiwan

11:45 Creep as a reliability problem in MEMS

R. Modlinski[ab], A. Witvrouw[a], P. Ratchev[a], A. Jourdain[a], V. Simons[a], H.A.C. Tilmans[a], J.M.J. den Toonder[c], R. Puers2[b] and I. De Wolf[a]
[a] IMEC vzw, Belgium
[b] E. E. Dept of K. U. Leuven, Belgium,
[c] Philips Research Laboratories,The Netherlands

12:10 Impact of the space environmental conditions on the reliability of a MEMS COTS based system

P. Schmitt[ab], X. Lafontan[c], F. Pressecq[a], B. Kurz[a], C. Oudea[d], D. Estève[b], J.Y. Fourniols[b], H. Camon[b]
[a] CNES, bpi 1414, 18, Av. E. Belin, 31401 Toulouse Cedex 9, France
[b] LAAS - CNRS, 7, Av. Col. Roche, 31077 Toulouse Cedex 4, France
[c] Nova MEMS, 14 rue du quai, 09700 Saverdun, France
[d] EADS – ST, 66, route de Verneuil, 78133 Les Mureaux Cedex, France

Lunch

13:30 Departure for Networking Event and Gala Dinner

Meeting Point: ETH Terrace (Side Leonhardstrasse)

Friday, October 8

Session ESD (ESD) Auditorium Maximum

Chair: T. Mouthaan, University of Twente

8:45 Experimental measurements and 3D simulation of the parasitic lateral bipolar transistor triggering within a single finger gg-nMOS under ESD

P.Galy[a], V.Berland[ab], A.Guilhaume[c], F.Blanc[d], J.P.Chante[e]
[a] Pole Universitaire Leonard de Vinci, France
[b] LORE, France
[c] EADS CCR, Centre Commun de Recherche, France
[d] PHILIPS Semiconductor, France
[e] CEGELY INSA Lyon, France

9:10 Low Frequency Noise Measurements for ESD Latent Defect Detection in High Reliability Applications

N. Guitard[a], D. Trémouilles[a], M. Bafleur[a], L. Escotte[a], L. Bary[a], P Perdu[b], G. Sarrabayrouse[a], N. Nolhier[a], R. Reyna-Rojas[b]
[a] LAAS/CNRS, France
[b] CNES, France

9:35 Electrostatic Effects on Semiconductor Tools

P. Jacob[ab], J. C. Reiner[a]
[a] EMPA Swiss Federal Laboratories for Materials Testing and Research, Switzerland
[b] EM Microelectronic Marin SA, Rue des Sors 2-3, CH-2074 Marin, Switzerland

10:00 Multiple-time-instant 2D thermal mapping during a single ESD event

V. Dubec[a], S. Bychikhin[a], M. Blaho[a], M. Heer[a], D. Poganya[a], M. Denison[b], N. Jensen[b], M. Stecher[b], G. Groos[c], E. Gornik[a]
[a] Institute for Solid State Electronics, Vienna University of Technology, Austria
[b] Infineon Technologies, Germany
[c] University of the Federal Armed Forces Munich, Germany

Session Interconnects Reliability (INT) Room D 7.2

Chair: F. Fantini, University of Modena

8:30 Reliability Challenges with Ultra-Low k Interlevel Dielectrics (INVITED)

J.R. Lloyd, M.R. Lane, X.-H. Liu, E. Liniger, T.M. Shaw, C.-K. Hu, R. Rosenberg
IBM T.J. Watson Research Center, Yorktown Heights NY 10598, USA

9:10 Reliability Improvement in Al Metallization: A Combination of Statistical Prediction and Failure Analytical Methodology

G. Zhang[a], C. M. Tan[a], K. T. Tan[b], K. Y. Sim[b], and W. Y. Zhang[b]
[a] Division of Microelectronics, School of EEE, Nanyang Technological University, Singapore
[b] Department of Failure Analysis & Reliability, Systems on Silicon Manufacturing Co., Singapore

9:35 MTF test system with AC based dynamic joule correction for electromigration tests on interconnects

L. Biesemans[ac], K. Schepers[a], K. Vanstreels[a], J. D'Haen[b], W. De Ceuninck[ab], M. D'Olieslaeger[ab]
[a] Institute for Materials Research, Limburgs Universitair Centrum, Belgium
[b] IMEC vzw, division IMOMEC, Wetenschapspark 1, B-3590 Diepenbeek, Belgium
[c] Hogeschool Limburg, Universitaire Campus, Gebouw H, B-3590 Diepenbeek, Belgium

10:00 An improved isothermal electromigration test for Cu-damascene characterization

M. Impronta[a], S. Farris[a], A. Scorzoni[ab]
[a] Istituto per la Microelettronica e Microsistemi (CNR-IMM), Consiglio Nazionale delle Ricerche, Italy
[b] Dipartimento di Ingegneria Elettronica e dell'Informazione, Università di Perugia, Italy

Friday, October 8

Session TCAD for Reliability (TCAD) Auditorium Maximum

Co-chairs: L. Bomholt, ISE AG, M. Stecher, Infineon

10:55 Analysis of the layout impact on electric fields in interconnect structures using finite element method

Changsoo Hong[a], Linda Milor[a], MZ Lin[b]
[a] School of Electrical and Computer Engineering, Georgia Institute of Technology, USA
[b] Taiwan Semiconductor Manufacturing Company, Ltd., Hsin-Chu, Taiwan, R.O.C.

11:20 Characterization of self-heating effects in semiconductor resistors during transmission line pulses.

C. Corvasce[a], M. Ciappa[a], D. Barlini[a], S. Sponton[b], G. Meneghesso[b], W. Fichtner[a]
[a] Swiss Federal Institute of Technology (ETH) Zurich, Integrated Systems Laboratory, Switzerland
[b] University of Padova, Department of Information Engineering, Italy

11:45 Statistical simulation of gate dielectric wearout, leakage, and breakdown

A. Gehring and S. Selberherr
Institute for Microelectronics, Vienna University of Technology, Austria

12:10 A CAD assisted design and optimisation methodology for over-voltage ESD protection circuits

V.Vassilev[ab], V.Vashchenko[c], Ph.Jansen[a], B.-J. Choi[c], A.Concannon[c], J.-J.Yang[c], G.Groeseneken[ab], M.I.Natarajan[a], M.Terbeek[c], P. Hopper[c], M.Steyaert[b], H.E.Maes[ab]
[a] IMEC Leuven, Belgium
[b] KUL, ESAT, Belgium
[c] National Semiconductor Corp., USA

12:35 Closing and BP Award

Registration

Registration either on-line (http://www.iis.ee.ethz.ch) or at the desk.

Administrative secretary of the conference:

Christine Haller
Swiss Federal Institute of Technology (ETH)
Integrated Systems Laboratory
ETH-Zentrum
CH-8092 Zurich, Switzerland

Phone +41 1 632 4268
Fax +41 1 632 1194
Email esref04@iis.ee.ethz.ch

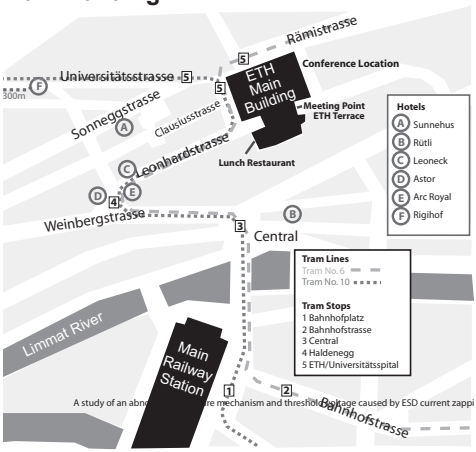
Desk location and opening hours

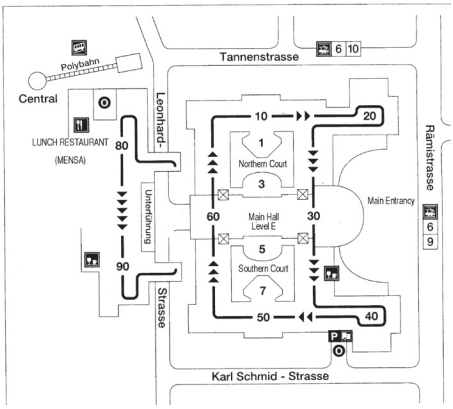
The registration desk is located at the Floor F of the ETH Main Building at the Rämistrasse 101, CH-8092 Zurich. The opening hours of the desk are

Monday, October 4	10:00	-	19:00
Tuesday, October 5	08:00	-	19:00
Wednesday, October 6	08:30	-	19:00
Thursday, October 7	08:30	-	13:30
Friday, October 8	08:30	-	13:00

See the conference homepage for the phone numbers and the email addresses to reach the delegates.

Main Building ETH





Workshops

The access to the workshops is included in the fees.

Best Paper Award Exchange Program

Chair: W. Wondrak, Daimler Chrysler

The recipient of the Best Paper Award will be entitled to present his/her paper either at the International Reliability Physics Symposium (IRPS, USA), or at the Reliability Center of Japan Symposium (RCJ, Japan), or at the International Symposium on Physical and Failure Analysis of Integrated Circuits (IPFA, Singapore) as an invited paper. The ESREF organization covers 1000 Euro for the travelling expenses.

Equipment Exhibition

The access to the equipment exhibition is included in the fees.

Lunch and coffee breaks

The lunches and the coffee breaks mentioned in the Conference schedule are included in the fees.

Lunches will be served before 13:30 in the ETH Mensa (lunch restaurant), which is located within the ETH Main building (side Leonhardstrasse, see map), while coffee breaks will be served in the exhibition area.

Reception party, networking event and gala dinner

The tickets for the reception party, networking event, and for the gala dinner are included in the fees.

The reception party takes place in conjunction with the Poster session in the patio at the Floor F of the ETH Main Building starting at 18:00.

A limited amount of tickets for the networking event and for the gala dinner are also available for companions. Please contact the registration desk before Tuesday Oct. 5, 12:00 to check for price and availability. The meeting point for the networking event and gala dinner is the ETH Terrace (side Leonhardstrasse, see map) at 13:30. Retour to Zurich is planned for 24:00.

Internet access for the delegates

Internet accesses will be available on the conference site for the delegates (room F 33.3).

Author preparation room

Computers are available in the author preparation room (F 33.3) to apply minor corrections to the electronic presentations. All presentations have to be finalized and approved by the audiovisual officer either the evening before the session (for sessions in the morning of the next day), or not later than 3 hours before the beginning of the session (for sessions in the afternoon).