ESD- Testing: HBM to very fast TLP

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Motivation

Closing designs windows and exploding costs for masks and processing require an a-priori understanding of the

- Interaction between the IC and the source of ESD stress
- ESD stress models trying to simulate the "Real World" to catch weak designs
- Implementation and limitations in ESD testers for today's IC qualification tests
- Tools for characterization and parameter extraction during the development of technology and cell library
- Pitfalls, work arounds, and .... perspectives.
Outline

• ESD-related Failure Mechanisms and Reliability
• ESD Stress Test Methods and Phenomena
  – Human Body Model (HBM)
  – Machine Model (MM)
  – System Level HBM (IEC HBM)
  – Charged Device Model (CDM)
  – Socket Discharge Model (SDM)
  – ESD From Outside-To-Surface ESDFOS
• Pulsed Characterization Methods
  – Transmission Line Pulsing TLP
  – Very Fast v-t-TLP
• Summary

ESD-Damage in Integrated Circuits

How to detect a failure or weakness in an integrated circuit?
Electrical signature in parametric and functional tests

Data Sheet Specification
  • Qualification Tests look for Data Sheet only
  • Engineering should go beyond!

Latent Damage

Degraded Parameters
  • Increased Leakage
  • Increased Iddq
  • Threshold Voltage
  • Timing
  • RF & Noise

Reduced Life Time ?

Functional Failure
  • Short
  • Open
  • Stuck-at
Failure Mechanisms in Integrated Circuits

Interconnect Burn-Out
Molten Silicon
Breakdown of gate oxide in transistor

Electrical: Open Short
Leakage nA - µA
Reduced Reliability

ESD Stress: Human Body Model & Machine Model

Just Models!!

Always two pins involved!
HBM acts as current source
MM = Japan driven Worst Case HBM
more sensitive to parasitics of tester and fixture
RLC Discharge Currents HBM, MM

Characterization of HBM-Tester
HBM-Correlation ggNMOS

Influence of test board cap. Cb:
• Slows initial front rise of voltage
• Inhomogeneous triggering of multi finger gg NMOS
• Critical power peak for low failure threshold

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HBM Correlation: Interaction

• Cannot be covered in a standard!
High Pincount Correlation Issue

- Active clamp ineffective for slow voltage rise
- Thin oxides may break down
- IO Negative to VDD

Total C_{Back} = 4.7 nF effective only for IO negative to VDD
Miller Effect increases effective C!

Miller Effect increases effective C!

Voltage Across Active Clamp 0.13 µm

1000V High Leakage  500V Low Leakage
Voltage Across Active Clamp 0.13 μm

Low Leakage Clamp
Turns off

Remedy: Add 10k resistor between pulses!

2 kV Real World HBM Discharge

Voltage across a Zener diode before and during a real world HBM discharge
Correlation Issues (2)

- EOS-like trailing voltage pulse during HBM stress does not turn-on protection causing 6.5 nm GOX degradation and failure of fail-safe inputs

![HBM Voltage Waveform](image)

- Leakage across HV relay

\[ \text{Pre-charge} \quad \text{Start HBM} \quad \text{End HBM} \quad \text{Trailing Pulse} \]

\[ \text{Time (s)} \quad 1.0 \times 10^{-7} \quad 1.0 \times 10^{-6} \quad 1.0 \times 10^{-5} \quad 1.0 \times 10^{-4} \quad 1.0 \times 10^{-3} \quad 1.0 \times 10^{-2} \]

\[ \text{Voltage (Volts)} \quad 12 \quad 8 \quad 4 \]

- Logarithmic Time Scale!

\[ \text{If in any doubt, measure voltage during HBM-test!} \]

High Pin Count Testing

- Pin count of ICs and modules exceeds available number of tester channels (1024 .. 2048)
- Some methods group power pins on an individual test board
- Other methods use different test boards for several subsets of pins
- Different methods already in use by semiconductor manufacturers but still comparative data necessary for standardization.
Three Test Fixture Boards

- TFB-1: All IO-Pins
- TFB-2: All VSS- and VDD-Pins + 1st Group of IO
- TFB-3: All VSS- and VDD-Pins + all other Groups of IO

- Reduction between 5% ... 30%
- High effort for product specific test boards

Ganging Method

- Electrically on-chip connected VSS and VDD pins are connected with the tester terminal via a single trace (Better multiple traces for the ground terminal B)

- Minimum difference to spec
- Pin count reduction between 5% ... 30%
- Test fixture board product specific
Rotational Method

- 4 x n DUT Pins are matched to n tester channels, if in every quarter at least one of each pin types is located.

Only Contacts of 1st quarter connected to tester channels

Pin count reduction by 75%
Complex programming
Sub-Group tests
Socket index may not allow rotation

Split-IO Method

- High reduction of pin count
- May be combined with ganging
- Easy programming
- Minimum of two product specific boards
- IO-Test in only sub groups (Different results possible, if discharge path does not follow protection scheme!)

If necessary
System Level HBM (IEC)

System Level IEC HBM:
Person touching system interface directly connected to an IC with *handheld metal tool* (R \(\ll\) \(\text{C}_{\text{IC}} + \text{C}_{\text{local}}\) with \(R \rightarrow 0\ \Omega\)).

System Level Issues for ICs

- Tendency: IC pins directly connected to high speed system interfaces (USB2.0, antenna, …)
- Cost, form factor, and performance
- More frequently:
  - Cable discharges

→ Extra cost for ICs and potentially unrealistic requirements!
System Level ESD-Generators

ESD- Stress: Charged Device Model CDM

Discharges the device capacitance via 1 Pin
Automated Fabrication: Gravity Feeder
Pick & Place
Tape & Reel
Lead Trim & Form
Lead Scan
Mark Print
...

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**Package Influence in the Charged Device Model**

- Capacitance \( C \)
- Area
- Thickness
- Inductance
  - Length Pin
  - Thickness

\[ C_{CDM} \approx 50 \, \text{pF} \]
\[ L_{CDM} = 0 \, \text{..} 10 \, \text{nH} \]
\[ R_{CDM} \rightarrow 0 \, \Omega \]

**Influence of the Package on the CDM Discharge Current**

<table>
<thead>
<tr>
<th>Package</th>
<th>Time (ns)</th>
<th>Capacitance (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLCC52</td>
<td>250V ATIS</td>
<td>9</td>
</tr>
<tr>
<td>QFP44</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>DIL8</td>
<td>1.6</td>
<td></td>
</tr>
<tr>
<td>SOP8</td>
<td>1.3</td>
<td></td>
</tr>
</tbody>
</table>

Photon \(+50 \text{cm})
Charged Board Model CBM

- Look at Printed Circuit Boards as super large packages!

⇒ Charged Board Model CBM (e.g. Olney EOS/ESD2003)

RLC Discharge Currents and Failure Signatures

- HBM
- IEC
- CDM 500 V
- 4 pf
- MM 500 V
- 5 kV

Energy

Internal Voltage Drop

S G D

HBM, MM
HBM IEC

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Institutsteil München

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ATIS Tutorial 05 ESD: 27

ESREF04 Tutorial 05 ESD: 28
Reliability Issues after CDM

<table>
<thead>
<tr>
<th>60 CDM pre-stressed inputs</th>
<th>50 unstressed reference inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pins</td>
<td>Fail</td>
</tr>
<tr>
<td>20</td>
<td>0</td>
</tr>
<tr>
<td>19</td>
<td>10</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>15</td>
<td>0</td>
</tr>
</tbody>
</table>

Electrical and Physical Failure Signatures:

- \( I_{\text{leak}} < 10 \mu\text{A}, \text{Gateoxide damage input inverter} \)
- \( I_{\text{leak}} > 10 \mu\text{A}, \text{Junction burnout protection element} \)

Gate oxide damage after CDM, but also HC injection, and for metal melting

Electrical limits:

- \(< 500 \text{ V CDM}\)
- \(< 50 \text{ V HBM or other Pulse}\)

Physical damage:

- Polycrystalline, low-ohmic damage
- Transistor with amorphous, high-ohmic damage

TEM after FIB
Charged Device Model CDM Today

- CDM Testers and test standards available
- Discharge current waveforms to calibrate CDM-testers together with metrology chain
- Open Issues:
  - Repeatability
  - Correlation
  - Circuit Model

Field Induced CDM

- POGO PIN
- Down
- Up
- Down
- JEDEC
- Time
- Discharge
- RAPID FCDM CHARGING
- FIELD CHARGING PLATE AT HIGH VOLTAGE (+) BEFORE DUT IS CONTACTED
- SLOW FCDM CHARGING
- DUT IS GROUNDED WHILE VOLTAGE (+) AT FIELD CHARGING PLATE IS INCREASED
- EBDA
- TIME
- Discharge

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Reproducibility of CDM Arc Discharge

- May improve for virgin pogo pin and controlled atmosphere!
- Do not immerse pogo pin into solvent.

Summary of Arc-free Method for CDM-Tester Characterization

- Establish repeatable contact.
- Measure DC-resistance (4 point or 2 point + correction)
- Employ well-known repeatable impulses to characterize impulse response of metrology chain (displayed ≠ measured)
- Employ well-known repeatable impulses to characterize impulse response of CDM-test system including the current transducer
- Carry out discharge experiments only to verify electrical contact performance for arc-discharges.
- Technically well-acknowledged by standardization committee of ESD-Association.
CDM Metrology Characterization: DC & Transmission

<table>
<thead>
<tr>
<th>DC</th>
<th>GP</th>
<th>Rm/Ω</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>0.91</td>
<td></td>
</tr>
<tr>
<td>A1</td>
<td>0.997</td>
<td></td>
</tr>
<tr>
<td>A2</td>
<td>0.998</td>
<td></td>
</tr>
<tr>
<td>A3</td>
<td>1.013</td>
<td></td>
</tr>
<tr>
<td>A4</td>
<td>0.996</td>
<td></td>
</tr>
<tr>
<td>A5</td>
<td>0.919</td>
<td></td>
</tr>
<tr>
<td>A6</td>
<td>0.959</td>
<td></td>
</tr>
</tbody>
</table>

CDM Tester Characterization: Transmission

- Reproducible for the same tester in three years
- Distinguishes two different test systems
Effective Parameters of the Studied CDM-Tester

Equivalent circuit of CDM tester with GP A0 \( R_m = 0.91 \, \Omega \) for height \( d_0 = 4.1 \, \text{mm} \) and \( d_1 = 8.9 \, \text{mm} \) (**)) over the ground plane:

<table>
<thead>
<tr>
<th>Element</th>
<th>Effective Value</th>
<th>Element</th>
<th>Eff.Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L_{POGO} )</td>
<td>3.5 nH</td>
<td>( R_{POGO} )</td>
<td>0.3 ( \Omega )</td>
</tr>
<tr>
<td>( R_{GND, PLANE} )</td>
<td>9.05 ( \Omega ) (17.05 ( \Omega ))</td>
<td>( R_{TESTER} )</td>
<td>2 ( \Omega )</td>
</tr>
<tr>
<td>( C_{GND, PLANE} )</td>
<td>25 pF (20 pF )</td>
<td>( L_{TESTER} )</td>
<td>2.2 ( \mu \text{H} )</td>
</tr>
</tbody>
</table>
CDM Status & Trends

- CDM acknowledged to reproduce field failures that cannot be reproduced by HBM
- Automotive specification AEC-Q100 Rev F2 [www.aecouncil.com](http://www.aecouncil.com) requires CDM qualification, other customers to follow.
- Reproducibility and standardization suffer still from metrology issues and the variations of the arc (spark) in air.

- Arc-free method for the characterization of the CDM-metrology and the CDM-tester proposed

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**Socket Discharge Model SDM**

- Keytek Zapmaster emulates the CDM-event in two steps:
  - A very fast step generated by S propagates along TL to the device at $V_{CDM}$ to address CDM-typical failure signatures
  - the TLs in the background discharge slower via the device
  - improper termination: multiple reflections and excess currents
### Characteristics of SDM

13 pins shorted together and discharge via 1 pin

- Depends strongly on interaction between DUT and tester
- In most cases CDM signature with more damage at lower failure thresholds
- Some companies use SDM for fast screening and CDM for detail work

#### Charged Board Model CBM

- Field failures at IC pins connected to board edge
- HBM and MM did not reproduce field failure
- FCDM tester reproduced field failure signature at –250 V
- Higher energy stored on the board causes more severe failure signature at lower levels
- Inductance of traces may slow discharge
- Tendency to MM, but 1 discharge pin!
- No motion to standardization yet.

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Olney et al. EOS2003
ESD Stress: ESD From Outside-To-Surface ESDFOS

• Direct discharge to top level metal through passivation layer leading to M2/M1-short
• Cannot be reproduced by any standard stress test !!

Stress Test HBM, MM, CDM, SDM, IEC-HBM, ++

• Combination of methods should reproduce the various failure signatures in production and field to identify possible ESD weakness
• Should be repeatable and reproducible
• Must comply to a test standard for comparability
• Typically used for product qualification
• Should be highly efficient in test time

• Yield only failure thresholds: pre-charge voltage
• Complex current waveforms
• Not all failure mechanisms covered yet by standardized stress tests !!
Outline

- ESD-related Failure Mechanisms
- ESD Stress Test Methods
- Pulsed Characterization Methods
  - Introduction
  - Transmission Line Pulsing TLP
  - Very Fast TLP vf-TLP
  - Applications:
    - Turn-on
    - Gate Oxide Breakdown
    - Backside Laser Interferometry
    - Capacitively Coupled TLP cc-TLP
- Summary

ESD Protection and Failure Mechanisms

- Turn-on: voltage, dV/dt, duration
- Failure: voltage, current, duration

To know: Characterize the protection structures and the elements to be protected in the relevant domain!
Design Window for Snapback Protection (ggNMOS)

Gate Oxide Breakdown Voltage = f(t)

Transmission Line Pulses TLP, vf TLP for Pulsed High Current Characterization
Pulsed Characterization TLP, vf-TLP

- Provides quasi-static voltage and current behavior (IV characteristic) in the different ESD domains! (DC failure thresholds are too low for ESD!)
- Identifies the best process split or device design
- Debugs unexpectedly low-failing ICs
- Extracts parameters for device and circuit simulation
- Should comply to standard for comparability
- Pulse source for further analysis tools

Ideally,
- reproduces failure signatures
- correlates with failure threshold of stress test
- provides transient turn-on characteristics (vf-TLP)

Characterization Method:
Transmission Line Pulsing TLP, vf TLP
dV/dt Triggering of 1 µm ggNMOS

Ebeam Prober & Pulse Generators

<table>
<thead>
<tr>
<th>Time t (ns)</th>
<th>VGGNMOS (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>15</td>
<td>15</td>
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<tr>
<td>20</td>
<td>20</td>
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<td>25</td>
<td>25</td>
</tr>
<tr>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>35</td>
<td>35</td>
</tr>
</tbody>
</table>

Voltage clamping of ggNMOS

Kropf, et al ESD-Forum 1993

TLP Systems

- TLP500 Current Source
- TDR TLP50 Time Domain Reflectometer
- TDT Time Domain Transmission
- TDTR Time Domain Transmission Reflectometer

Source Impedance

TLP Systems: TLP500 Current Source

Minimize Parasitics!!
Maximal 5 cm to DUT

TLP square pulse generator Zo= 50 Ω

- Important for snapback devices with high breakdown voltages and low holding voltages!!

Time Domain Reflectometer TLP50

- Constant impedance from generator to DUT
- Rise time filters may be added
Pulse at a Discontinuity

Transmission Line $Z_0$

1) Matched $Z_L = Z_0$

2) Open $Z_L >> Z_0$

3) Short $Z_L = 0 \, \Omega$

Example: $gg$NMOS

Principle of the Very Fast TLP

Transmission Line with Impedance $Z_0$

$V_{\text{incident}}$

$V_{\text{transmitted}}$

$V_{\text{refl}}$

$V(s)$

$1 : n$

$0 < Z_{\text{DUT}} < Z_0$

$V_{\text{DUT}} = V_{\text{incident}} + V_{\text{refl}}$

$I_{\text{DUT}} = (V_{\text{incident}} - V_{\text{refl}}) / Z_0$
**Separated versus Overlaid Pulses**

- Overlapping technique for longer pulse (e.g., 100 ns) duration only
- Requires very flat pulse roof, additional current probe, and oscilloscope channel

1) Measure $V(t)$

2) Cut and shift to compute $V(t)$ & $I(t)$

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**Controlled Impedance for vf-TLP**

- Delay Line TL3 with RF-Coplanar Probe e.g.: Cascade ACP40
- Individual ground pads of DUTs!
- Pad pitch matches wafer probe!
- Additional pads and DC-needles for gate or substrate bias
5 Step Calibration of the vf-TLP: Step 1

- Calibrate for length of TL3 including test fixture
- Measure time delay between half height of the rising edges of the initial and the reflected pulse for short or open.
- Time delay used by algorithm for shifting the reflected pulse left over the incident.
- Direct influence on measured transient!

5 Step Calibration of the vf-TLP: Step 2, 3 and 4

Load Resistance OK!

Courtesy of BEI
5 Step Calibration of the vf-TLP: Step 5

- Absolute DUT voltage: Zener breakdown voltage
- Known Voltage + Resistive Load $R = 5 \, \Omega$: Absolute DUT Current
- NO TRANSIENT DATA!
- Optional for TLP500 Systems

Further Issues

- Variable contact resistance for low-ohmic structures
  - Kelvin Probes (Grund 2003)
- Best time resolution of sampling single shot oscilloscope 50 ps/pt
- Losses and dispersion deteriorate rising edge on long cables.
- Overlay uncertainty limits timing accuracy
Applications of the vf-TLP

- Addresses the CDM-domain well for two terminal structures
  Turn on of protection elements and breakdown of gate oxides

- Helps in CDM troubleshooting of ICs
- Reference for the calibration of device simulators
- Drives DUTs for analysis by
  Backside Laser Interferometry and Emission Microscopy
- Drives Capacitively Coupled-TLP (cc-TLP) setup to apply CDM-like single pin stress
**vf TLP: Turn-on of gg NMOS**

- Turn-on time and holding voltage increase with gate length

**Shooting CDM Trouble of Input**

- Higher turn-on voltage for short pulses critical for gate oxides!!
Backside Laser Interferometer (BLI)

- Method applied to deep sub micron technologies, too.

BLI: Temperature & Free Carrier Density

Temperature

Free Carrier Density

- Method applied to deep sub micron technologies, too.
Do NOT expect Correlation between vf-TLP and CDM for ICs, but Valuable for 2Pin-Structures!!

Different current paths result in different failure thresholds.

Capacitively Coupled TLP (cc-TLP)

Arc-free single pin stress
Square pulses from vf-TLP injected into Cb across DUT generate CDM like voltage across GOX.
Correlation of Withstand Currents

0.13 µm CMOS

- Good correlation for simple CDM-relevant IO-circuits on package emulator

Comparison CDM cc-TLP

- Wider pulses explain lower threshold
- Correlation in physical failure signature
Summary (1)

- HBM – μs pre-pulses and trailing pulses critical for actively clamped circuits.
- HBM – background capacitance relevant for protection efficiency
- MM almost dormant in standardization
- Issues with interpretation of ringing and high pin count devices
- Further growing importance of CDM
- Arc-free characterization method should help to improve correlation
- Charged Board Model emerges for reproduction of failures on board and module level
- ESD-from-Outside-to Surface: A new failure mechanism not reproduced by standard tests
- How far can ICs cope directly with System Level stress?

Summary (2)

- TLP well-established as a characterization tool during development and trouble shooting
- ESD Association develops standard test method for 100 ns TLP to address the HBM/MM domain.
- vf-TLP (Gieser ESD96) accepted to address the CDM-domain
- TLP sources pulses for BLI, EMMI and cc-TLP studies
- Both 50 Ω and 500 Ω have their field of application
- When will a combination of TLP tests replace today’s qualification tests with more or less reproducible RLC discharge waveforms?
Acknowledgements

Cordial Thanks

• to my management and my team,
in particular to: Henry Wolf, ESD Senior Scientist

• to the members of the standardization group for Device Testing of the
ESD Association.

• to our project partners from industry and academia.

• to the German Federal Ministry for Education and Research
and the European Community for funding.

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- ESD Association’s ANSI Standard Test Methods www.osda.org
  (HBM, MM, CDM, SDM, TLP, Glossary of Terms)
- JEDEC Test Methods: www.jedec.org
  (HBM, MM, FCDM)
- Automotive Electronics Council (AEC): AEC-Q100 Rev F www.aecomital.com
  (HBM, MM, FCDM)