ESD- Testing: HBM to very fast TLP

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Motivation

Closing designs windows and exploding costs for masks and processing require an a-priori understanding of the

- Interaction between the IC and the source of ESD stress
- ESD stress models trying to simulate the “Real World” to catch week designs
- Implementation and limitations in ESD testers for today’s IC qualification tests
- Tools for characterization and parameter extraction during the development of technology and cell library

- Pitfalls, work arounds, and …. perspectives.

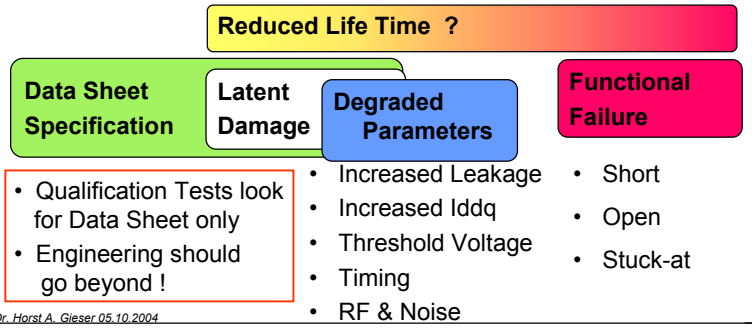
Outline

- ESD-related Failure Mechanisms and Reliability
- ESD Stress Test Methods and Phenomena
  - Human Body Model (HBM)
  - Machine Model (MM)
  - System Level HBM (IEC HBM)
  - Charged Device Model (CDM)
  - Socket Discharge Model (SDM)
  - ESD From Outside-To-Surface ESDFOS
- Pulsed Characterization Methods
  - Transmission Line Pulsing TLP
  - Very Fast vf-TLP
- Summary

ESD-Damage in Integrated Circuits

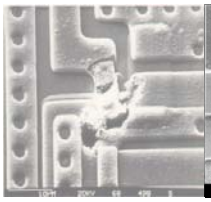
How to detect a failure or weakness in an integrated circuit ?

Electrical signature in parametric and functional tests

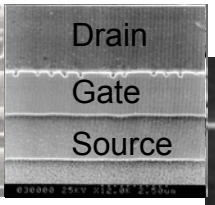


Failure Mechanisms in Integrated Circuits

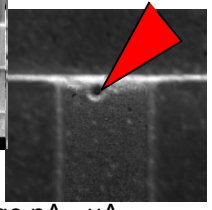
Interconnect Burn-Out



Molten Silicon



Breakdown of gate oxide in transistor

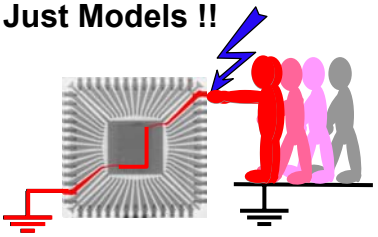


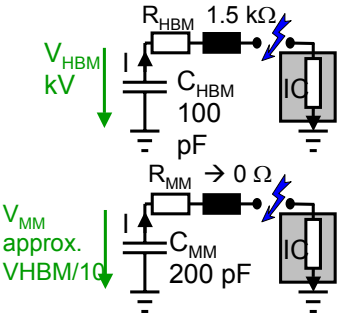
Electrical: Open Short

Leakage nA - µA
Reduced Reliability...

ESD Stress: Human Body Model & Machine Model

Just Models !!



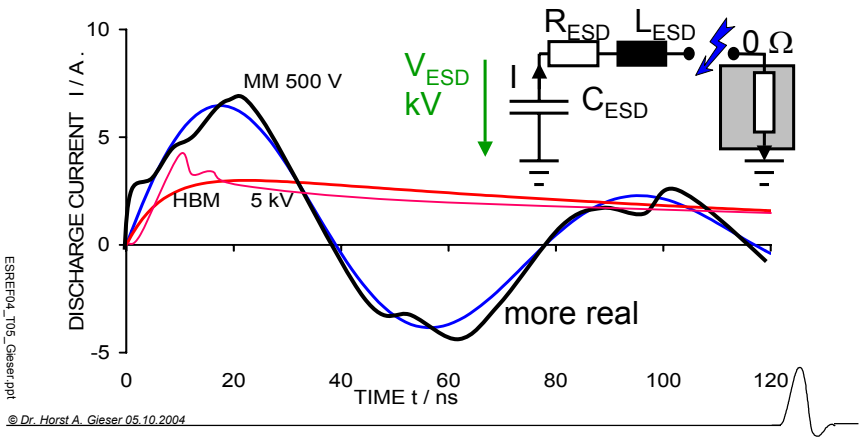


Always two pins involved !

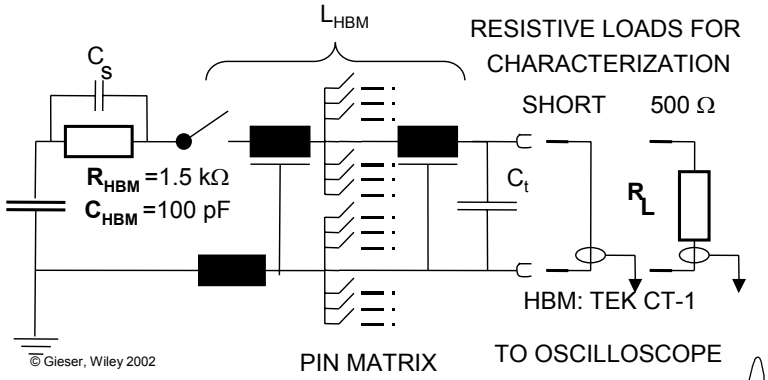
HBM acts as current source

MM = Japan driven Worst Case HBM
more sensitive to parasitics of tester and fixture

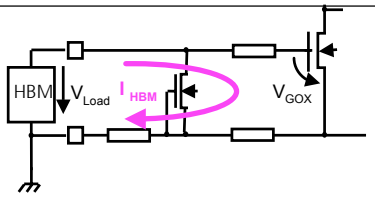
RLC Discharge Currents HBM, MM



Characterization of HBM-Tester

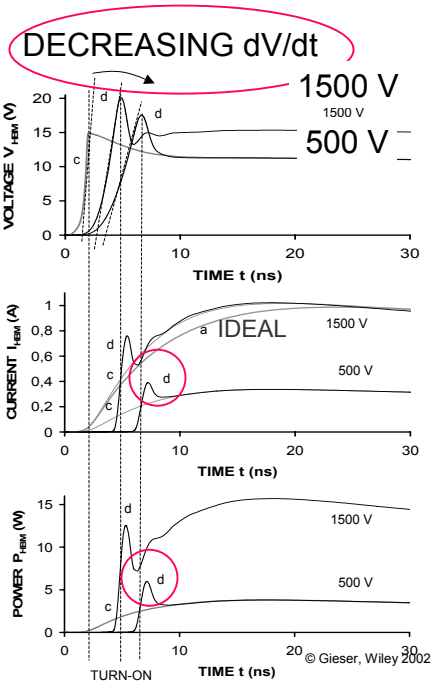


HBM-Correlation ggNMOS



Influence of test board cap. C_B:

- Slows initial front rise of voltage
- Inhomogeneous triggering of multi finger gg NMOS
- Critical power peak for low failure threshold



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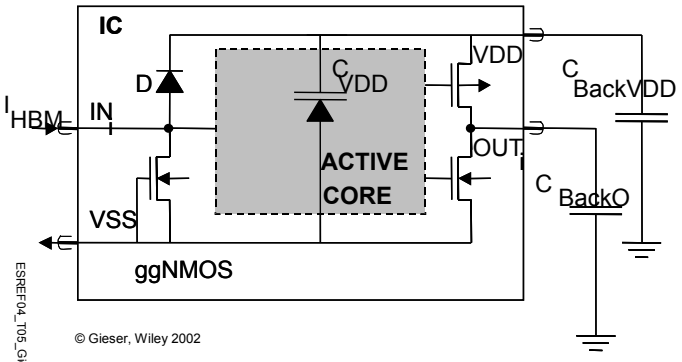
HBM Correlation: Interaction



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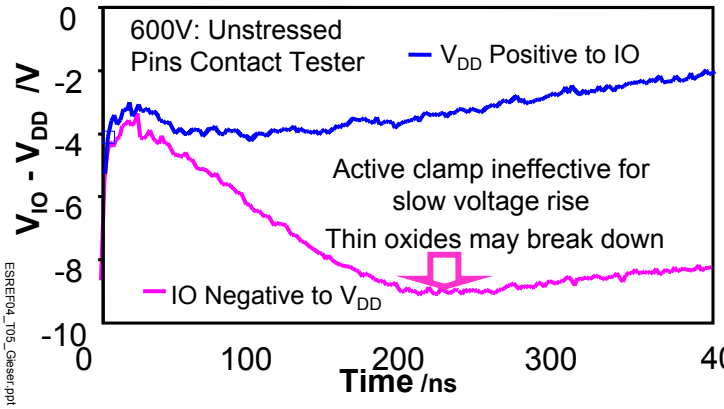
- Cannot be covered in a standard !

High Pincount Correlation Issue



Total C_{Back} = 4,7 nF effective only for IO negative to VDD

Miller Effect increases effective C !

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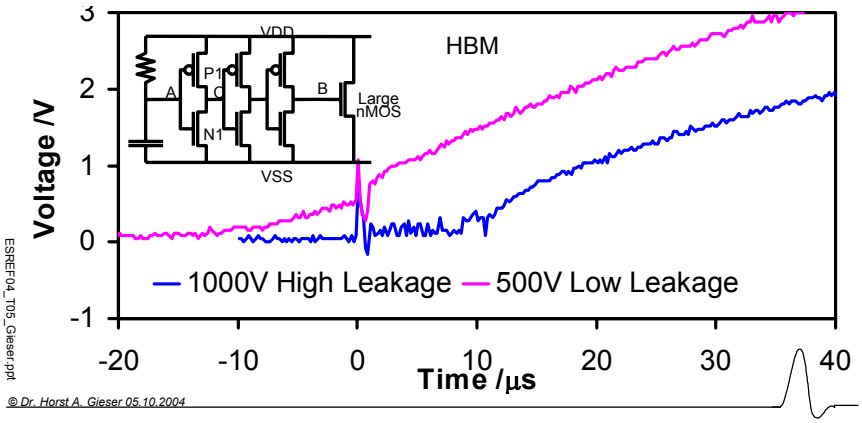
Kunz et al. EOS2004

Voltage Across Active Clamp 0.13 µm



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R.A. Ashton EOS2004
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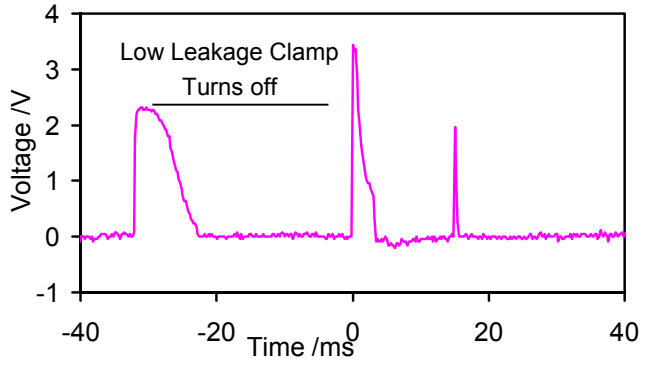
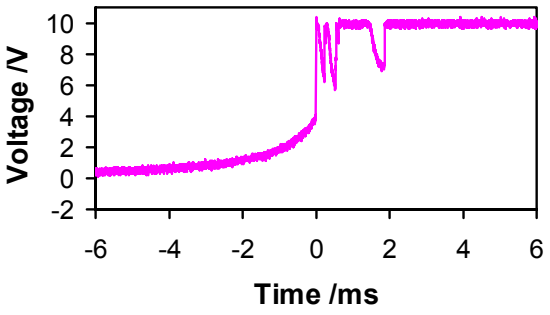
Voltage Across Active Clamp 0.13 µm



1800 V HBM

Remedy: Add 10k resistor between pulses !

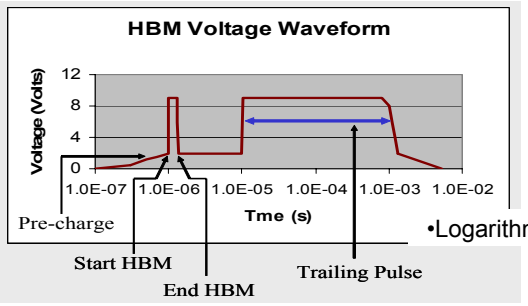
2 kV Real World HBM Discharge



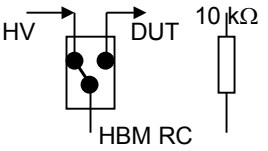
- Voltage across a Zener diode before and during a real world HBM discharge

Correlation Issues (2)

- EOS-like trailing voltage pulse during HBM stress does not turn-on protection causing 6.5 nm GOX degradation and failure of fail-safe inputs



Leakage across HV relay



•Logarithmic Time Scale !

→ If in any doubt, measure voltage during HBM-test !

Duvvury et al. EOS2004
Meuse et al. EOS2004

High Pin Count Testing

- Pin count of ICs and modules exceeds available number of tester channels (1024 .. 2048)
- Some methods group power pins on an individual test board
- Other methods use different test boards for several subsets of pins

- Different methods already in use by semiconductor manufacturers but still comparative data necessary for standardization.

Three Test Fixture Boards

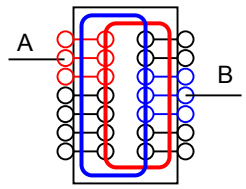
- TFB-1: All IO-Pins
- TFB-2: All VSS- and VDD-Pins + 1st Group of IO
- TFB-3: All VSS- and VDD-Pins + all other Groups of IO

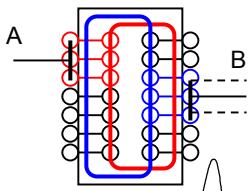
- Reduction between 5% …30 %
- High effort for product specific test boards

Ganging Method

- Electrically on-chip connected VSS and VDD pins are connected with the tester terminal via a single trace
  (Better multiple traces for the ground terminal B)

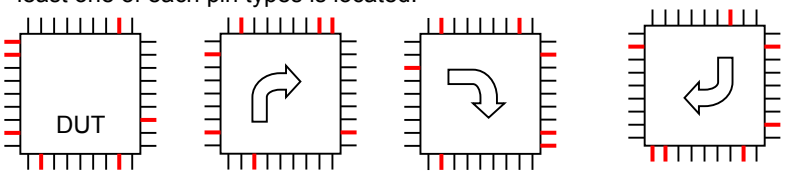
- Minimum difference to spec
- Pin count reduction between 5% …30 %
- Test fixture board product specific

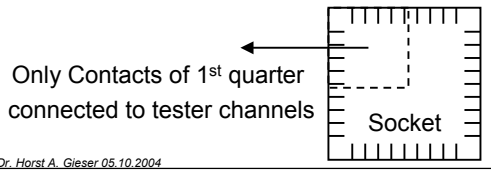




Rotational Method

- 4 x n DUT Pins are matched to n tester channels, if in every quarter at least one of each pin types is located.

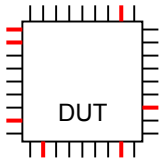


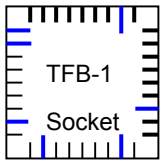


- Universal TFB
- Pin count reductoion by 75 %
- Complex programming
- Sub-Group tests
- Socket index may not allow rotation

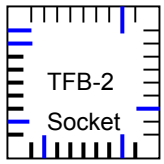
Split-IO Method

- High reduction of pin count
- May be combined with ganging
- Easy programming
- Minimum of two product specific boards
- IO-Test in only sub groups (Different results possible, if discharge path does not follow protection scheme !)

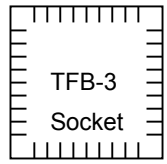




All supply pins
+ 1st group of IO

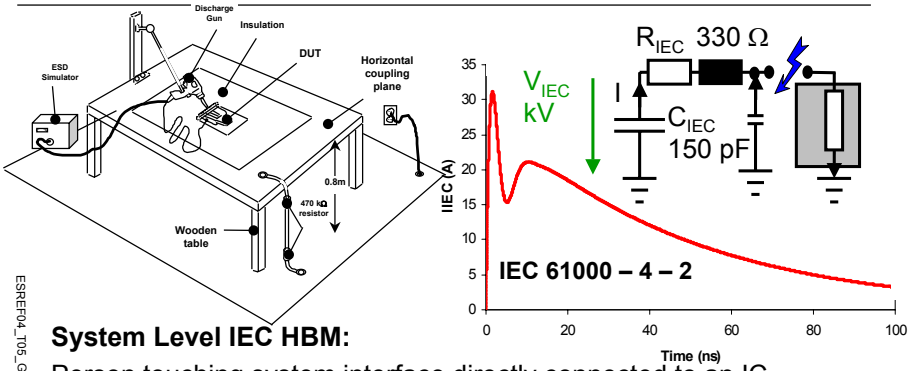


All supply pins
+ 2nd group of IO



If necessary
All supply pins
+ 3rd group of IO

System Level HBM (IEC)

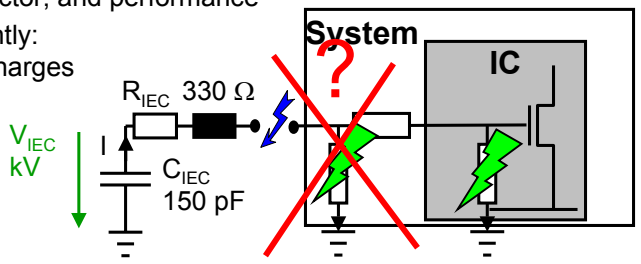


System Level IEC HBM:

Person touching system interface directly connected to an IC with **handheld metal tool** (R ↘; C↗+ C_local with R → 0 Ω).

System Level Issues for ICs

- Tendency: IC pins directly connected to high speed system interfaces (USB2.0, antenna,…)
- Cost, form factor, and performance
- More frequently:
  Cable discharges

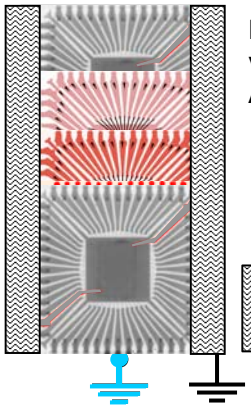


→ Extra cost for ICs and potentially unrealistic requirements !

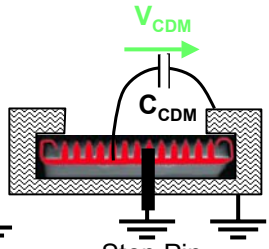
System Level ESD-Generators

ESREF04_T05_Gieser.ppt

ESD- Stress: **Charged Device Model CDM**



Discharges the device capacitance
via 1 Pin
Automated Fabrication: Gravity Feeder
- Pick & Place
- Tape & Reel
- Lead Trim & Form
- Lead Scan
- Mark Print
- ...



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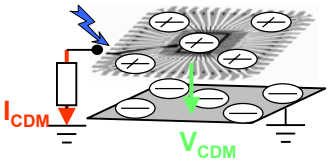
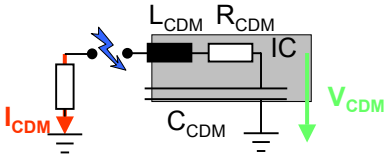
Package Influence in the Charged Device Model

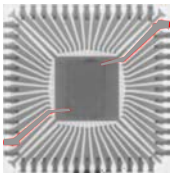




- Capacitance C
  - Area
  - Thickness
- Inductance
  - Length Pin
  - Thickness

C_{CDM} 1 .... 50 pF
L_{CDM} 0 .... 10 nH
R_{CDM} → 0 Ω

PLCC52



20 mm

DIL8 SOP8

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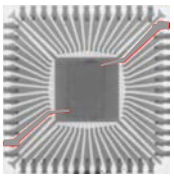
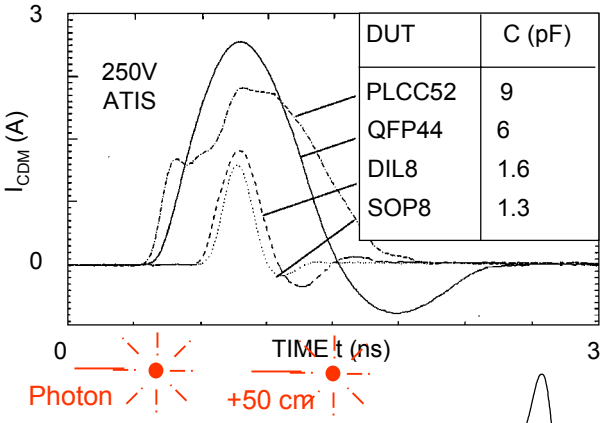
Influence of the Package on the CDM Discharge Current

PLCC52



20 mm

DIL8 SOP8



DUT	C (pF)
PLCC52	9
QFP44	6
DIL8	1.6
SOP8	1.3

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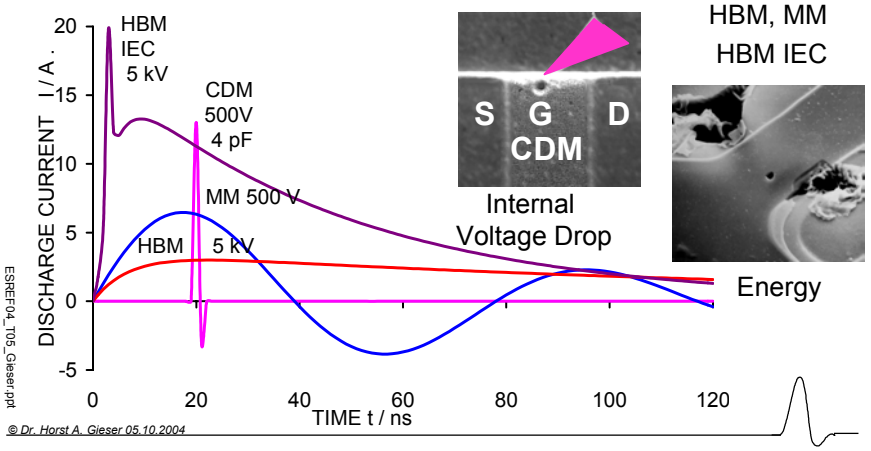
Charged Board Model CBM

- Look at Printed Circuit Boards as super large packages !

→ **C**harged **B**oard **M**odel CBM (e.g. Olney EOS/ESD2003)

RLC Discharge Currents and Failure Signatures



Reliability Issues after CDM

60 CDM pre-stressed inputs					50 unstressed reference inputs		
Pins		Fail	Stress Test	Fail	Pins	Stress Test	Fail
20		0	Dyn. LT 100h	**3**	13	Dyn. LT 100h	0
19		10	Static LT 3h	**4**	18	Static LT 3h	0
6		0	V-Ramp to 14V	**6**	16	V-Ramp to 16V	0
15		0	**HBM < 50 V**	**15**	3	HBM > 1300V	1
Electrical and Physical Failure Signatures:							
I_{leak} << 10 µA, Gateoxide damage input inverter					I_{leak} >> 10 µA; Junction burnot protection element		

Gieser, Reiner et al ESREF1993

Gate oxide damage after CDM,
but also HC injection, and for metal melting

Gieser93, Reiner95
Reiner00, Sherry03

Gate Oxide Damage after CDM

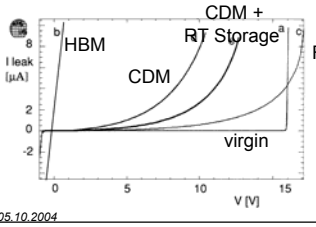
< 500 V CDM

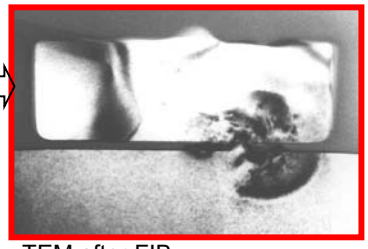
< 50 V HBM
or other Pulse

Polycrystalline, low-ohmic damage

MOS- Input -transistor

Transistor with amorphous, high-ohmic damage

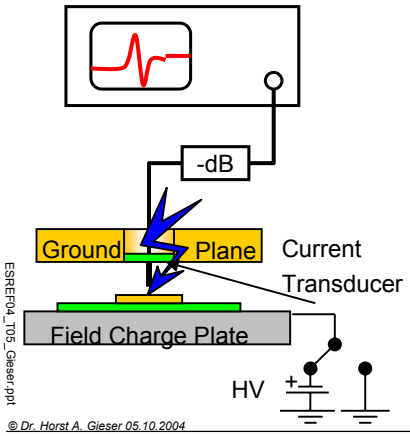




TEM after FIB

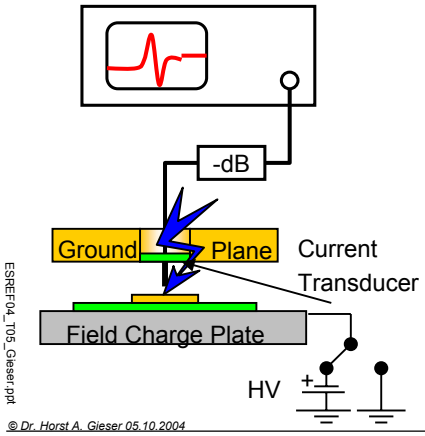
J. Reiner EOS95
H. Gieser et. al. ESREF93

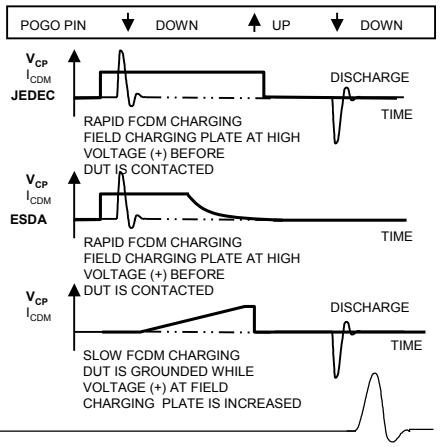
Charged Device Model CDM Today



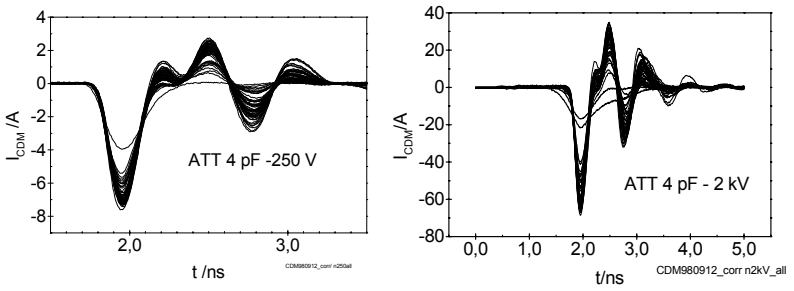
- CDM Testers and test standards available
- Discharge current waveforms to calibrate CDM-testers together with metrology chain
- Open Issues:
  - Repeatability
  - Correlation
  - Circuit Model

Field Induced CDM





Reproducibility of CDM Arc Discharge



- May improve for virgin pogo pin and controlled atmosphere !
- Do not immerse pogo pin into solvent.

ESREF04_T05_Gieser.ppt

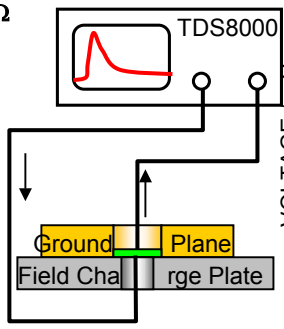
Summary of Arc-free Method for CDM-Tester Characterization

- Establish repeatable contact.
- Measure DC-resistance (4 point or 2 point + correction)
- Employ well-known repeatable impulses to characterize impulse response of **metrology chain (displayed =? measured)**
- Employ well-known repeatable impulses to characterize impulse response of **CDM-test system including the current transducer**
- Carry out discharge experiments only to verify electrical contact performance for arc-discharges.
- Technically well-acknowledged by standardization committee of ESD-Association.

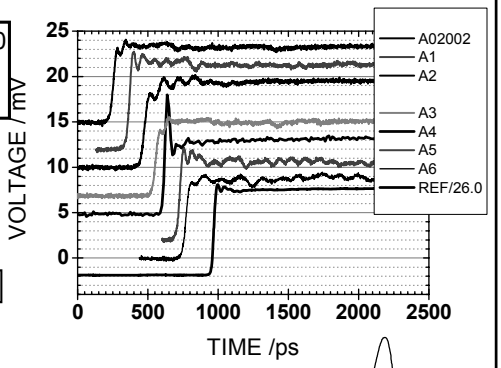
ESREF04_T05_Gieser.ppt

CDM Metrology Characterization: DC & Transmission

GP	DC Rm/ Ω
A0	0.91
A1	0.997
A2	0.998
A3	1.013
A4	0.996
A5	0.919
A6	0.959



Face to Face

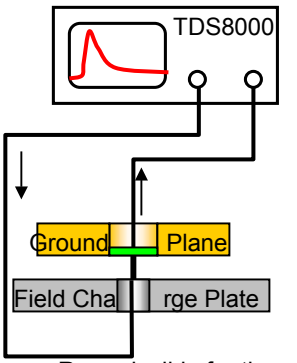


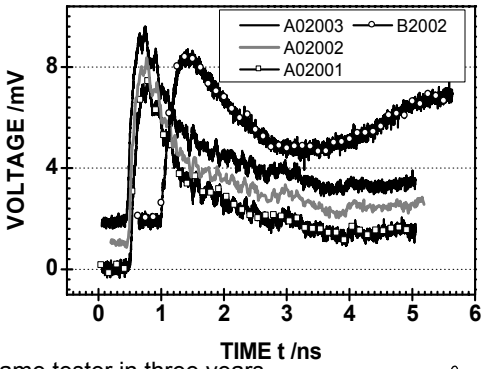
ATIS Analysis & Test of Integrated Systems

Fraunhofer Institut Zuverlässigkeit und Mikrointegration Institutsteil München

Gieser et al. EOS2003

CDM Tester Characterization: Transmission





- Reproducible for the same tester in three years
- Distinguishes two different test systems

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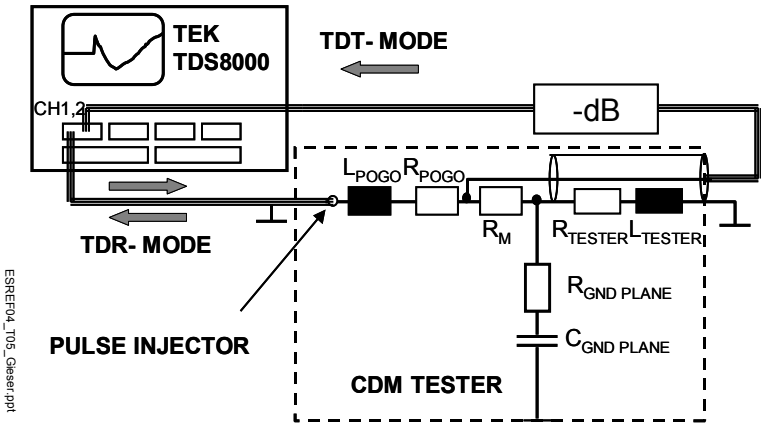
Fraunhofer Institut Zuverlässigkeit und Mikrointegration Institutsteil München

Gieser et al. EOS2003

CDM Tester Model for Simulation

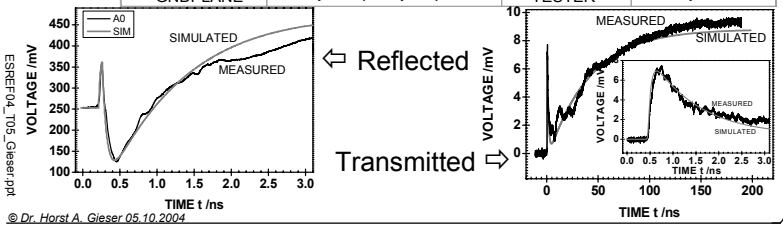


ESREF04_T05_Gieser.ppt

Effective Parameters of the Studied CDM-Tester

Eqivalent circuit of CDM tester with GP A0 R_m= 0.91 Ω for height d_0 = 4.1 mm and d_1 = 8.9 mm (**) over the ground plane:

Element	Effective Value	Element	Eff.Value
L_{POGO}	3.5 nH	R_{POGO}	0.3 Ω
$R_{GNDPLANE}$	9.05 Ω (17.05 Ω)	R_{TESTER}	2 Ω
$C_{GNDPLANE}$	25 pF (20 pF)	L_{TESTER}	2.2 µH

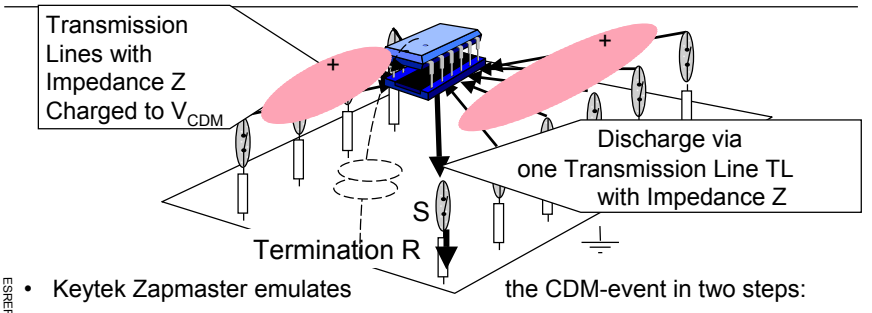


ESREF04_T05_Gieser.ppt

CDM Status & Trends

- CDM acknowledged to reproduce field failures that cannot be reproduced by HBM
- Automotive specification AEC-Q100 Rev F2 www.aecouncil.com requires CDM qualification, other customers to follow.
- Reproducibility and standardization suffer still from metrology issues and the variations of the arc (spark) in air.
- Arc-free method for the characterization of the CDM-metrology and the CDM-tester proposed

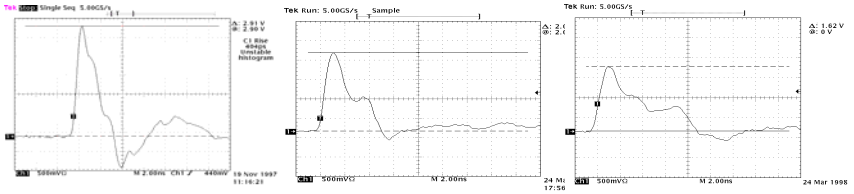
Socket Discharge Model SDM



- Keytek Zapmaster emulates the CDM-event in two steps:
  - A very fast step generated by S propagates along TL to the device at V_{CDM} to address CDM-typical failure signatures
  - the TLs in the background discharge slower via the device
  - improper termination: multiple reflections and excess currents

Characteristics of SDM

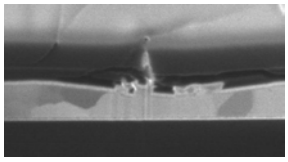
13 pins shorted together and discharge via 1 pin



32 pin TFB 256 pin TFB 512 pin TFB

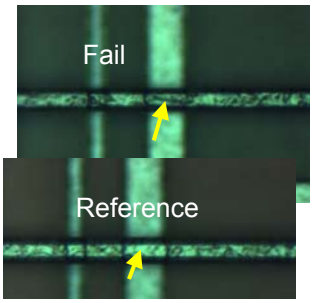
- Depends strongly on interaction between DUT and tester
- In most cases CDM signature with more damage at lower failure thresholds
- Some companies use SDM for fast screening and CDM for detail work

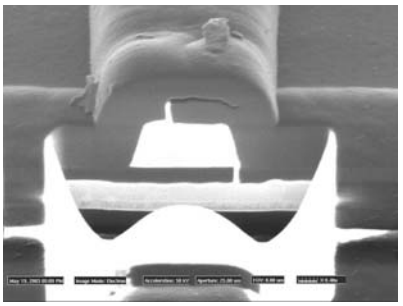
Charged Board Model CBM



- Field failures at IC pins connected to board edge
- HBM and MM did not reproduce field failure
- FCDM tester reproduced field failure signature at –250 V
- Higher energy stored on the board causes more severe failure signature at lower levels
- Inductance of traces may slow discharge
- Tendency to MM, but 1 discharge pin!
- No motion to standardization yet.

ESD Stress:
ESD From Outside-To-Surface ESDFOS





- Direct discharge to top level metal through passivation layer leading to M2/M1-short
- Cannot be reproduced by any standard stress test !!

Stress Test HBM, MM, CDM, SDM, IEC-HBM, ++

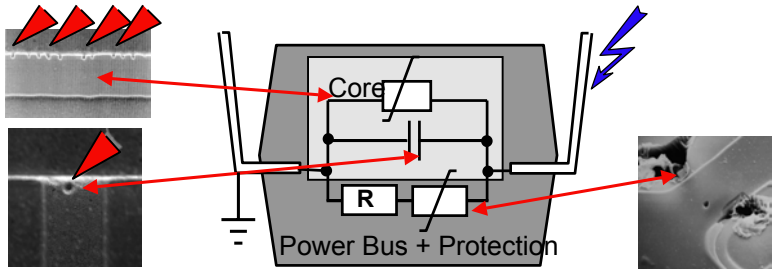
- Combination of methods should reproduce the various failure signatures in production and field to identify possible ESD weakness
- Should be repeatable and reproducible
- Must comply to a test standard for comparability
- Typically used for product qualification
- Should be highly efficient in test time

- Yield only failure thresholds: pre-charge voltage
- Complex current waveforms
- Not all failure mechanisms covered yet by standardized stress tests !!

Outline

- ESD-related Failure Mechanisms
- ESD Stress Test Methods
- Pulsed Characterization Methods
  - Introduction
  - Transmission Line Pulsing TLP
  - Very Fast TLP vf-TLP
  - Applications:
    Turn-on
    Gate Oxide Breakdown
    Backside Laser Interferometry
    Capacitively Coupled TLP cc-TLP
- Summary

ESD Protection and Failure Mechanisms

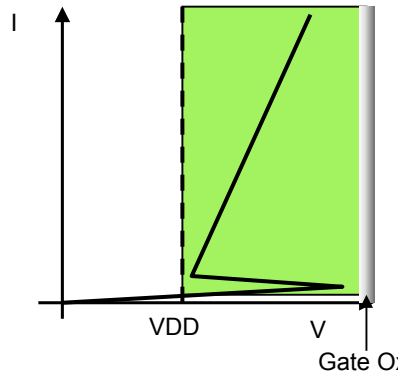


ESD can force each of the three pathes into conduction and fail !

- Turn-on: voltage, dV/dt, duration
- Failure: voltage, current, duration

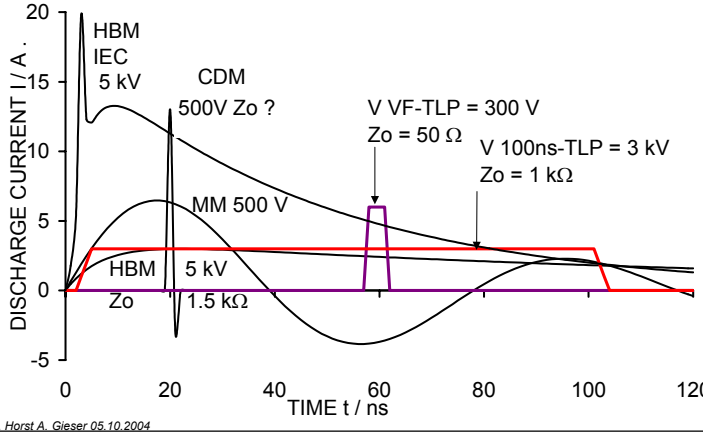
To know: Characterize the protection structures and the elements to be protected in the relevant domain!

Design Windowfor Snapback Protection (ggNMOS)



Gate Oxide Breakdown Voltage = f(t)

Transmission Line Pulses TLP, vf TLP for Pulsed High Current Characterization



Pulsed Characterization TLP, vf-TLP

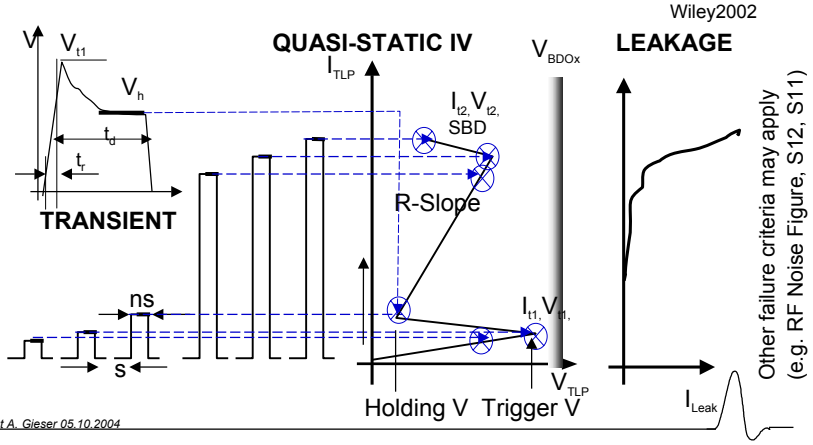
- Provides quasi-static voltage and current behavior (IV characteristic) in the different ESD domain**S !** (DC failure thresholds are to low for ESD!)
- Identifies the best process split or device design
- Debugs unexpectedly low failing ICs
- Extracts parameters for device and circuit simulation
- Should comply to standard for comparability
- Pulse source for further analysis tools

Ideally,

- reproduces failure signatures
- correlates with failure threshold of stress test
- provides transient turn-on characteristics (vf-TLP)

Characterization Method: Transmission Line Pulsing TLP, vf TLP

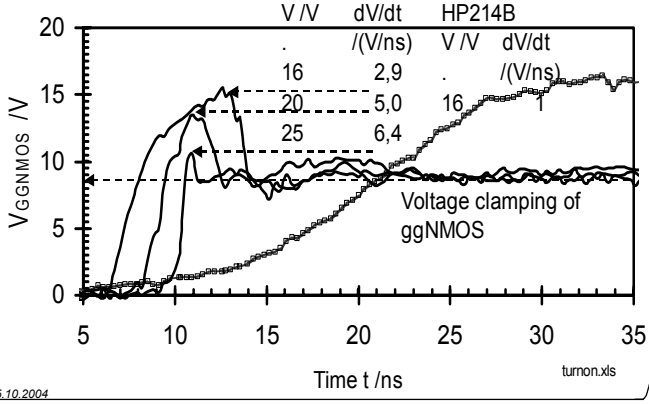
Wiley2002



Maloney 1985, Gieser 1996, Hyvonen 2003

dV/dt Triggering of 1 µm ggNMOS

Ebeam Prober & Pulse Generators



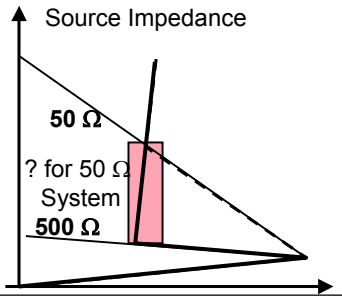
ATIS Analysis & Test of Integrated Systems

Fraunhofer IZM Institut Zuverlässigkeit und Mikrointegration Institutsteil München

Kropf, et al ESD-Forum 1993

TLP Systems

- TLP500 Current Source
- TDR TLP50 Time Domain Reflectometer
- TDT Time Domain Transmission
- TDTR Time Domain Transmission Reflectometer



ATIS Analysis & Test of Integrated Systems

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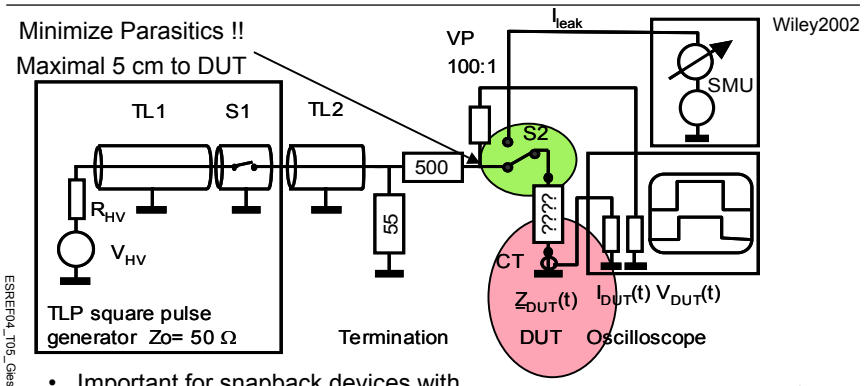
Gieser 2002, Voldman 2003, Grund 2003

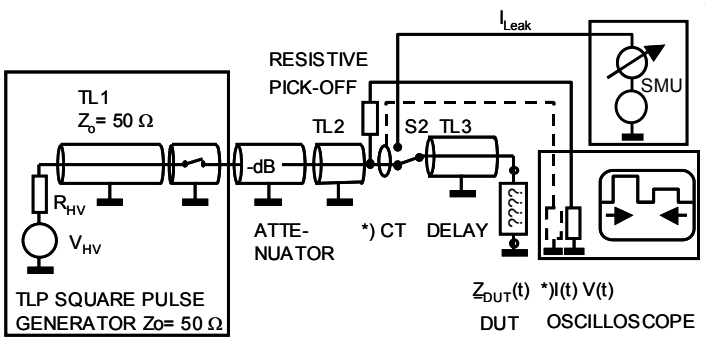
TLP Systems: TLP500 Current Source



- Important for snapback devices with high breakdown voltages and low holding voltages !!

ESREF04_T05_Gieser.ppt

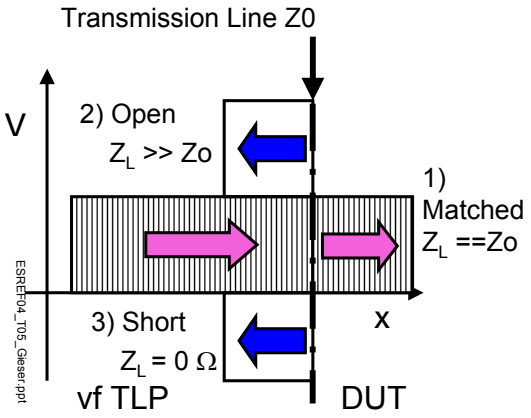
Time Domain Reflectometer TLP50



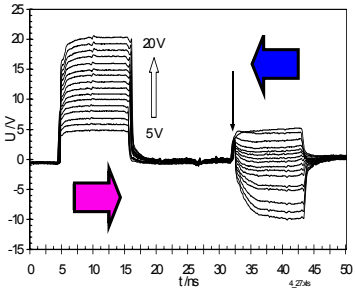
- Constant impedance from generator to DUT
- Rise time filters may be added

ESREF04_T05_Gieser.ppt

Pulse at a Discontinuity



Example: ggNMOS



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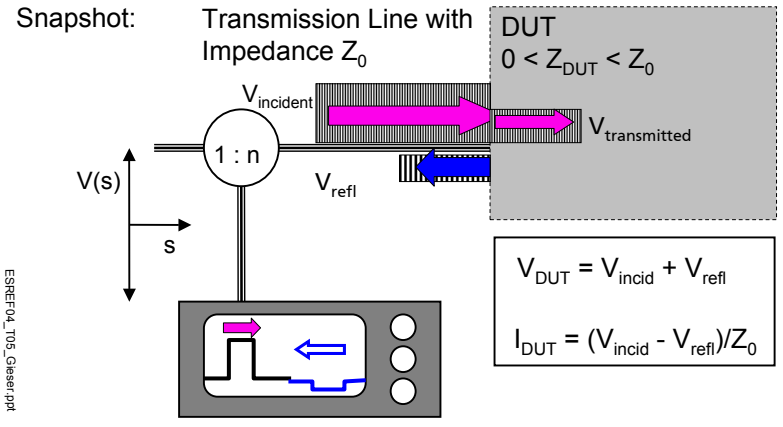
Principle of the Very Fast TLP

Snapshot:



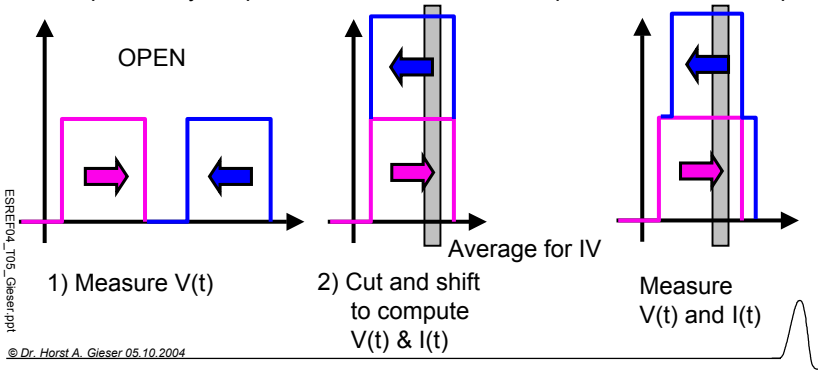
$V_{DUT} = V_{incid} + V_{refl}$

$I_{DUT} = (V_{incid} - V_{refl})/Z_0$

ESREF04_T05_Gieser.ppt

Seperated versus Overlayed Pulses

- Overlapping technique for longer pulse (e.g. 100 ns) duration only
- Requires very flat pulse roof, additional current probe, and oscilloscope channel



1) Measure V(t)

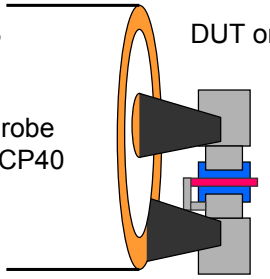
2) Cut and shift to compute V(t) & I(t)

Measure V(t) and I(t)

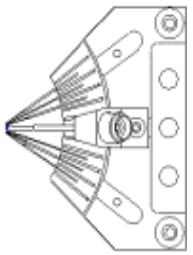
Controlled Impedance for vf-TLP

Delay Line TL3 with

RF- Coplanar Probe e.g: Cascade ACP40



DUT on Wafer

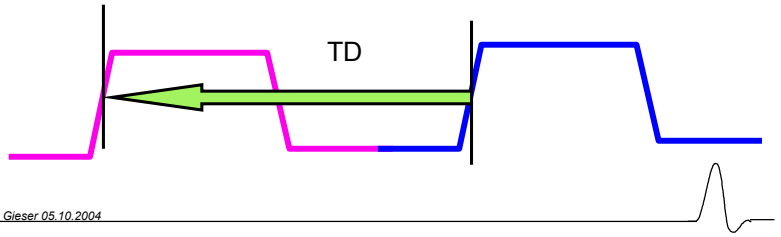


Cascade Microtech

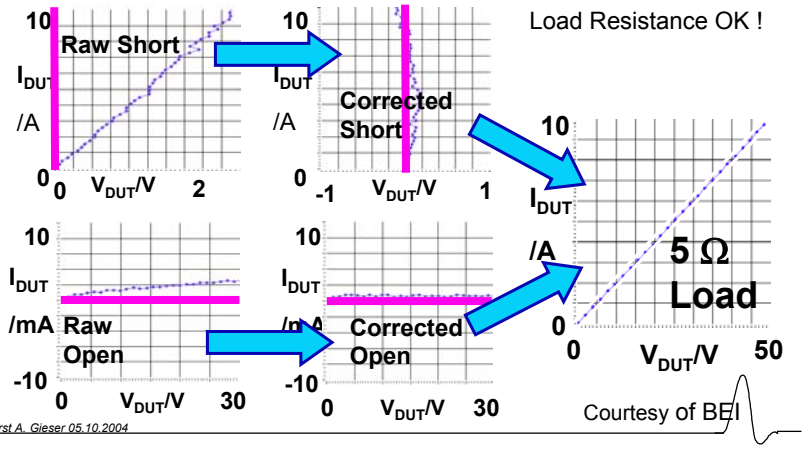
- Individual ground pads of DUTs !
- Pad pitch matches wafer probe !
- Additional pads and DC-needles for gate or substrate bias

5 Step Calibration of the vf-TLP: Step 1

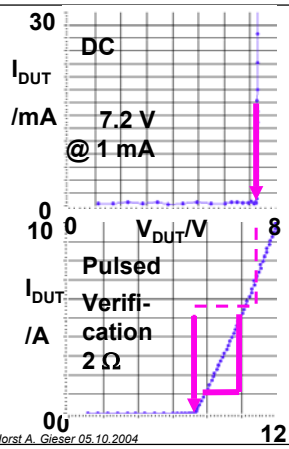
- Calibrate for length of TL3 including test fixture
- Measure time delay between half height of the rising edges of the initial and the reflected pulse for short or open.
- Time delay used by algorithm for shifting the reflected pulse left over the incident.
- Direct influence on measured transient !



5 Step Calibration of the vf-TLP: Step 2, 3 and 4



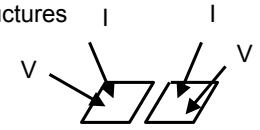
5 Step Calibration of the vf-TLP: Step 5



- Absolute DUT voltage: Zener breakdown voltage
- Known Voltage + Resistive Load R = 5 Ω: Absolute DUT Current
- NO TRANSIENT DATA !
- Optional for TLP500 Systems

Further Issues

- Variable contact resistance for low-ohmic structures
  - Kelvin Probes (Grund 2003)
- Best time resolution of sampling single shot oscilloscope 50 ps/pt
- Losses and dispersion deteriorate rising edge on long cables.
- Overlay uncertainty limits timing accuracy



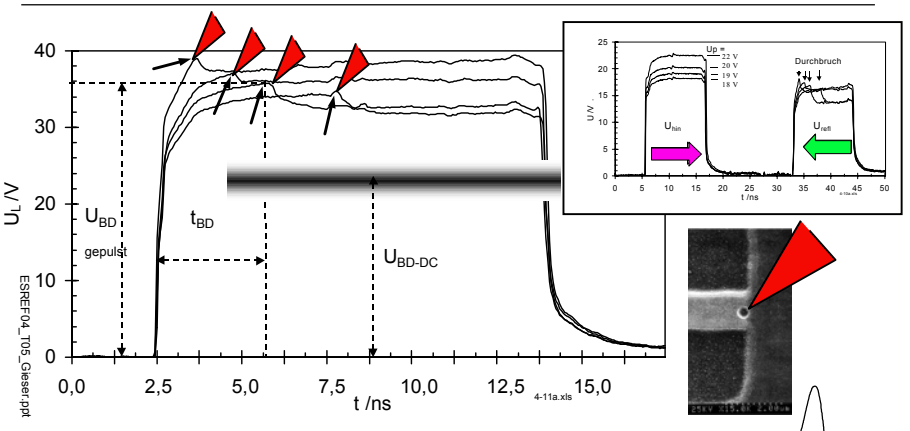
Applications of the vf-TLP

- **Addresses the CDM-domain well for two terminal structures**
  Turn on of protection elements and
  breakdown of gate oxides

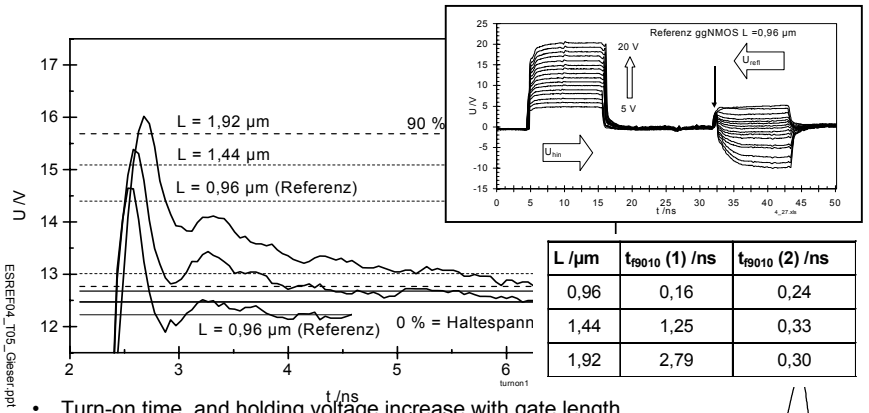
- Helps in CDM troubleshooting of ICs
- Reference for the calibration of device simulators
- Drives DUTs for analysis by
  Backside Laser Interferometry and
  Emmission Microscopy

- Drives Capacitively Coupled-TLP (cc-TLP) setup to apply CDM-like single pin stress

vf TLP: Gate Oxide Breakdown



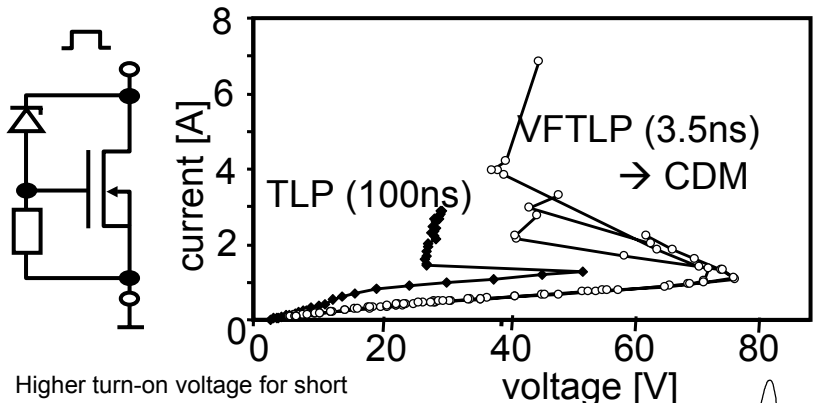
vf TLP: Turn-on of gg NMOS



L /µm	t_{f9010} (1) /ns	t_{f9010} (2) /ns
0,96	0,16	0,24
1,44	1,25	0,33
1,92	2,79	0,30

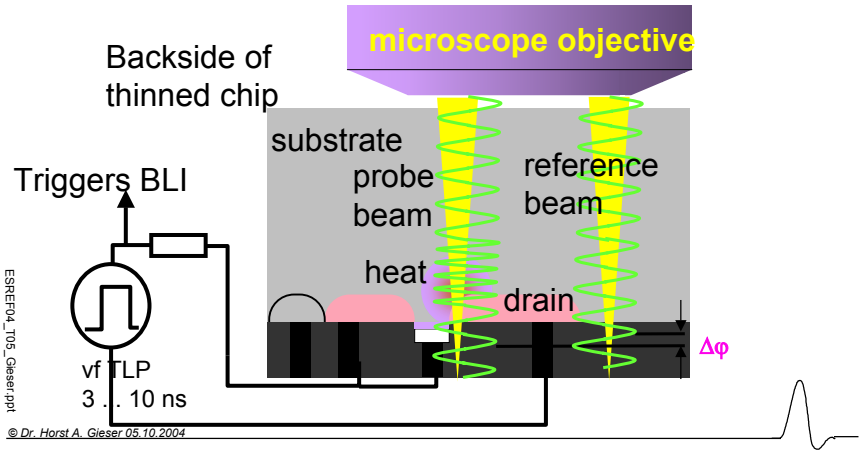
- Turn-on time and holding voltage increase with gate length

Shooting CDM Trouble of Input

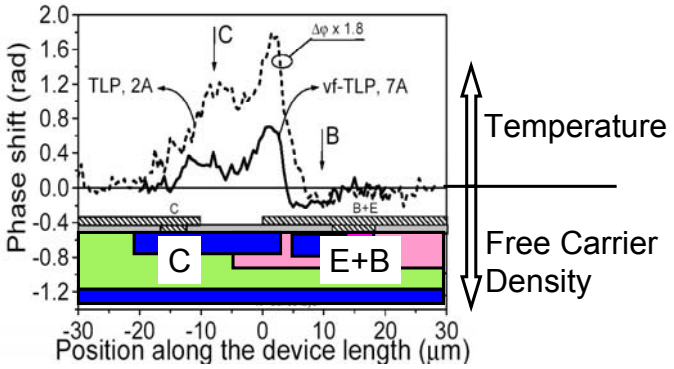


- Higher turn-on voltage for short pulses critical for gate oxides !!

Backside Laser Interferometer (BLI)



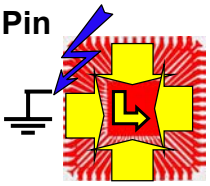
BLI: Temperature & Free Carrier Density

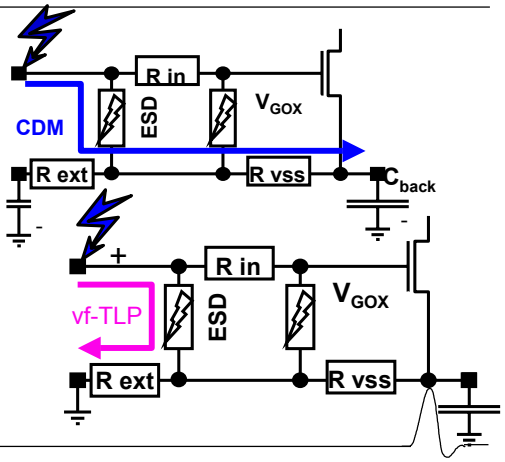


- Method applied to deep sub micron technologies, too.

Do NOT expect Correlation between vf-TLP and CDM for ICs, but Valuable for 2Pin-Structures !!

Charged Device Model CDM 1 Pin



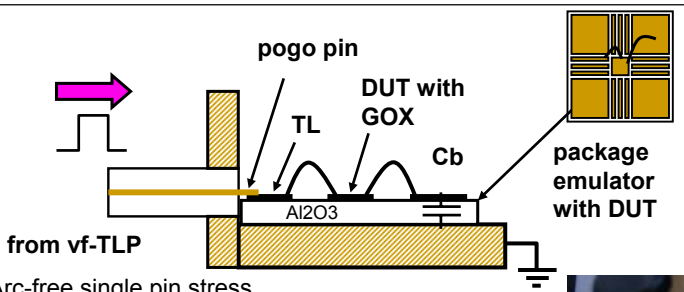


- Different current pathes result in different failure thresholds

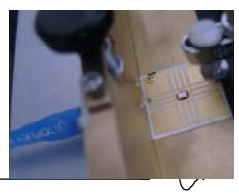
ESREF04_T05_Gieser.ppt

Capacitively Coupled TLP (cc-TLP)

Wiley2002



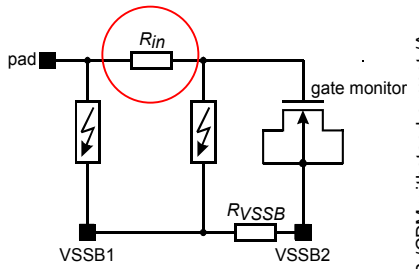
- Arc-free single pin stress
- Square pulses from vf-TLP injected into Cb across DUT
  generate CDM like voltage across GOX



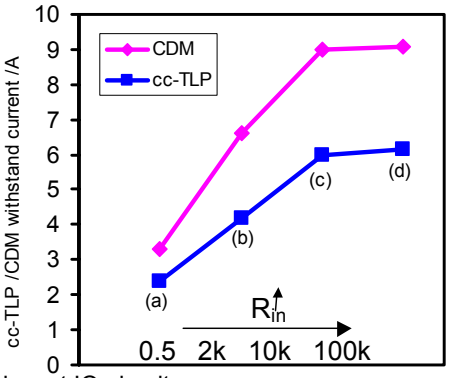
ESREF04_T05_Gieser.ppt

Wolf et.al. EOS2003, Gieser US Pat. 6512362

Correlation of Withstand Currents



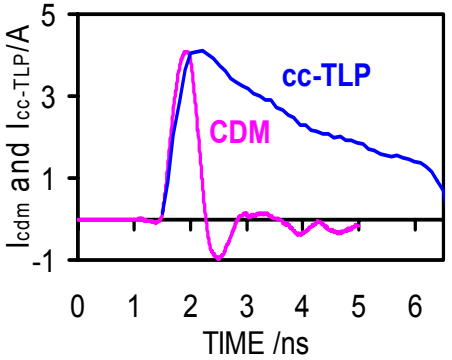
0.13 µm CMOS

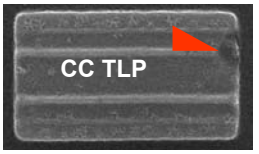


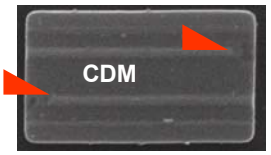
- Good correlation for simple CDM-relevant IO-circuits on package emulator

Wolf et.al. EOS2003, Gieser US Pat. 6512362

Comparison CDM cc-TLP







- Wider pulses explain lower threshold
- Correlation in physical failure signature

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Summary (1)

- HBM – µs pre-pulses and trailing pulses critical for actively clamped circuits.
- HBM – background capacitance relevant for protection efficency
- MM almost dormant in standardization
- Issues with interpretation of ringing and high pin count devices
- Further growing importance of CDM
- Arc-free characterization method should help to improve correlation
- Charged Board Model emerges for reproduction of failures on board and module level
- ESD-from-Outside-to Surface: A new failure mechanism not reproduced by standard tests
- How far can ICs cope directly with System Level stress ?

Summary (2)

- TLP well-established as a characterization tool during development and trouble shooting
- ESD Association develops standard test method for 100 ns TLP to address the HBM/MM domain.
- vf-TLP (Gieser ESD96) accepted to address the CDM-domain
- TLP sources pulses for BLI, EMMI and cc-TLP studies
- Both 50 Ω and 500 Ω have their field of application

- When will a combination of TLP tests replace today's qualification tests with more or less reproducible RLC discharge waveforms ?

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For free download of ESD-related test standards:

- ESD-Association’s ANSI Standard Test Methods **www.esda.org**
  (HBM, MM, CDM, SDM, TLP, Glossary of Terms)
- JEDEC Test Methods: **www.jedec.org**
  (HBM, MM, FCDM)
- Automotive Electronics Council (AEC): AEC-Q100 Rev F **www.aeconcil.com**
  (HBM, MM, FCDM)