Virtual Reliability Qualification

Prof. Kouchi (G.Q.) Zhang
g.q.zhang@philips.com
g.q.zhang@tue.nl

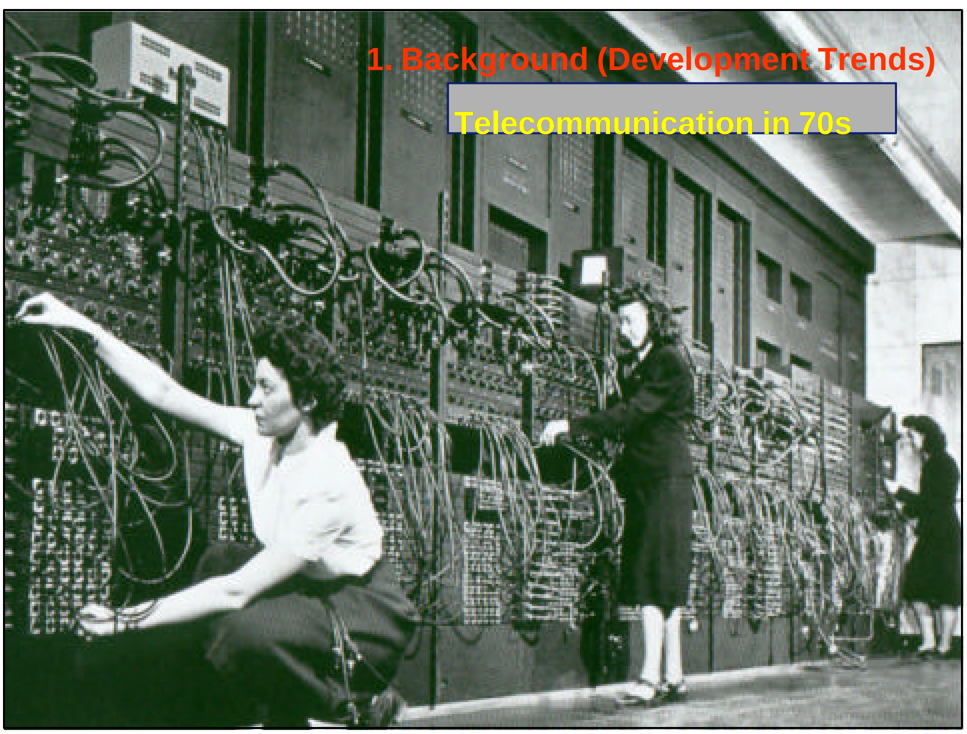
1. Development trends

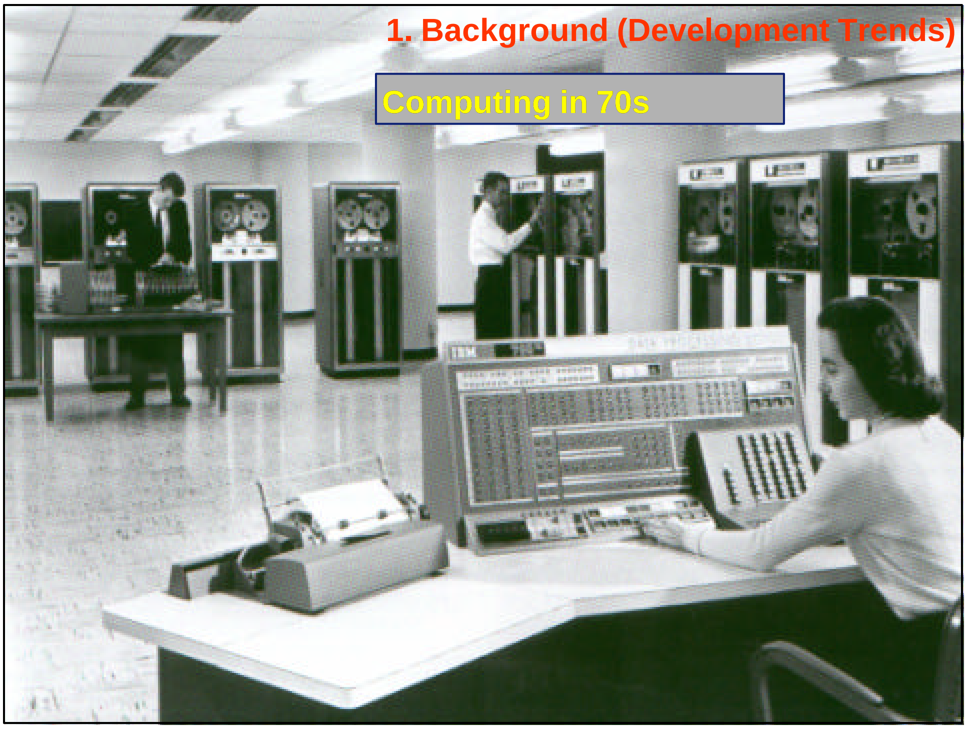
2. Consequences for reliability
- Thermo-mechanical problems
- Motivations

3. Virtual prototyping and qualification
- The Methodology
- Status Quo/challenges
- Demonstrators

4. Conclusions

1. Development trensd




1. Background (Development Trends)
Computing in 70s


1. Background (Development Trends)
Consumer electronics anno 2004

- **Moving from a world of electronic “boxes” to the world of ambient intelligence where technology is built into our environment via connectivity and integration.**
- **Focus on function, not the devices that enable them.**

•sensitive to people's needs
•personalized to their requirements
•anticipatory of their behavior and
•responsive to their presence

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Consumers wishes

Smaller, smarter, lighter, faster, cheaper, more flexible, more convenient, more reliable and functionalities.

Development trends

- Miniaturisation down to nano-scales
- Increasing levels functionality & technology integration
- Eco-designs

- Cost reduction
- Short-time-to-market
- Outsourcing

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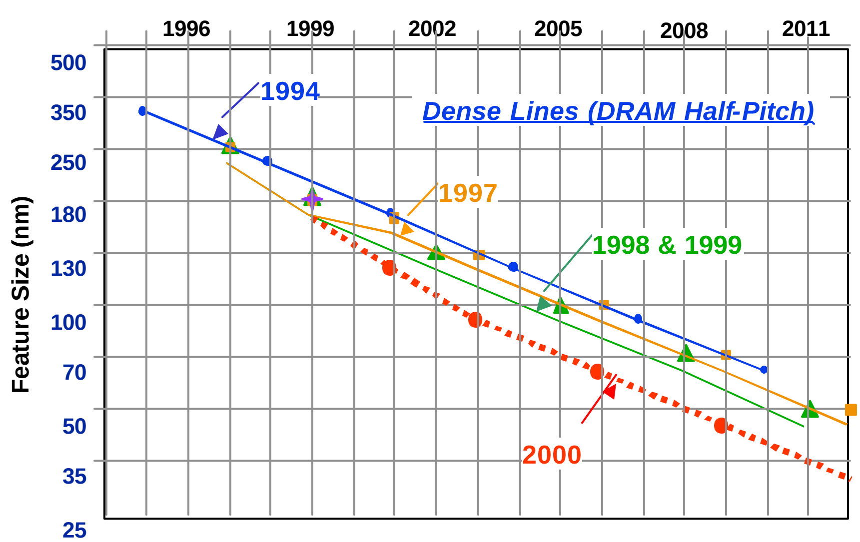
ITRS Roadmap History



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Process technology evolution

System-on-Chip: standardization

- Standard CMOS density will continue to grow exponentially, driving down the cost of digital data processing and storage
  - More Moore : System-on-Chip
- But realized digital design complexity increasingly lags behind the potential of new technologies, while investments soar
  - Decelerating long-term semiconductor market growth to single digit

Is the Roadmap Going to End?

Let's see some famous forecasts

" I think there is a world market for maybe five computers "
Thomas Watson, Chairman of IBM, 1943

" Computers in the future may weigh no more than 1.5 tons "
Popular Mechanics Magazine, 1949

" 640K ought to be enough for anybody "
Bill Gates, 1981

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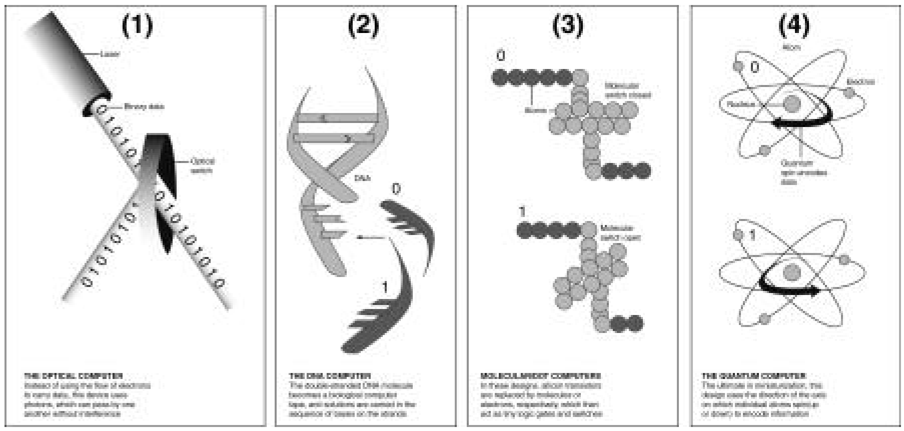
Alternative Switching Technologies



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Packaging & assembly

•Wire diameter	< 10 microns
•Interconnect pitch of NLWSP	< 20 microns
•Thickness of copper film/PCB	< 10 microns
•Microvia diameter	< 20 microns

Not only the wafer technology, packaging and assembly are also going beyond visualization!

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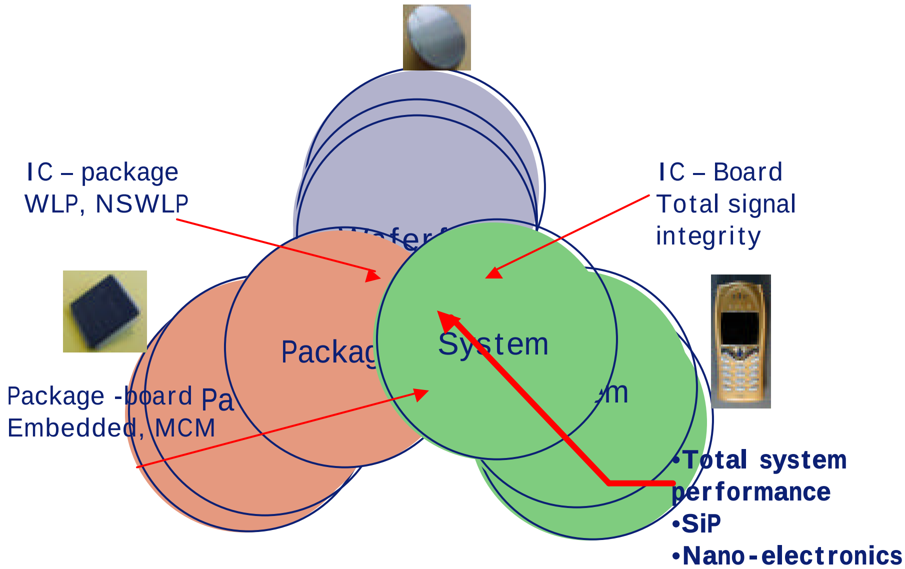

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More Moore and more than moore

Complementing, not competing

More Moore: **SoC-** Programmable monolithic IC

- Advanced baseline CMOS, standard packaging
- Maximize utilization of (expensive) mask sets
- Diversification is in the software & embedded IP mix

More than Moore: **SiP -** Multi-technology module

- Mature and advanced wafer processes, advanced packaging
- Maximize utilization of dedicated option fabs
- Diversification is in the components & technology mix

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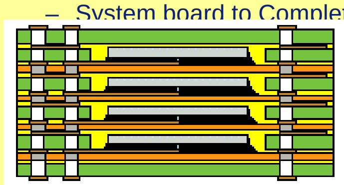
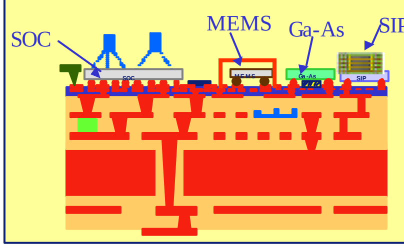
Examples of technology and function integration

SIP1	SIP3
• 3-D Stacking of ICS or Package Structures, Similar to PWB – Macro dimensions – Vertical stack up – Testable – System board to Complete	• 3 -D Build up, similar to IC Fabrication – Micro to Nano dimensions – Sequential build up and test similar to MCM-D and IC – Wafer to IC concept for high yield

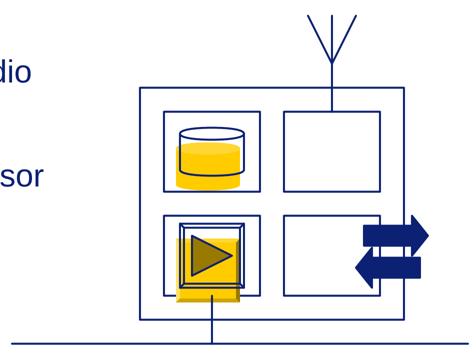




Generic sub-system

storage radio

µP sensor



(digital) communication bus

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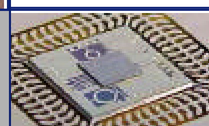
System-in-Package domains – 3

More than… **SoC**	*…one IC*	*…IC process*	*…electronics*
SiP 1 e.g., MCM			
SiP 2 e.g., Passive Integration			
SiP 3 e.g., MOEMS			

Increasing value proposition ®

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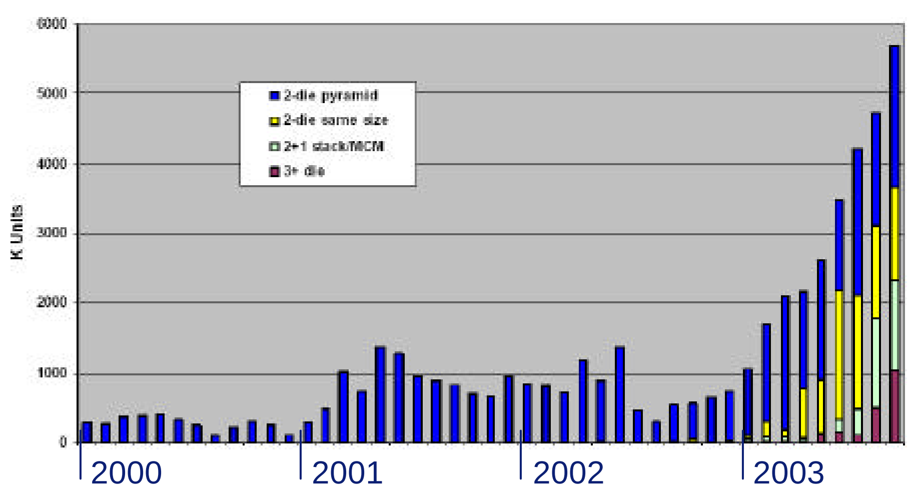
Stacked BGA production (leading vendor)



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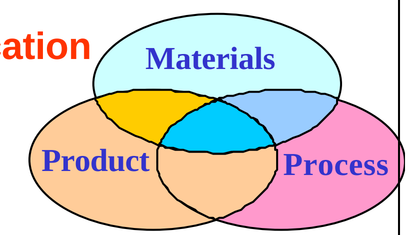
Eco-Design

Designing environmentally compatible products/processes while maintaining price/performance and quality characteristics.

Key Focus Areas:
- **Energy Usage (Products & Manufacturing Processes)**
- **End-of-Life Management**
- **Product Packaging**
- **Removing the boxes**
- **Virtual prototyping & qualification**



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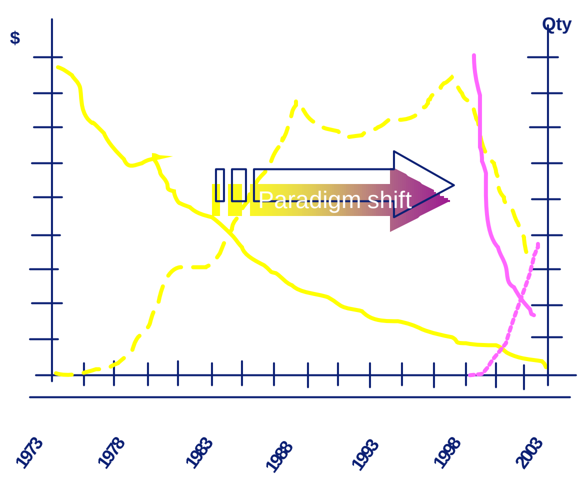
Paradigm shift: From Yellow to Purple



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2. Consequences for reliability

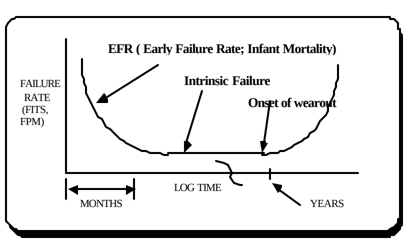
Reliability

The probability that a product in operation will survive under certain conditions during a certain period in time. IEC50 (191)

Quality

The totality of features and characteristics of a product or service that bear on its ability to satisfy stated or implied need. ISO 8420

Conventional bathtub curve



Our scope

From 0 hour to life time

- Multi-scale in both time and geometric domains with scale factors going up to 10^9.

- Strong interactions among different
  - disciplines (electrical, thermal, mechanical, physics, chemical, material science, etc.)
  - technologies (IC, packaging, assembly, system, soft and hardware)
  - failure modes and failure mechanisms

- Behaviour is strongly non-linear, stochastic, time and temperature dependence.

- Greatly increased loading intensity/loading steps

- Greatly increased design complexity and shrinking of design margin to nano levels.

- Strict demand on and challenges for ensuring quality, robustness and reliability to cover the total value chain

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$Q\&R=$??? $f_1(b_1, b_2,..\ b_i..)\ f_2(c_1, c_2,..\ c_i..)\ f_3(t_1, t_2,..\ t_i..)$ db dc dt

b: Business variables
c: Consumer variables
t: Technical variables

$f_3(t_1, t_2,..\ t_i..)=$??? F_1(material) F_2(process) F_3(product)

Q&R is innovation and integration of innovations

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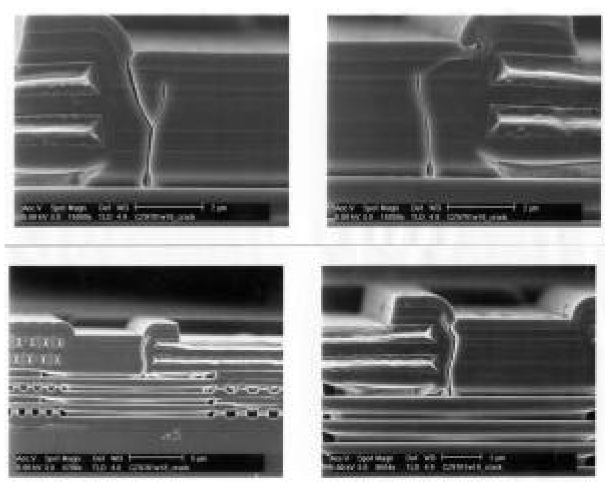

Example of various cracks emanating from the edge of bond pads.
May be caused by interface defects

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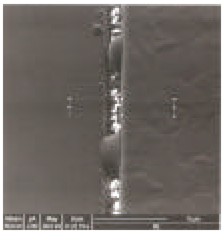
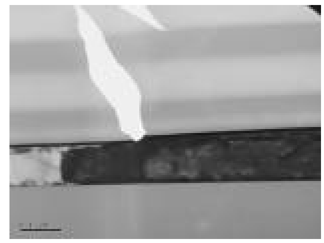


Pattern shift (Power line) caused by packaging stresses



Cracking as a result of electromigration

Warpage caused by wafer thinning: 200mm wafer thinned to 50 um

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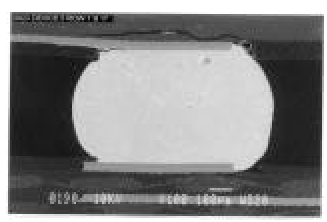
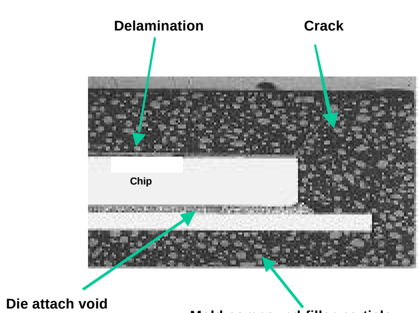
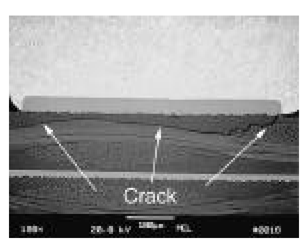
Die cracking in flip chip







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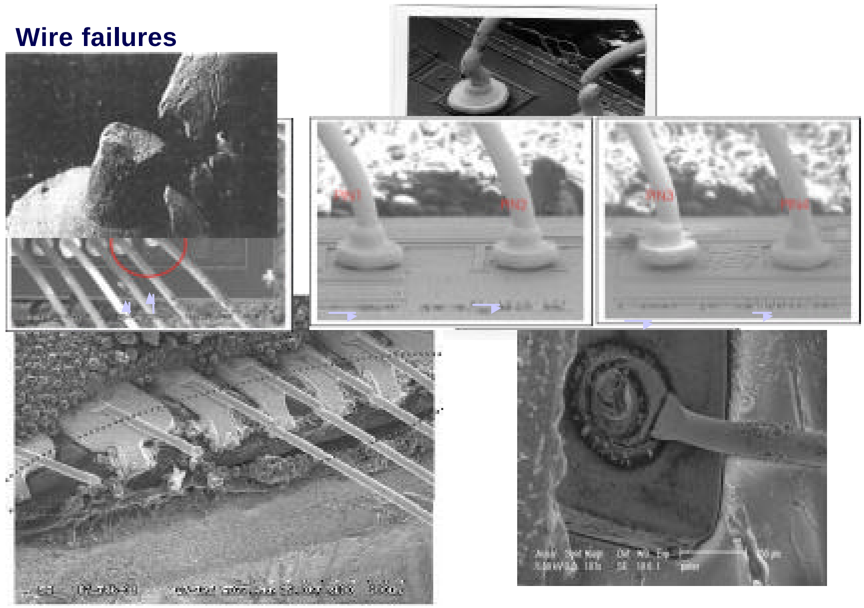
Wire failures



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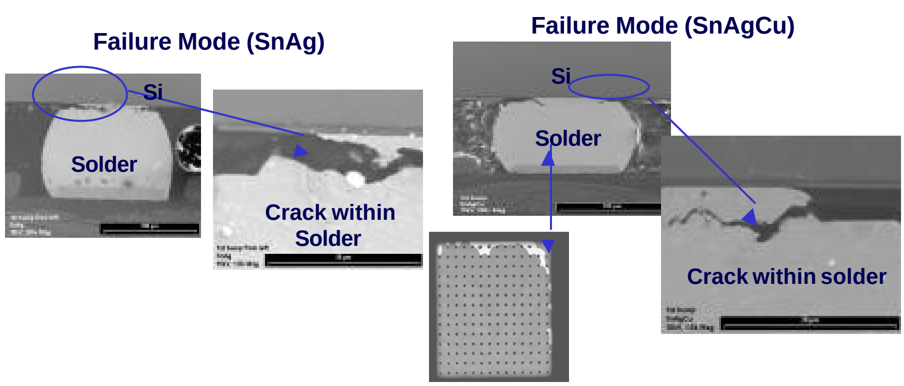

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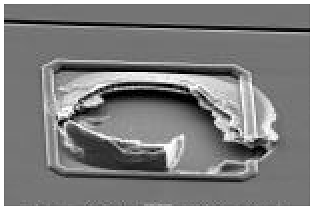
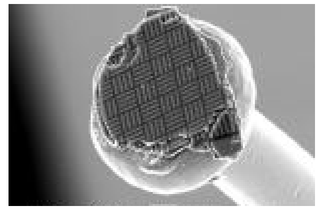
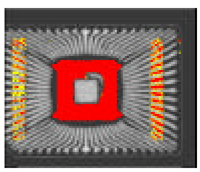
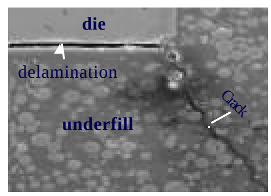
Delamination









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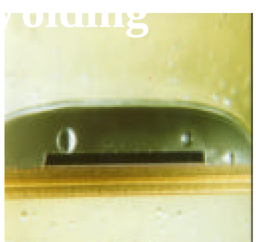
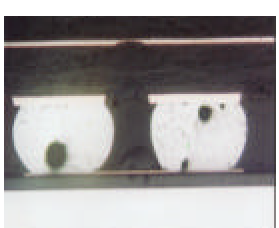
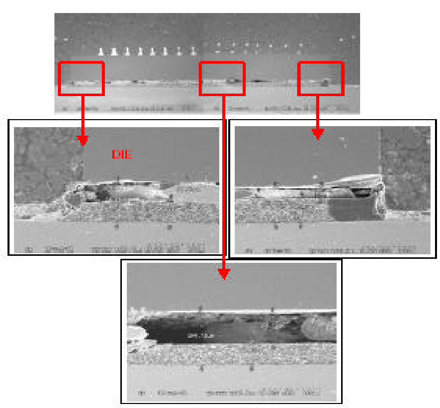


Chip on Board Globtop Voiding



Flip Chip Solder Joint Voiding



Underfil Voiding

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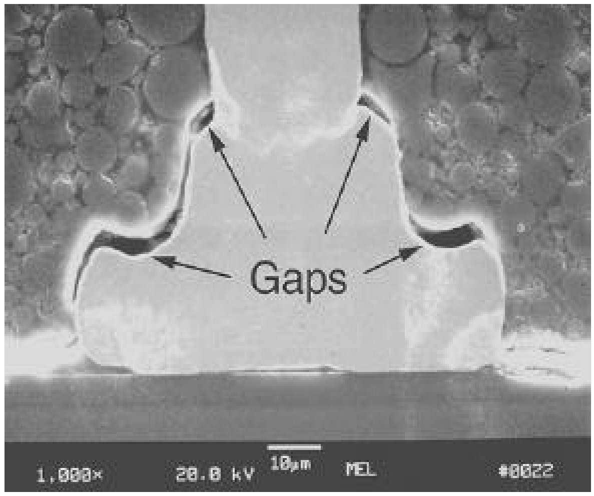
Voids caused by molding compound shrinkage



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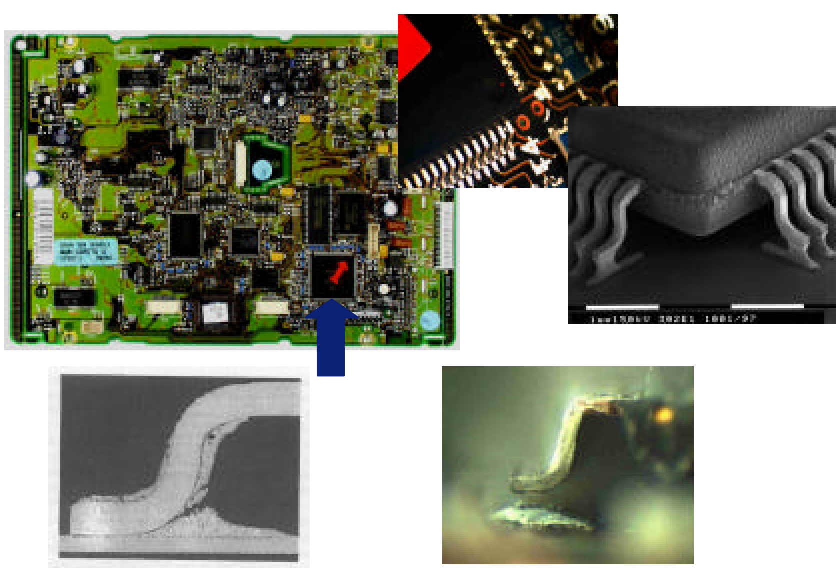

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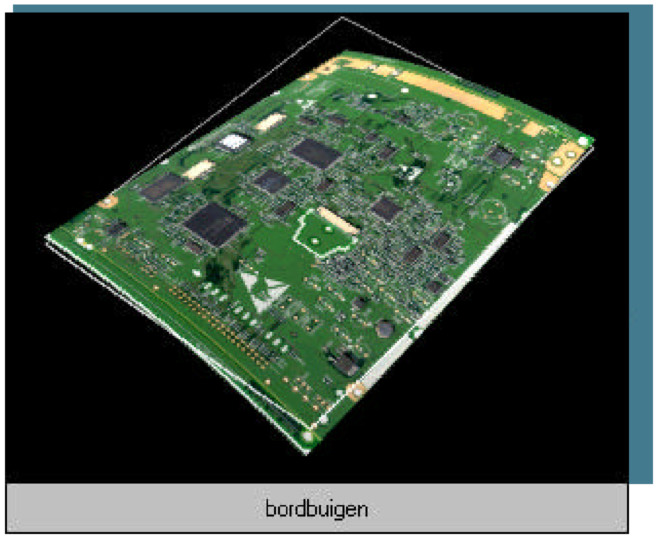

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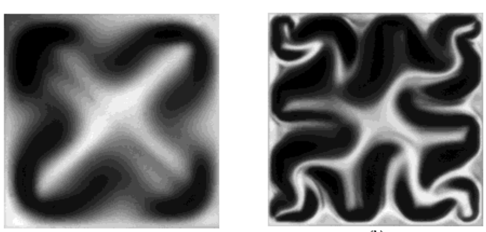
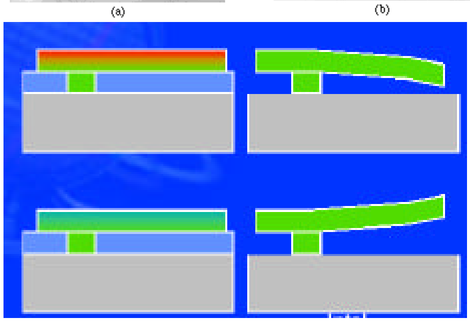


MEMS processing challenges:

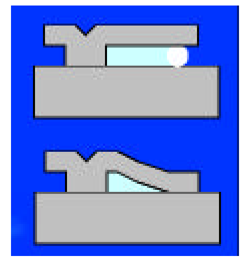
Buckling & postbuckling of membrane during CMOS micromachning

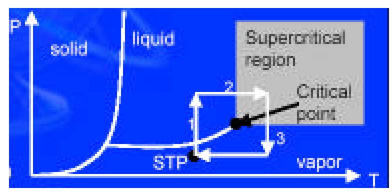


Stress gradients between the top and the bottom layers of a film

Releasing MEMS: Stiction problem

- Surface forces (van der Waals, hydrogen bonding, etc.) are much stronger than bulk forces (spring restoring forces, gravity)
- Consequence: MEMS stict upon contact
- Common for MEMS that are mechanically compliant or have small gaps





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Wear out
- Fatigues
- Creep
- Wear
- .....

Overstress
- Cracks (die, plastic, wirebond, etc.)
- Delamination
- Pop-corn
- Buckling
- Yields (ball shear, pattern shift, etc.)
- Warpage
- Large deformation
- Electro/thermal/stress migration
- Voiding
- ......

- **New and combined failure modes &mechanisms**
- **>65% of failures thermo-mechanical related!**

No appropriate thermo-mechanical design method

•Experience and trial-error based design method
•Empirical, phenomenological, case dependent,
•Sub-optimal product/process
•High development costs

No appropriate thermo-mechanical qualification method

•Time and money consuming
•Unclear correlation between application profiles with spec. and accelerated testing
•No guarantee for extrapolating to outside of the spec.
•No satisfied coverage for quality, robustness and reliability

New Paradigm of Reliability

To meet the needs of tech. trends, a new & knowledge-based Reliability Paradigm is a must.

The scientific successes of many micro/nano-related technology development would never lead to a business success without breakthroughs in the way that we are handling reliability through the whole value chain .

3. Virtual prototyping and qualifications

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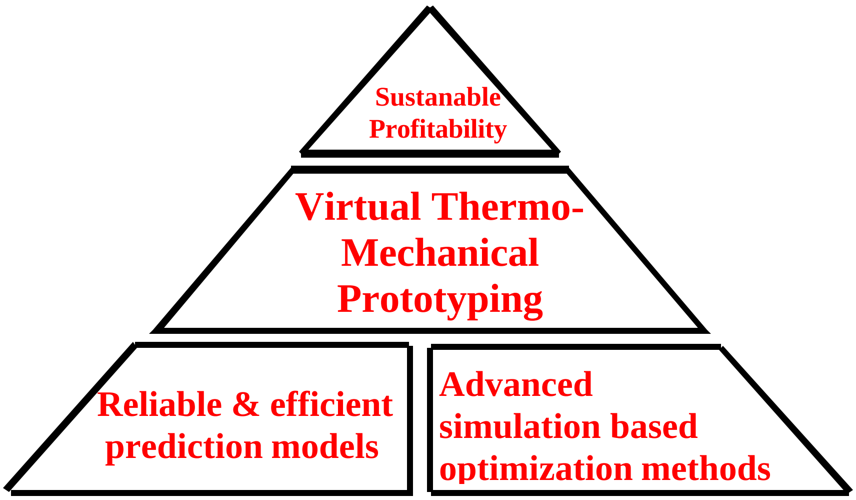

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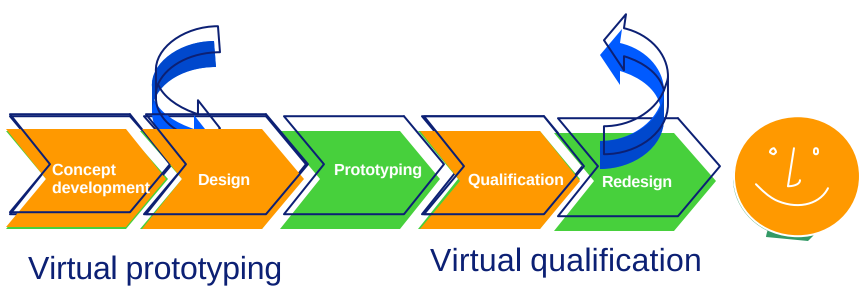

Objectives and benefits

- Short-time-to-market
- Cost reduction
- Product/process optimization
- Quality, robustness and reliability insurance

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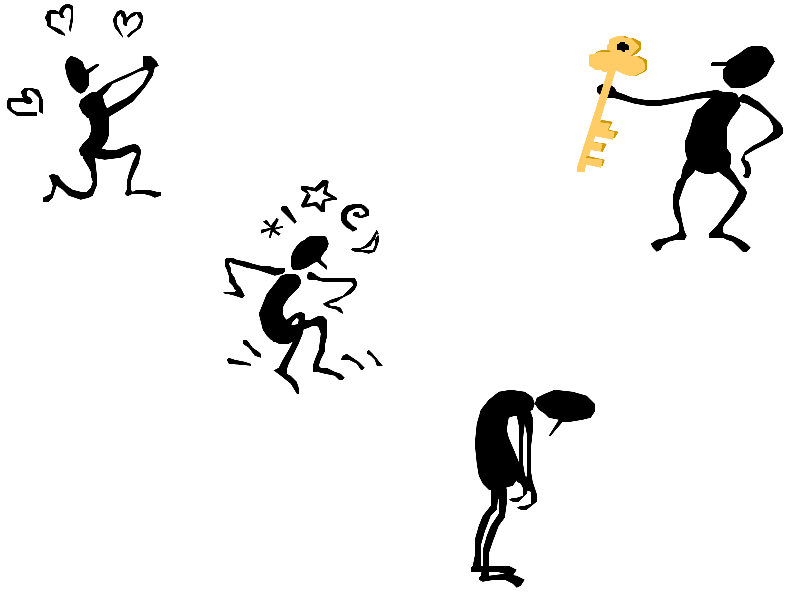

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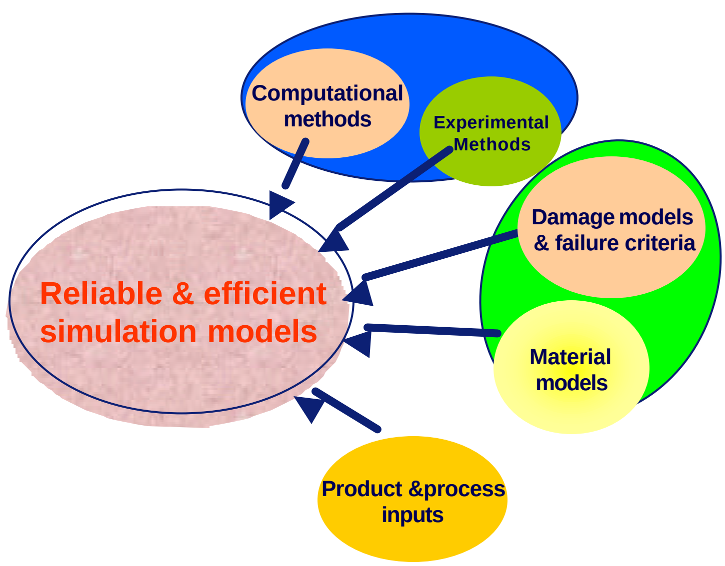

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Product &process inputs

• Process parame sembly, testing, reliability qualific

• Product paramet s,tolerance design, interface design, ...effects, etc.;

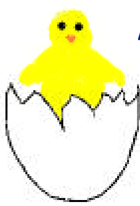
All statistic in nature

37C for 21 days

140C for 3 minutes

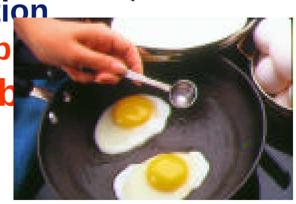
Determining

• loading and loading history; material behavior; initial stress d amage initiation and evolution



• d performance of product/p

!!! Inputs must be reliab



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Damage models & failure criteria

Material models

- **Material & damage models**

Laws governing the behavior of materials & interfaces

- Constitutive law and damage models cannot be partitioned anymore

- Size effects
  * Microstructures and their evolutions
  * Gradient effect (chemical, electrical, thermal and mechanical)
  * Surface effect

- Strong process-dependence
  Temperature, time, constraint, stress, interfaces & reactions

- Multi-scale damage, initiation, failure criteria and process-dependent evolution

- Ultimate aim: Material design rules to tailor the properties for specific need

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Computational methods

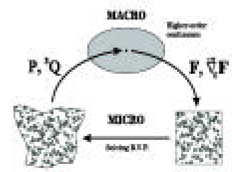
Experimental Mechanics

Deterministic

Characterization

Stoch

•Non-continuum;
•Multi-scale (bridging gaps);
•Multi-physics;
•Multi-failure mode;
•Multi-process;
•Nonlinear;
•3D applications;
•Efficient & accurate
•Advanced FEM tool (MARC)



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In principal, all the simulation results are wrong, unless you can prove they are right.

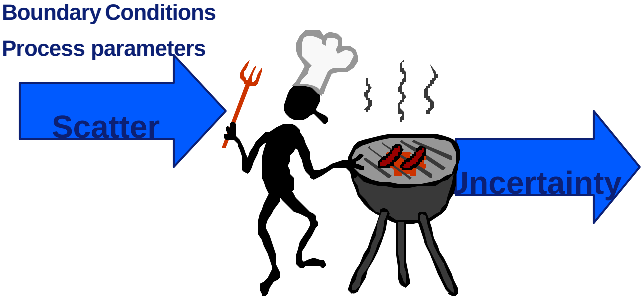
Simulation based optimization

Optimization based on and integrated with advanced simulation models

- Maximum & minimum
- Robust design
- Parameter sensitivity

under given bounds of design and response parameters

Material Parameters
Geometry
Boundary Conditions
Process parameters



Deformation
Stresses / Strains
Fatigue, Creep, Crack
……

1. How large is the scatter of the output parameters?
2. What is the probability that output parameters do not fulfil design criteria (failure probability)?
3. How much does the scatter of the input parameters contribute to the scatter of the output (sensitivities)?

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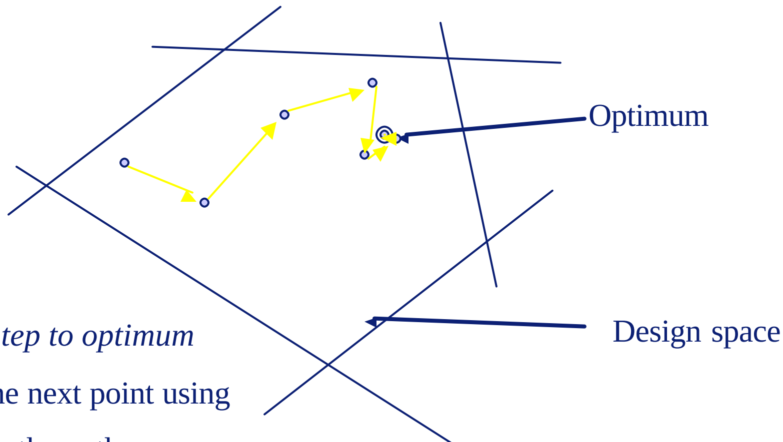
Sequential optimization



Step by step to optimum

Determine next point using

info from the path

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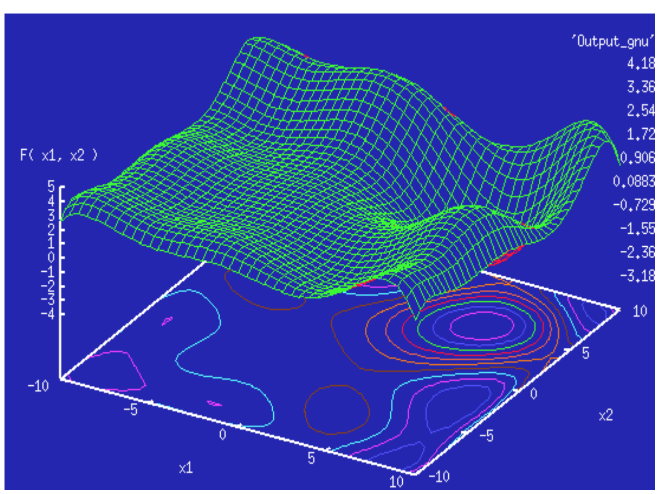
Compact-model optimization



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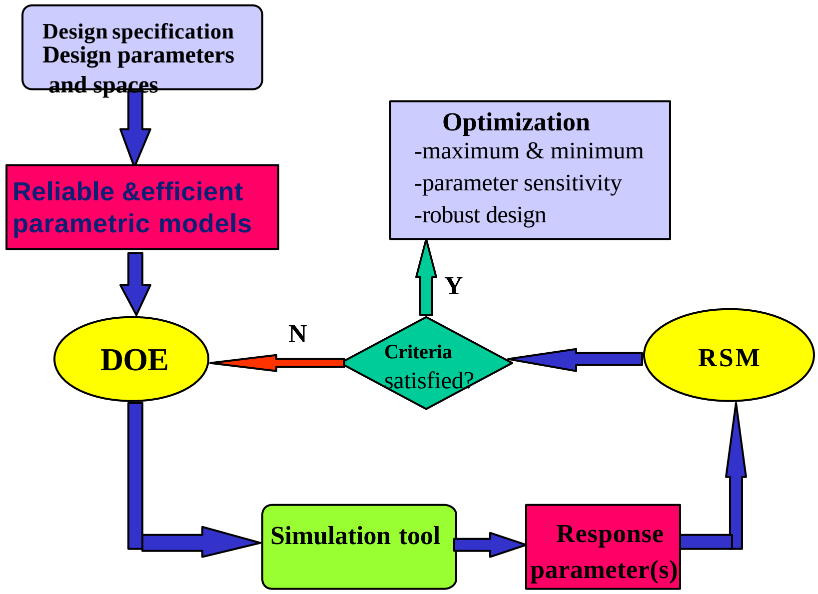

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Problem

Expensive for nonlinear responses

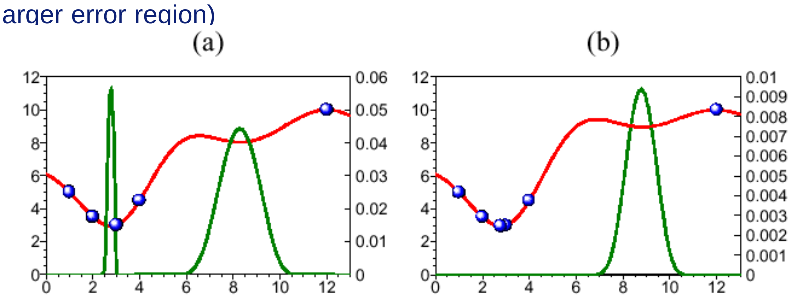
Objective

To develop smart infill sampling strategy & criteria for efficient and reliable RSM development and global optimization

Method

EGO (Efficient Global Optimization): Expected **I**mprovement

(low objective function in optimal objective region & high uncertainty in larger error region)



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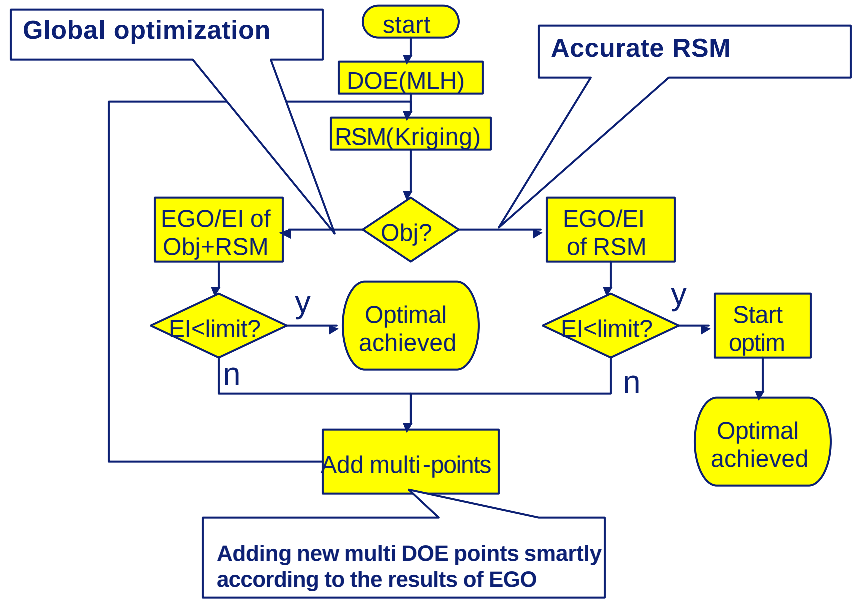

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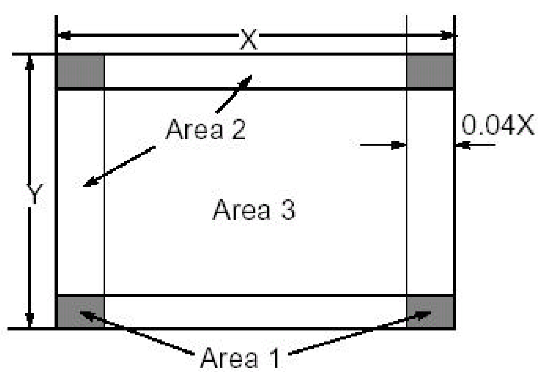
Current IC stress design rules



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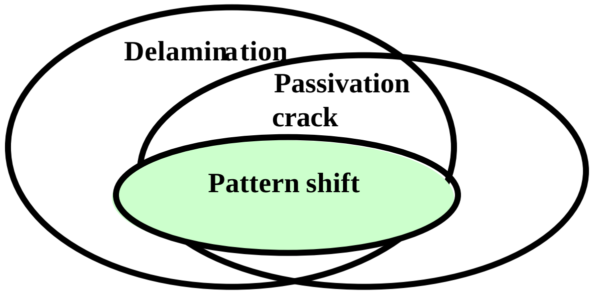

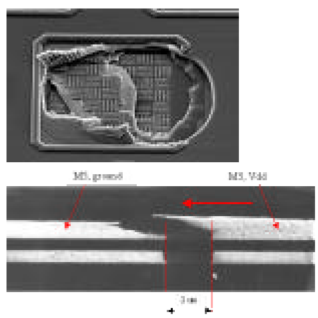

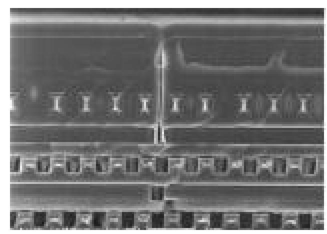

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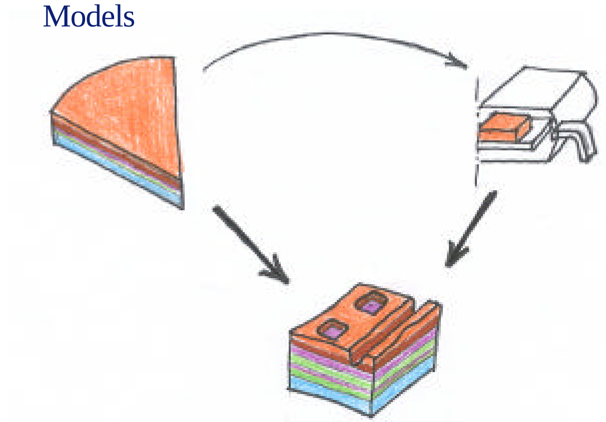
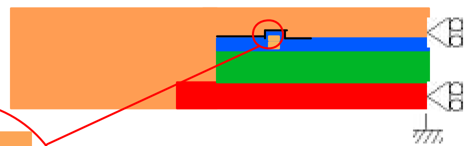
1 Wafer
Models

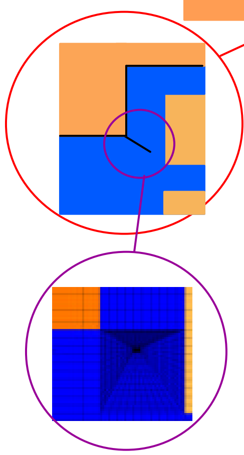
2 Packaging Models



3 IC Models

Delamination - Crack energy criteria

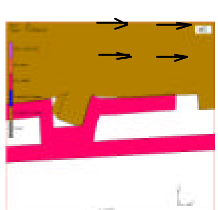




2D model
with delamination
and crack

Aim:
- Predict J-integral values
- Determine effect of 2nd metal level

Influence of IC/compound delamination on passivation cracks/pattern shift



Deformation mechanism

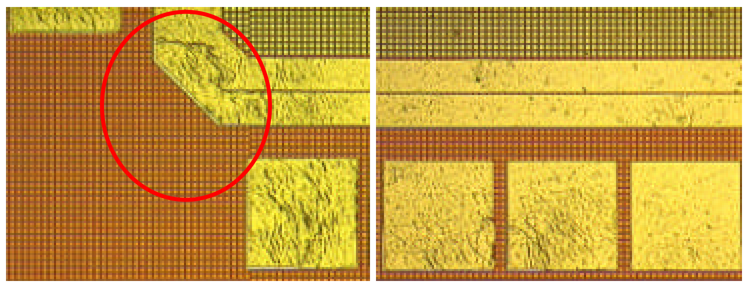
Tensile stress distribution

- Delamination may lead to passivation cracks and pattern shift.
- Depending on metal layout.
- Critical crack location is identified.

Experimental and numerical results

- Special test samples designed for the carrier product.
- Observations compared with simulations.
- With the verified models a wide design space simulated.

Metal shift



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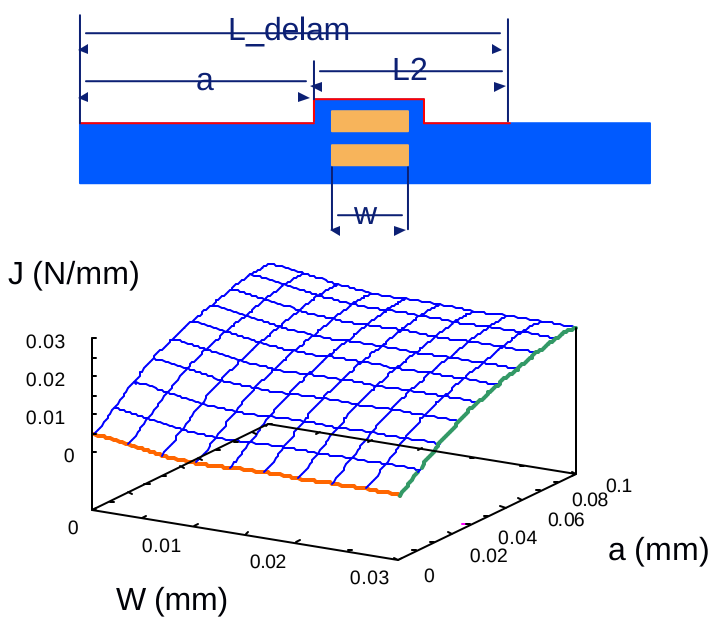

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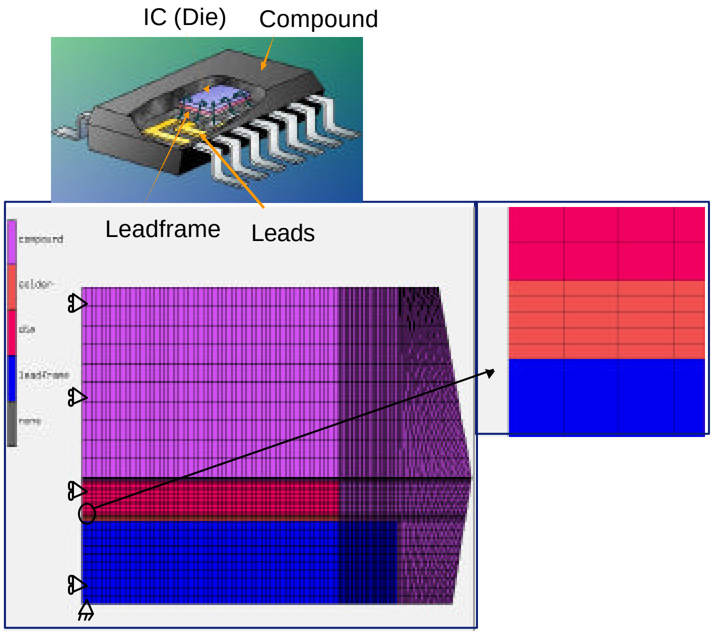

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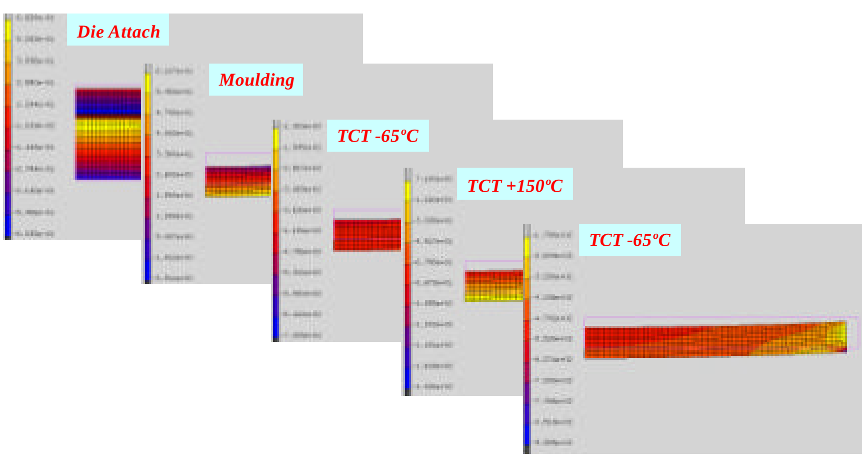
Stress Evolution for Nominal Design



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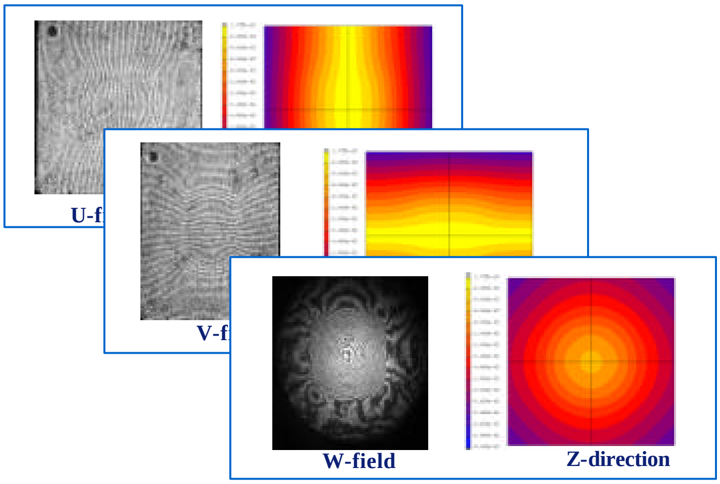
Results - Comparison with FEM



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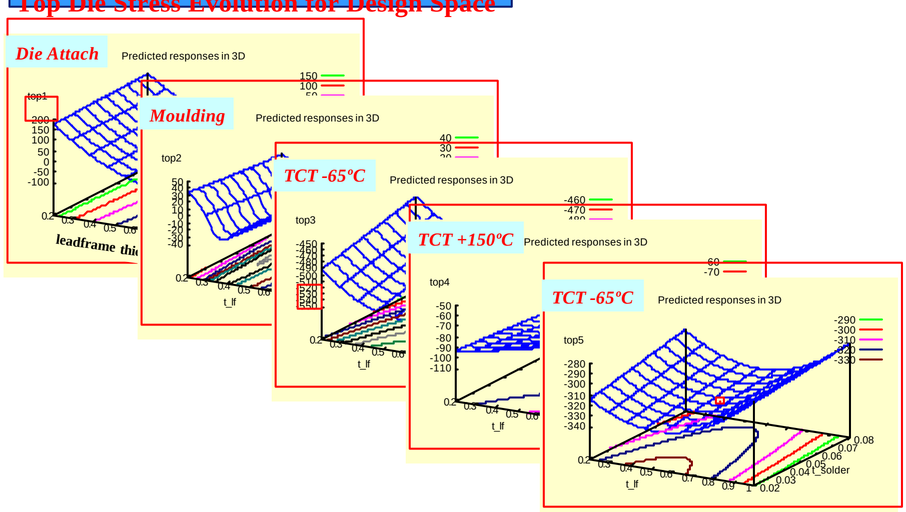
Top Die Stress Evolution for Design Space



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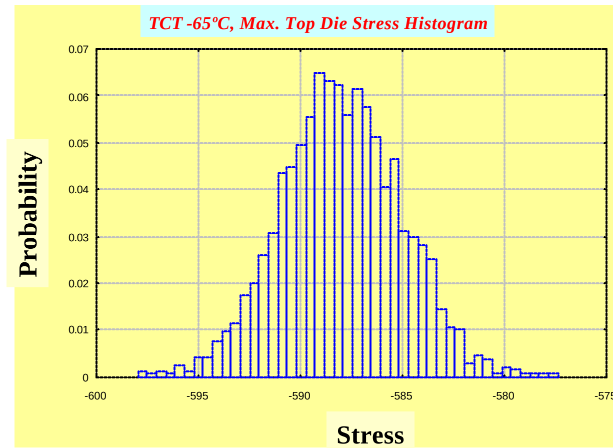
Sensitivity to Solder Thickness



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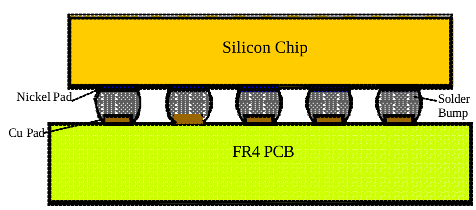
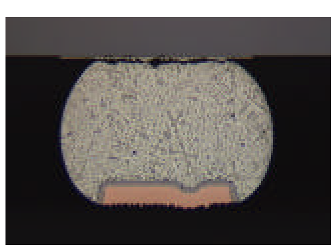
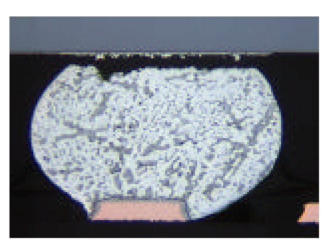
Solder joint failure under thermal loading







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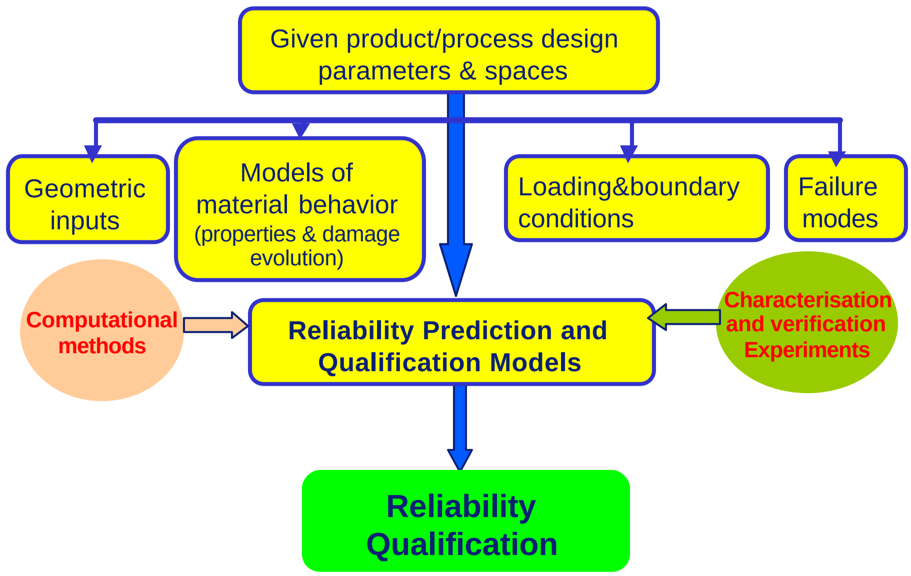
2. Methodologies

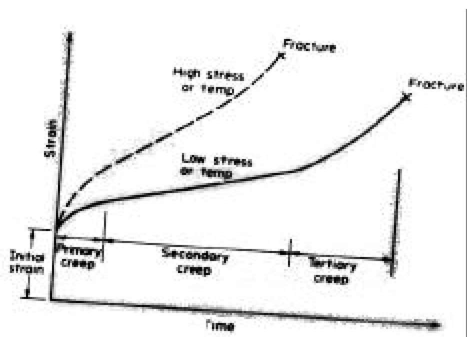


Homologous temperature (?)

$T_{hom}=T_{current}/T_{melting}$

Creep (?)

- Time dependent inelastic strain under constant load and elevated temperature
- Three phases: Primary (decrease SR); secondary constant(SR); tertiary(increase SR)



$$\dot{e} = \dot{e}^{el}_{eq} + \dot{e}^{cr}_{eq} + \dot{e}^{pl}$$

$$\dot{e}^{inel} = \dot{e}^{cr} + \dot{e}^{pl}$$ Extended Maxwell

$$\dot{e}^{inel} = \dot{e}^{cr}$$ Maxwell

$$\dot{e}^{inel} = \dot{e}^{pl}$$ Elastic-plastic

$$\dot{e}^{inel} = \dot{e}^{cr} = \dot{e}^{pl}$$ Bingham

$$\dot{e}^{cr} = f_1(s)\, f_2(T)\, f_3(t)$$

f_1 (s)=A s ^{n}
f_1 (s)=B exp(α s)
f_1 (s)=C (exp(α s)-1)
f_1 (s)=Dsinh(βα)
f_1 (s)={Dsinh(βα)}^{m}

f_2(T)=exp (-Q/RT)

R:boltzmann constant; T absolute tem.; Q apparent activation energy

f_3 (t)=a t^n
f_3 (t)=(1+bt$^{1/3}$)exp(kt)

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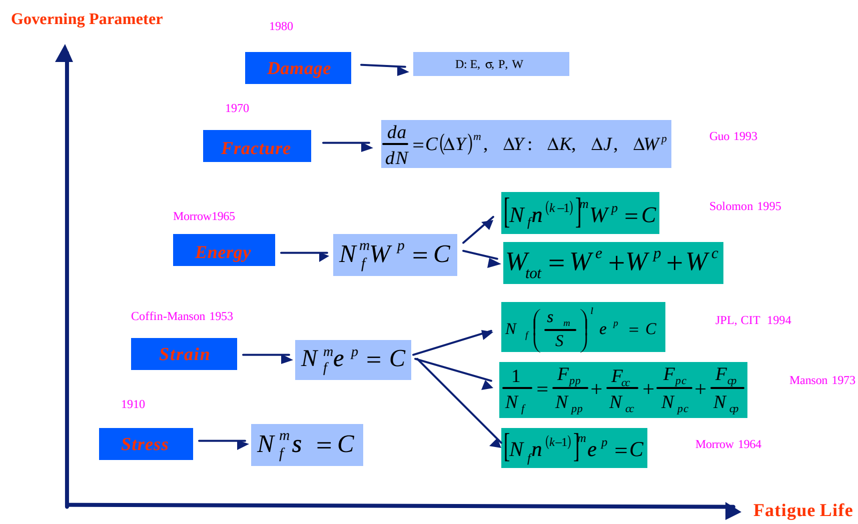
2. Methodologies



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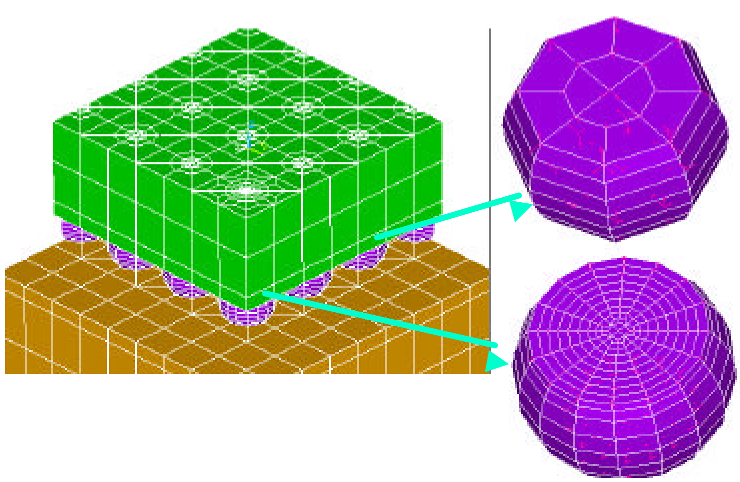
Finite Element Model-7x7Matrix Array



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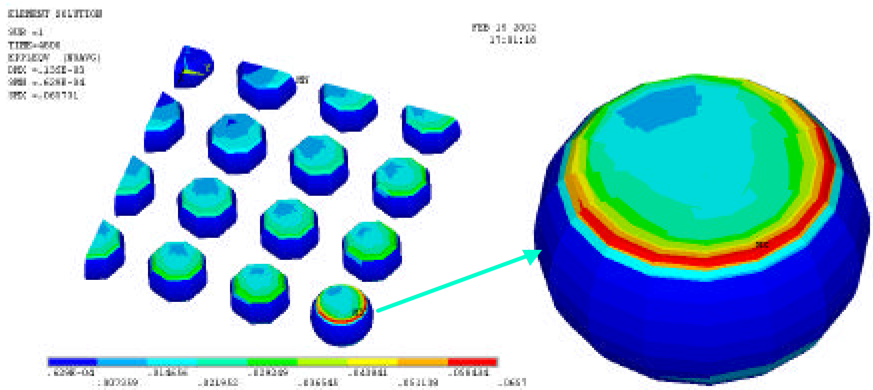
Equivalent Plastic Strain Distribution in Solder Joints at the End of 2nd Cycle



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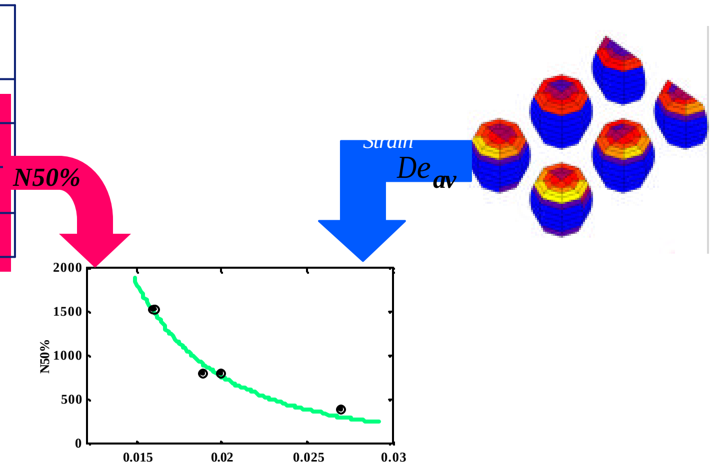
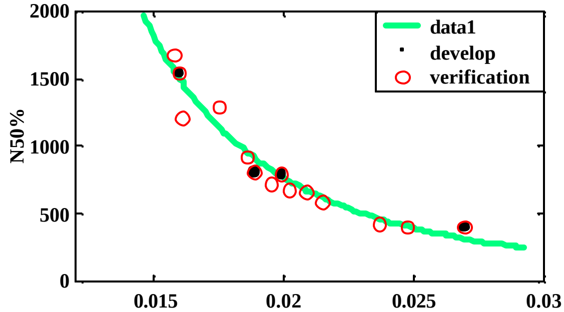
Fatigue Life Model: Manson_Coffin Based Empirical Model

Case	N50% (Test)
A1	1530
A4	711
B2	803
B7	390



Fatigue Life Model: Manson_Coffin Based Empirical Model



$$Life = 0.448(\Delta\varepsilon_{10um})^{-2.49}$$

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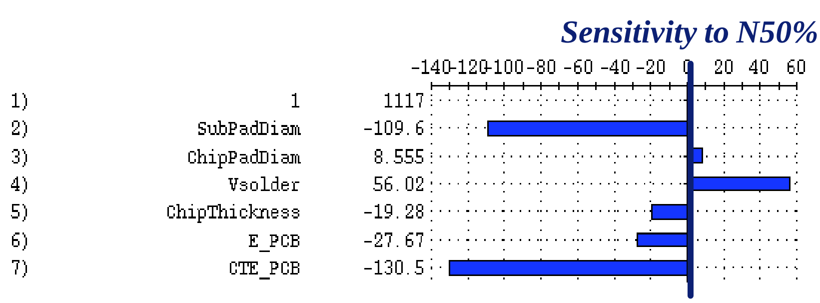
What are the most sensitive parameters to N50%?



- **Most sensitive parameters to N50%:**
  - **Substrate pad diameter (an increase in substrate value, has a decreasing effect to the reliability N50%)**
  - **Solder volume**
  - **CTE of the PCB**
- **These parameters need a good income inspection**

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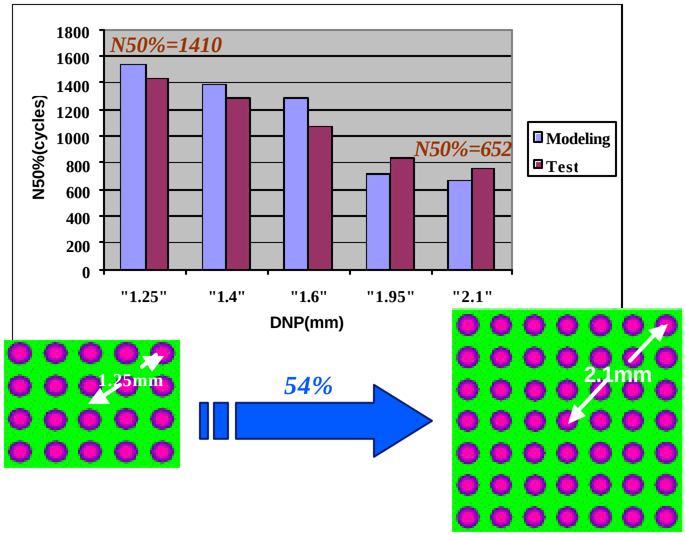
Effects of component size (DNP)



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Example: Optimizing wire loop design to prevent wire break

Problem:

Interconnect wire break is the dominant failure in electronic packaging. Figs. 1 & 2 show the failure on the stitch and the ball side, respectively. There is urgent industrial need to design optimal wire loop in order to prevent possible wire breaks.

Method:

Due to the large scale difference, global-local method is used in developing reliable FEM models to simulate the stress levels in a wire, in combination with nonlinear material model of the wire. From the global package model, wire deformations are obtained and serve as the input for the local wire model.

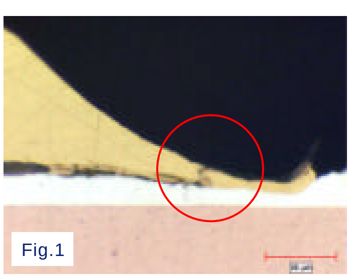

Fig.1

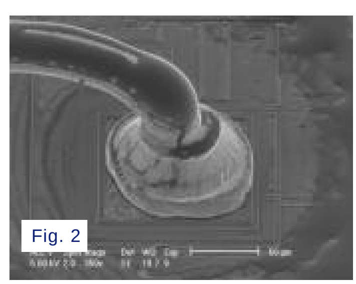

Fig. 2

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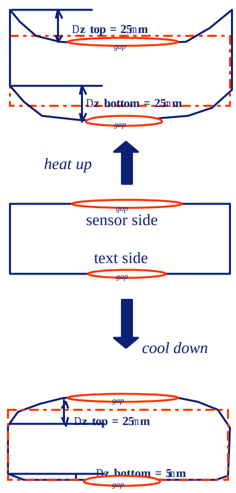
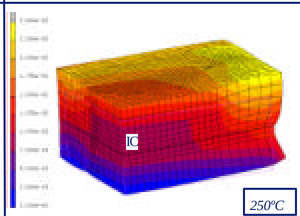
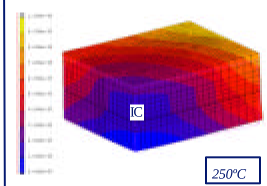
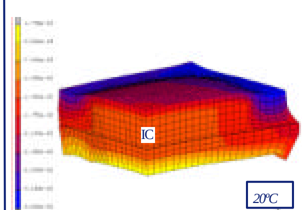
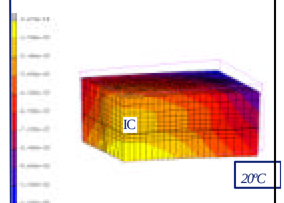
Correlation with Interferometry Measurements

Temp	Measurements	Model: transparent	Model: black
250ºC		 Dz top = 23μm Dz bottom = 11μm	 Dz top = 8μm Dz bottom = 7μm
175ºC			
20ºC		 Dz top = 31μm Dz bottom = 10μm	 Dz corner top = 12μm Dz corner bottom = 8μm

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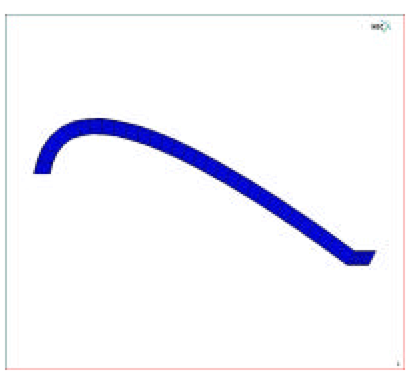
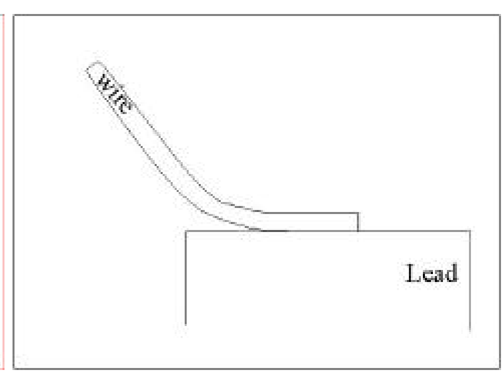
Wire fatigue - principle





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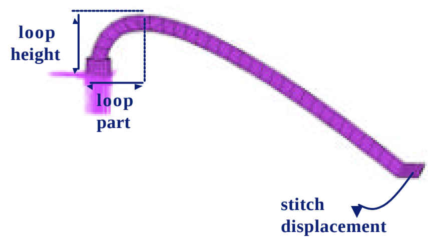
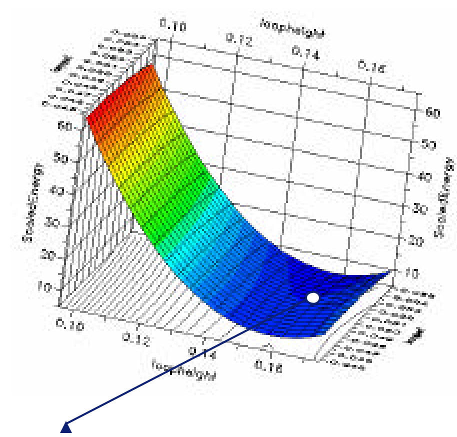
Result: Optimized wire shape





Optimized loop

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4. Conclusions

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- Future technology/business development trends demand virtual prototyping/virtual qualifications.
- The developed methodologies can generate high added business values.
- Not to replay physical prototyping/qualification, but to reduce their numbers and duration.
- Many challenges remain. Combined effort needed.

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