Integrated Systems Engineering
Development, Modeling, and Optimization of Microelectronic Processes, Devices, Circuits, and Systems

TCAD for Reliability

Tutorial at ESREF 2004, Zurich

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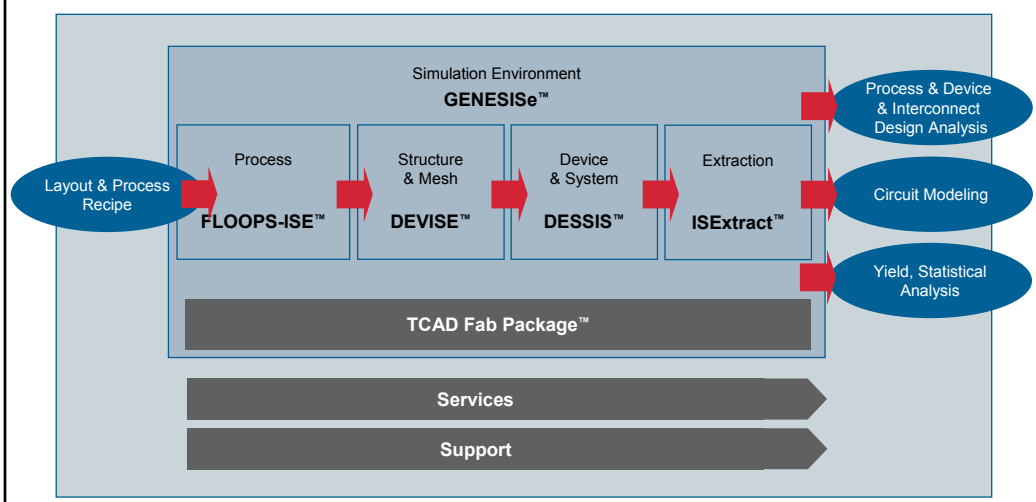
- ISE TCAD™ overview
- ESD
- Hot carrier effects, trap models and degradation
- Radiation effects: single event upsets, total dose effects
- Discussion
- TCAD tool demo

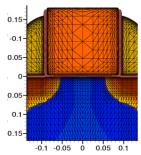
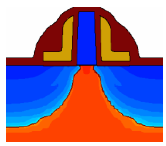
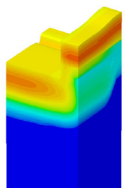
Tool Overview

Product Overview



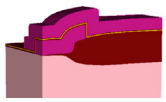
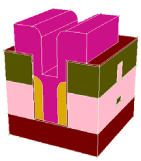
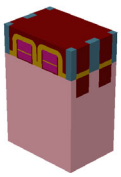
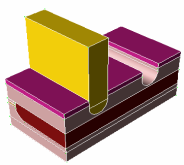
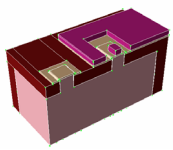
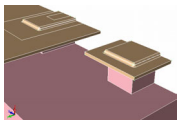
FLOOPS-ISE™

- Originally written by Mark Law and coworkers at University of Florida.
- Single simulator for 1D, 2D, and 3D
  - Consistent models and syntax
- Implantation, diffusion, oxidation
  - State-of-the-art models
  - Calibration ongoing
- Etching and deposition
  - *MGOALS*: Highly efficient geometrical engine
- Anisotropic boundary adaptive meshing
- *Alagator*: user defined diffusion models
  - fast prototyping
  - simple implementations of advanced models

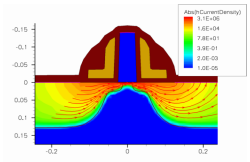
DEVISE™

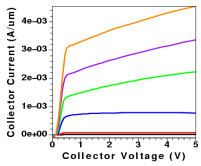
- 3D ASIC modeler from Spatial as geometry kernel
- 2D/3D Boundary Editor
- 2D/3D Doping and Refinement Editor
- 3D Process Emulator (PROCEM)
- Interactive and Batch Mode
- Interface to the ISE Meshing Engines

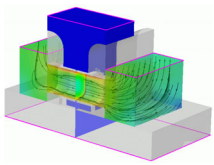







DESSIS™

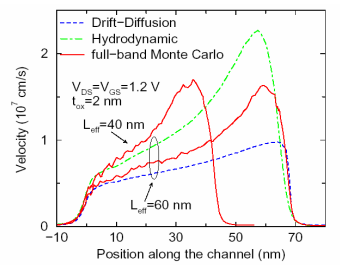
- 1D / 2D / 3D Simulator
- DC / Transient / AC Analysis / Optical AC / Noise Analysis
- Quantum Effects
- Si, SiGe, and Arbitrary Materials
- State-of-the-Art Transport Models
- Monte Carlo Device Simulations with SPARTA™
- Heterostructure Capabilities
- Mixed-Mode: Numerical and Compact SPICE Models
- Physical Model Interface (PMI)
- Optoelectronics (LED, VCSEL, Solar Cells, …)
- High-Efficiency Linear Solvers
- …

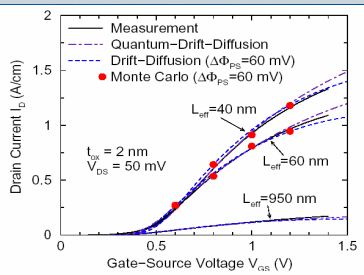


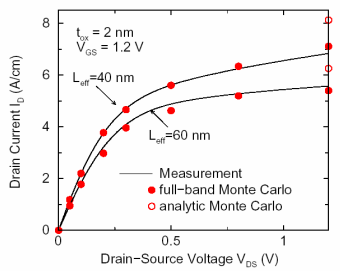


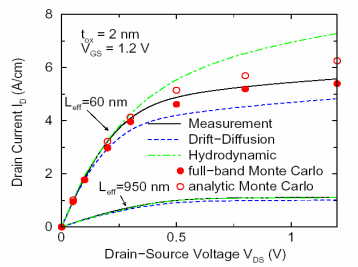


SPARTA™ : Monte Carlo Simulations



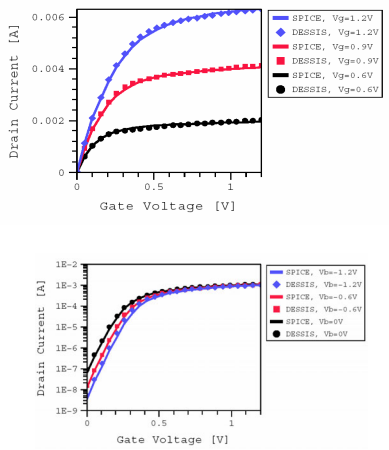






ISExtract™

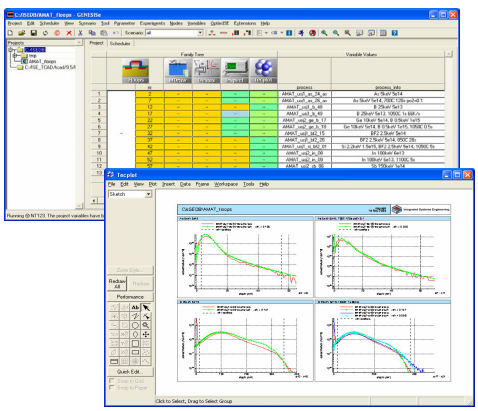
- BSIM3 and BSIM4
- BSIMPD (SOI)
- MEXTRAM 504 (Bipolar, SiGe HBT)
- Gummel-Poon (Bipolar)
- Statistical SPICE Modeling/Sensitivity Analysis
- Direct capacitance extraction
- Global Optimization with Full Parameter Set



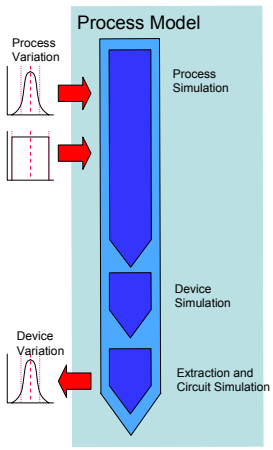
BSIM3 parameter extraction for a NMOS with (L/W)=0.18μm/10μm

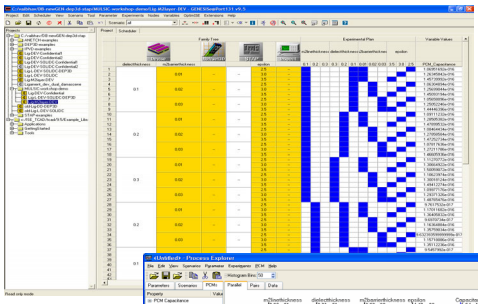
TCAD Fab Package™ for CMOS Calibration

- ISE-TCAD TOOLS
  - GENESISe interface
  - FLOOPS with ChargedPair Diffusion model and MC implant
  - DESSIS, drift-diffusion transport
  - OptimISE integration
- Wizards and viewers for convenient experiment creation and visualization
- Over 240 SIMS for USJ applications from AMAT

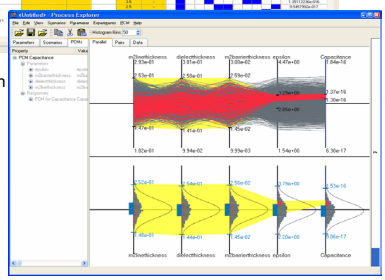


TCAD Derived Process Models





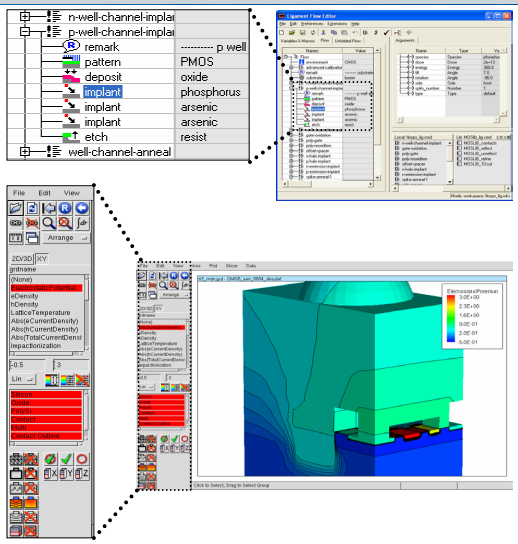
DoE for parametric analysis in GENESISe



ISE Process Explorer for evaluation of process-device relations and yield

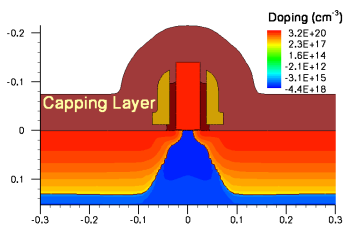
Framework Tools

- GENESISe: convenient simulation environment with a clean, spreadsheet like organization of simulation projects
- LIGAMENT: Process flow editor where the knowledge of the simulator's command line syntax is no longer necessary. Support of recipes/macros/libraries for easy knowledge transfer.
- Tecplot-ISE: with new user interface, fully integrated with ISE menus and sidebar

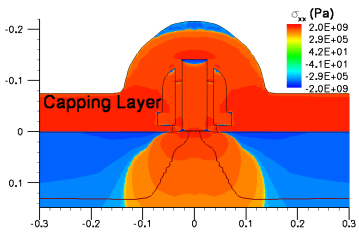


Application Overview

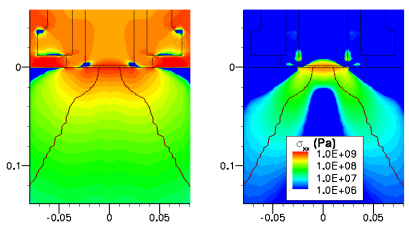
Strained Silicon: NMOS



Doping of strained silicon NMOS

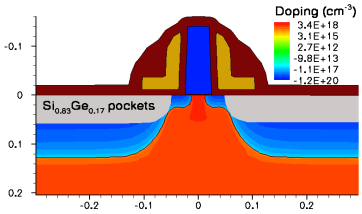


The capping layer is under high tensile strain. This leads to compressive stress in the source and drain regions and in turn to tensile stress in the channel.

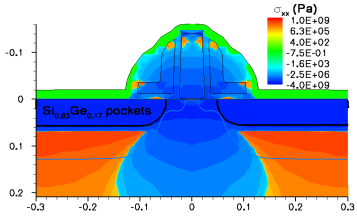


Comparison stress tensor between NMOS transistor with high tensile capping layer (left) and device, simulated with no-stress cap layer (right).

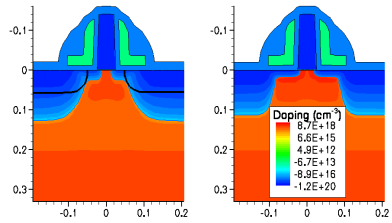
Strained Silicon: PMOS



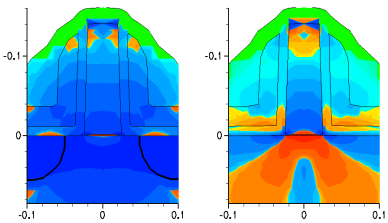
Doping of strained silicon PMOS



Stress tensor after source and drain formation

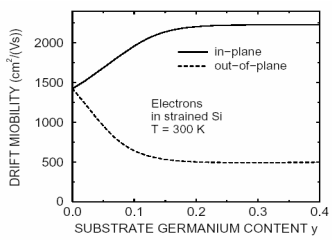


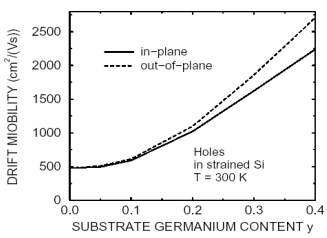
Comparison of final doping in PMOS with (left) and without (right) pockets.

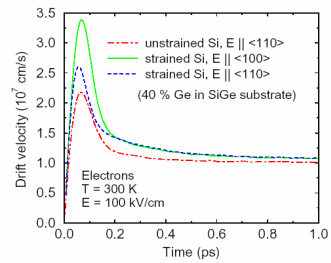


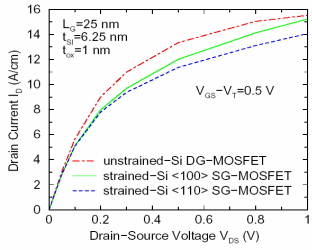
Comparison stress tensor between PMOS with (left) and without (right) SiGe pockets

Strained Silicon: MC Simulations

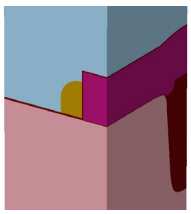




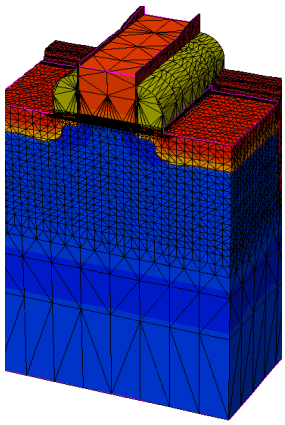




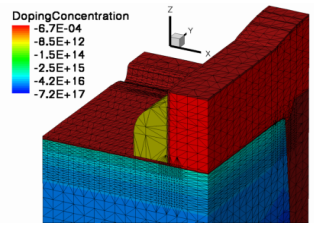
3D NMOS Transistor



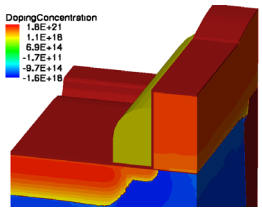
3D Boundary with DEVISE



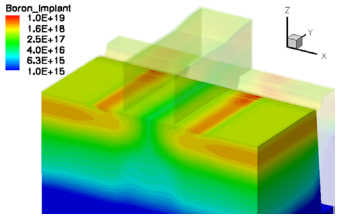
Structure for Device Simulation



Mesh for Process Simulation

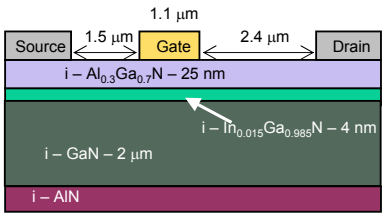


Half of NMOS at the End of Process Simulation

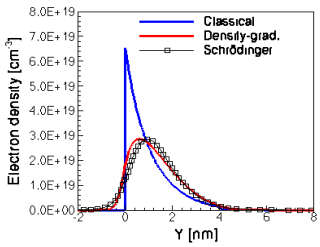


3D Boron Halo Implantation

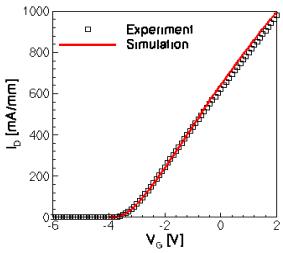
AlGaN/GaN HFET

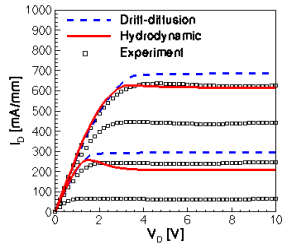


HFET Structure



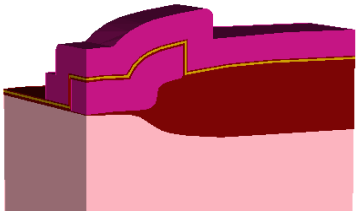
Electron Distribution in the Channel



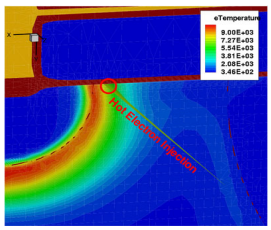


Measurement and Simulation of Transfer and Output Characteristics.

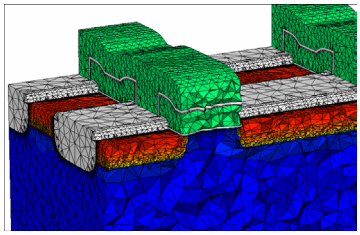
Flash Memory



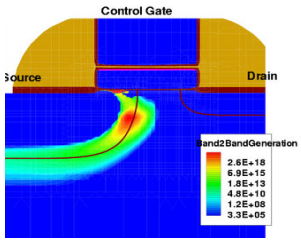
Process Emulation with DEVISE



DESSIS Simulation of Programming

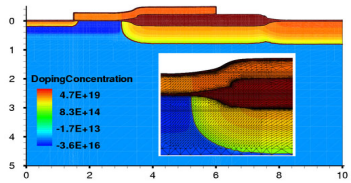


NOFFSET3D Mesh of Flash Cells

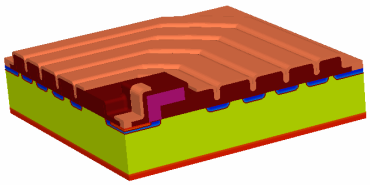


DESSIS Simulation of Erasing

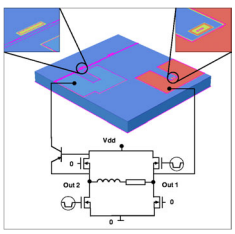
Power Devices



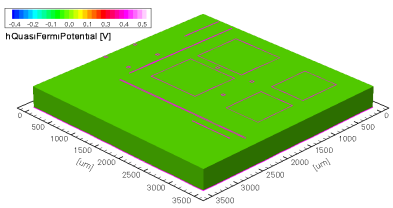
LDMOS with LOCOS in FLOOPS-ISE



Guard Ring Termination



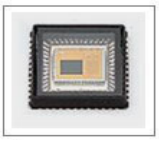
3D Mixed-Mode Full Chip Simulation of Substrate Currents in an H-Bridge



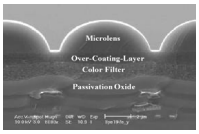
3D Full Chip Simulation of Substrate Potential Distribution

CMOS Image Sensors

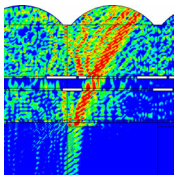
Standard CMOS Image Sensor Applications



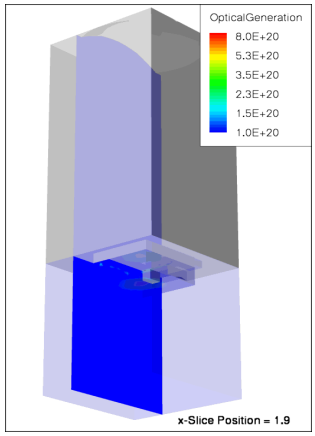
CMOS Image Sensor:
Hynix Semiconductors



SEM picture of a cross-section through microlenses
H.S. Oh, et al., AP-ASIC 2000

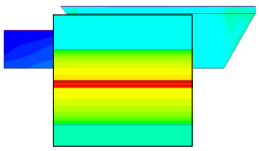


2D EMLAB Simulation of optical cross-talk

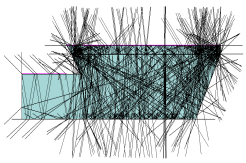


3D EMLAB Simulation of carrier generation in a CMOS image sensor

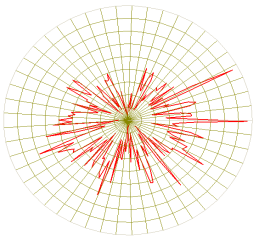
Light Emitting Diodes



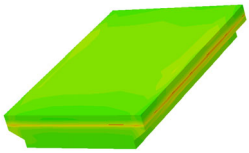
Optical intensity



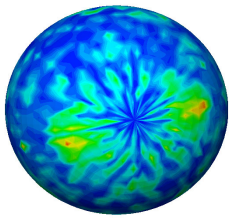
Ray Trace portrait



Emission power angular distribution



Spontaneous emission in quantum wells or bulk regions is considered as radiation source

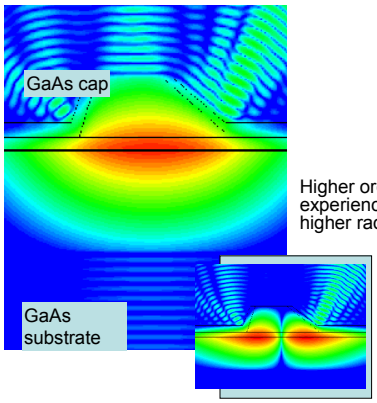


“Far-field” is represented as output intensity projected to the sphere

Edge-Emitting Lasers

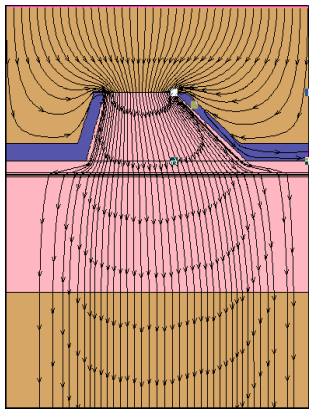
DESSIS-Laser: Edge-Emitting Lasers with Controlled Leakage

Electromagnetic wave radiation towards the higher refractive index GaAs cap/substrate

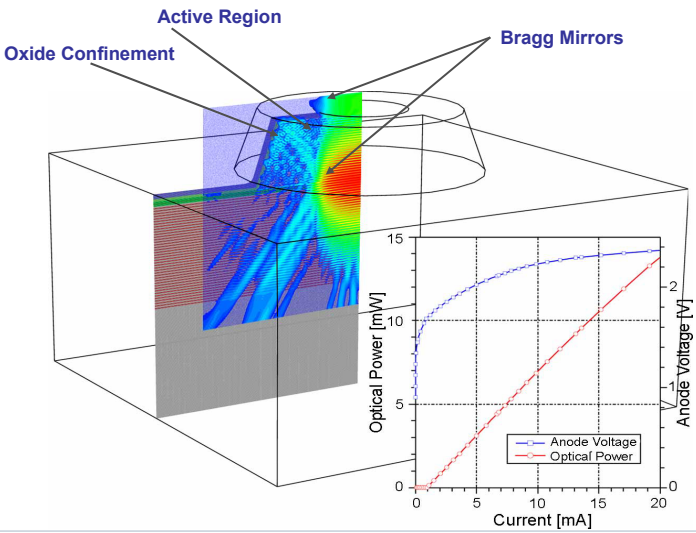


Higher order mode experiences considerably higher radiation loss

Current confinement by AlGaP current blocking regions (in blue)



Vertical-Cavity Surface Emitting Laser

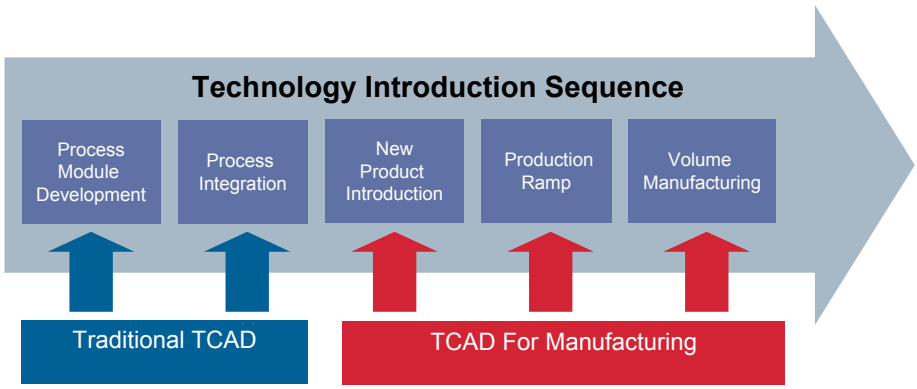


- DESSIS-Laser: Vertical-cavity surface-emitting laser (VCSEL)
- Finite-element type full-vectorial optical mode solver
- Rigorous simulation of diffraction loss and radiating waves
- Simulation includes spatial hole burning and thermal lensing

TCAD for Manufacturing

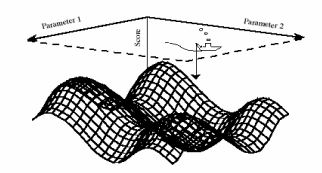
Expand TCAD to Manufacturing

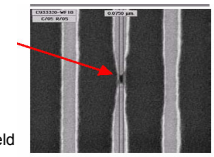
Expanding the use of TCAD to manufacturing is **evolutionary**.



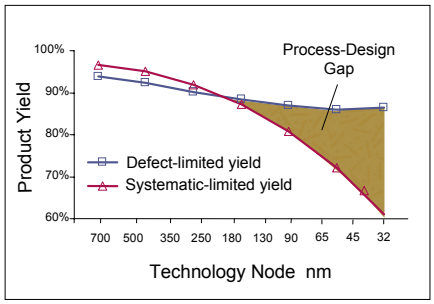
Systematic Yield and TCAD

- Many new products have lifetimes of 8 months or less.
- If a specific IC/SOC design exhibits highly variable yield, attributable to systematic causes.
- TCAD can identify certain root causes that are otherwise difficult to find in low volume products.
- Corner Simulations: Find worst-case scenarios of process, temperature and supply voltage variations.
- Response Surface Modeling:



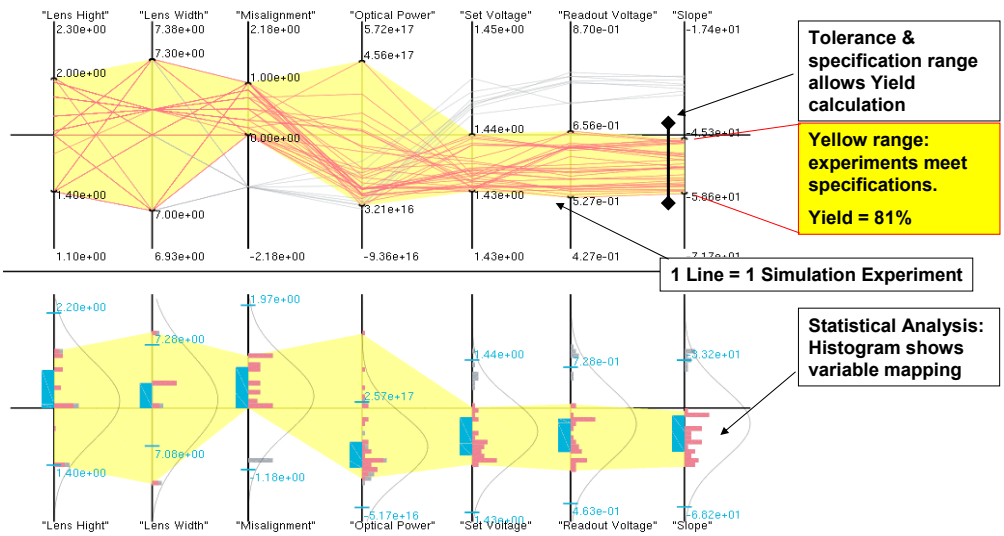


Defect-limited yield

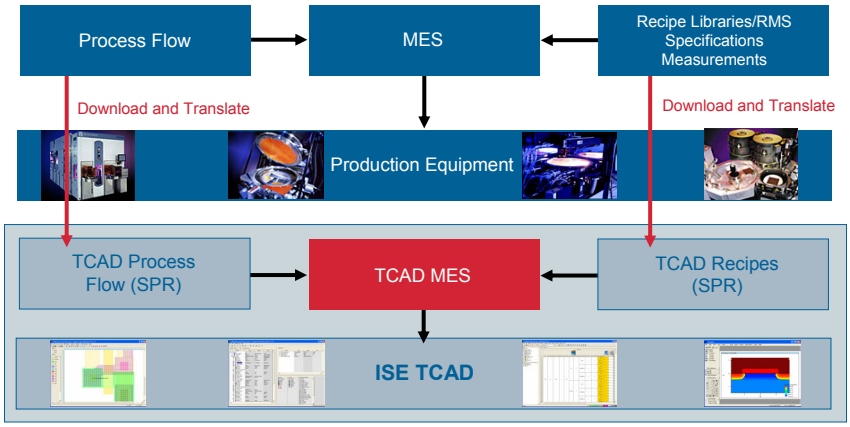


Ref: C.N. Berglund et al., Optical Microlithography XVI, 2003, p. 457

Yield Analysis for a CMOS Image Sensor



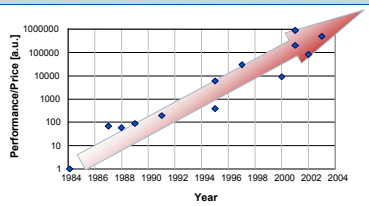
Fab Link™



ISE TCAD: Future

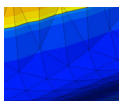
Cluster and Grid Computing

- In 2003, ISE invested in a Linux-based cluster computer for use by Calibration & Services.
- Currently, ISE has 42 Intel Xeon processors (21 nodes, one master), 2.4 GHz, 4 GB RAM per node.
- They are easily extendable by plugging additional nodes into the rack.
- Operates under Red Hat Linux.
- Sun ONE Grid Engine is used for job scheduling.
- Web-based access to load statistics is through the Ganglia toolkit.

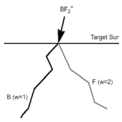


Rack view of MATRIX cluster

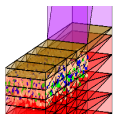
Process Model Hierarchy



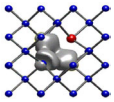
- Continuum approximation
  - Analytic implantation
  - Programmable PDE solver (Alagator)



- Atomistic implantation
  - Monte Carlo implantation
  - Crystal-TRIM



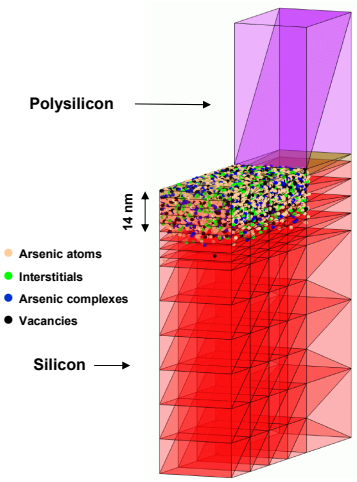
- Atomistic diffusion
  - Kinetic Monte Carlo

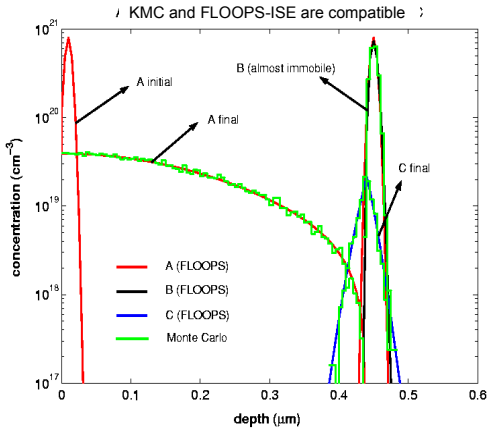


- First principle / *Ab initio*
  - Molecular dynamics
  - VASP (Vienna *Ab Initio* Simulation Package)

AtomISE™

Kinetic Monte Carlo Simulation



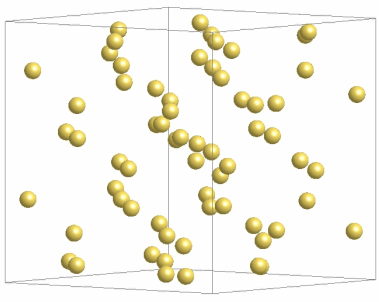


1 keV As implantation 10^{14} cm^{-2}, 5 s at 700°C.

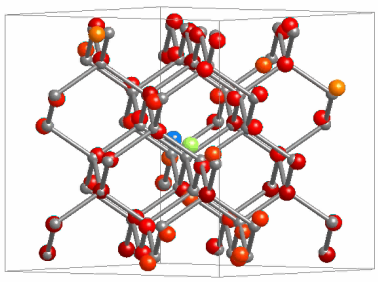
E. Alonso (ETH Zurich)

Self-Interstitial Diffusion in Silicon

Ab Initio Calculation of Diffusion Coefficient



Raw data produced by VASP: Thermal motion of silicon atoms.

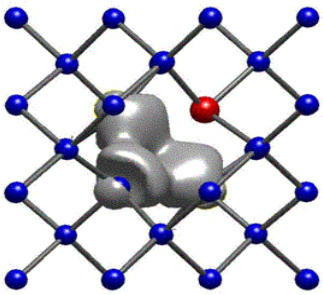


Distance from lattice (gray): Red balls are near the lattice site, and the blue and green balls are farther away.

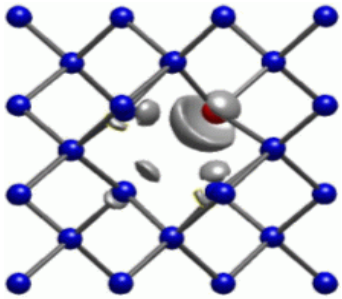
B. Sahli ETH Zurich, TOP NANO 21 (KTI Project)

Arsenic Activation and Deactivation

First-Principle Calculations Provide Strong Evidence That Dopant-Vacancy (As-V) Clustering Is Responsible for Arsenic Deactivation



The first acceptor state constitutes a bond between the Si atoms (blue) adjacent to the vacancy (center). Arsenic is red.



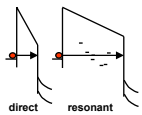
Donor state

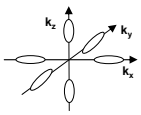
C. Müller ETH Zurich: TOP NANO 21 (KTI Project)
Physical Review B 68, 045208 (2003)

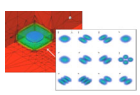
Device Model Hierarchy

$$\vec{J}_n = -nq\mu_n \nabla \phi_n$$

$$\vec{J}_p = -pq\mu_p \nabla \phi_p$$

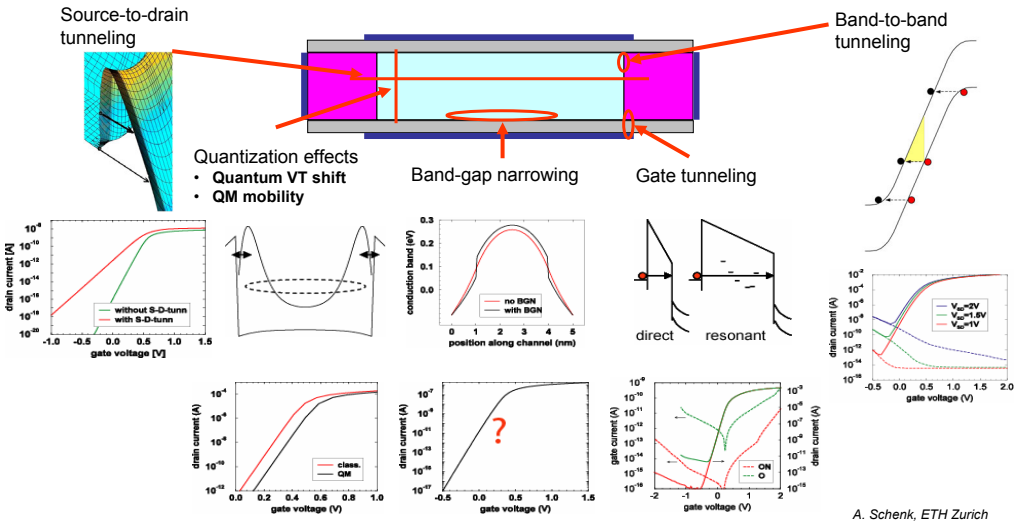






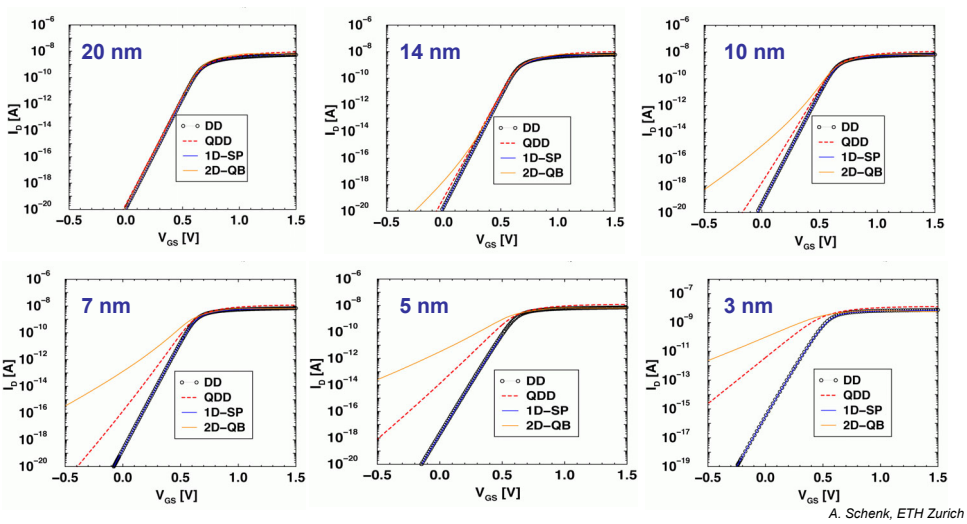
- Continuum approximation
  - Drift-diffusion
  - Hydrodynamic
- Quantum models
  - Van Dort
  - Density gradient, Schrödinger
  - Tunneling
- Atomistic modeling
  - Monte Carlo transport models
- Single electron simulation
  - SIMNAD

Five Quantum Effects



A. Schenk, ETH Zurich

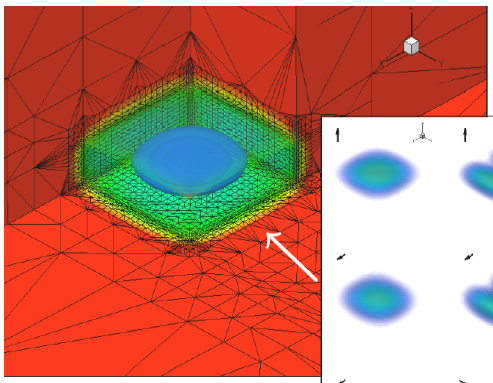
Source-Drain Tunneling as Function of Lg in QDD



A. Schenk, ETH Zurich

Quantum Transport

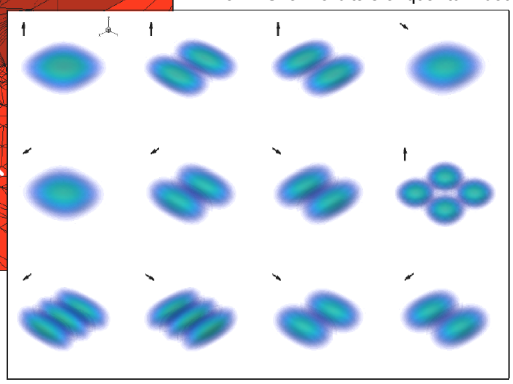
Quantum Dot Flash RAM



SIMNAD charge density on DESSIS mesh.

F. Heinz ETH Zurich: NANOTCAD (supported by EU and Swiss Federal Office for Education and Science).

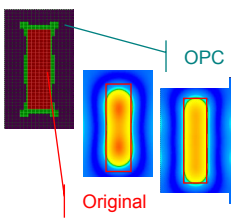
Kohn–Sham orbitals of quantum dot.

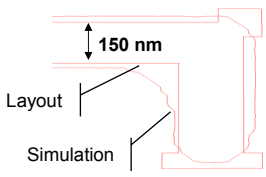


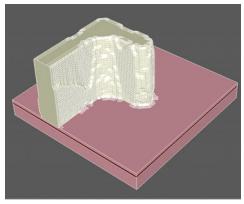
Lithography Simulation 1

Lithography

- Extremely crucial for tight dimensional control
- Central and crucial step in parametric yield
- OPC and PSM





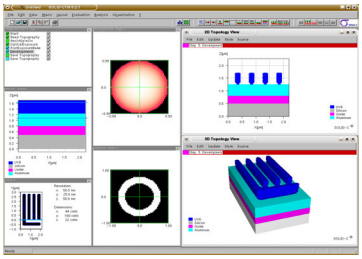


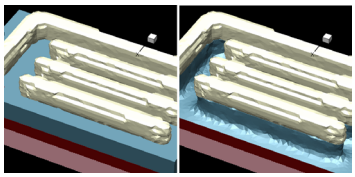
Lithography Structure from Solid-C (Sigma-C, FhG) in DEVISE

Evaluation/Status

- For geometric construction, footprint may be sufficient; for physical simulation, full resist shape needed
- Resolution of fine details in uniform cell-based mesh can be an issue
- Cell-based output needs considerable simplification

Lithography Simulation 2

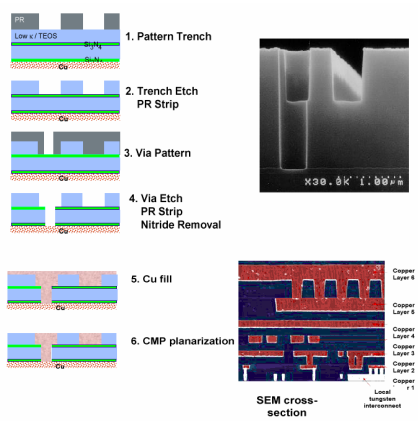




Lithography simulation in Solid-C on a 3-D DEVISE structure and subsequent etch step using ANETCH

- The lithography simulation tool Solid-C is integrated through LIGAMENT.
- DEVISE generates the 3-D structure which is supplied to Solid-C along with the layout information for lithography simulation.
- Solid-C generates the resist pattern using a cell-based approach.
- The structure is output and imported back in DEVISE.
- Decimation/smoothening tools (YAMS, Smooth3D) are required to allow further geometric operations on the structure.

Back-end Simulation (MULSIC) 1



Focusing on dual-damascene process

IST Project 2000-30133 MULSIC with FhG-IISB, TU Vienna, ISE
Process simulation software modules from FhG, integrated into ISE TCAD: GENESISe, LIGAMENT, DEVISE

Deposition
- PECVD (plasma-enhanced chemical vapor deposition) for dielectric deposition
- IPVD (ionized physical vapor deposition) for barrier layer
- Electroplating: superconformal vapor deposition: for trench and via filling

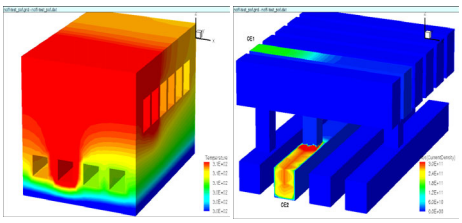
Lithography: Solid-C
- Only integration as part of MULSIC

Etching
- Dielectric etching

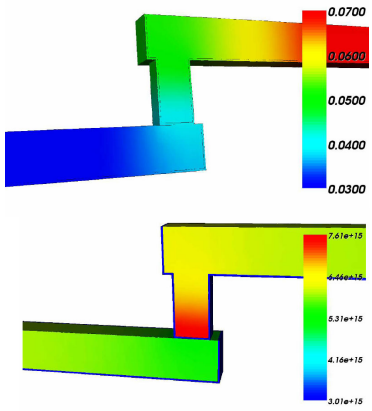
Planarization (CMP)
- Dielectric planarization
- Copper planarization

Back-end Simulation (MULSIC) 2

In MULSIC, TU Vienna concentrates on thermo-electro-mechanical simulation of interconnects as well as on the simulation of electromigration and electromigration promoting factors



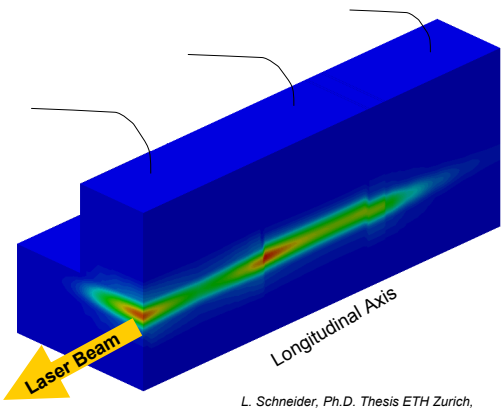
Temperature and current density distribution computed using STAP from TU Vienna



Electric field distribution (top) and vacancy concentration in interconnect structure with barrier layer

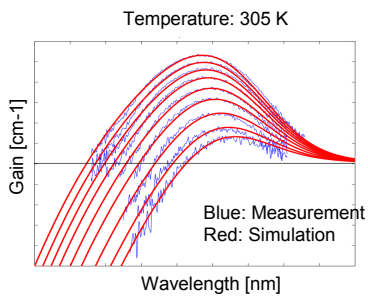
Optoelectronics Outlook

Full 3D Edge-Emitting Laser Simulation
Example: Ridge Waveguide Multisection Sampled-Grating DFB



L. Schneider, Ph.D. Thesis ETH Zurich, presented at NUSOD-03 Conference.

State-of-the-Art Active Region Models:
- k·p band structure
- Many-body gain



M. Luisier, Ph.D. Thesis ETH Zurich.

ESD

Introduction

- Charged objects discharge to IC pins
  - With very high currents (up to 10 or more A)
  - With rather short discharge duration (1ns to 200ns)
- Electro static discharge is a major threat for integrated circuits reliability:
  - Approximately 25% of total IC failures due to ESD
  - During manufacturing, assembly, shipment, and in the field
- Typical ESD models for test & specification:
  - Human Body Model (HBM)
  - Machine Model (MM)
  - Charged Device Model (CDM)

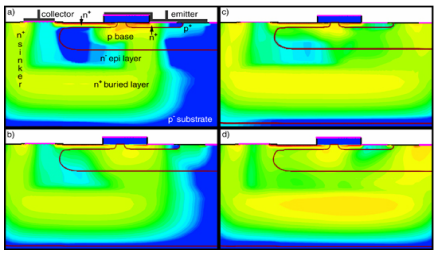
ESDEM Research Project

ESPRIT research project:

ESD Design Methodology

- Project with partners
  - Robert Bosch GmbH
  - IZM-FhG
  - STMicroelectronics
  - University of Bologna
  - ETHZ
  - IMEC
  - ISE AG
- Focus on
  - Development and validation of TCAD-based ESD design methodology
  - Development and calibration of high-temperature models
  - ESD compact models

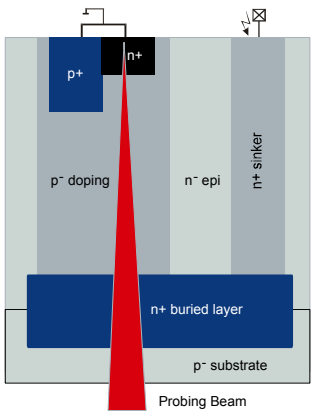
www.iis.ee.ethz.ch/nwp/esdem/



Device simulation of a bipolar protection element with lateral and vertical operation modes. The resulting current distribution is shown.

DEMAND Research Project

- IST-2000-30033 DEMAND:
- **Design Methodology for Enhanced Device Robustness**
- Partners
  - Infineon Technologies
  - University of Bologna
  - TU Vienna
  - ETH Zurich
  - ISE AG
- Focus
  - consistent methodology for designing robust devices
  - New optical and electrical characterization techniques at high temperatures
  - physical models for device simulation in the temperature range above 700K under high current conditions

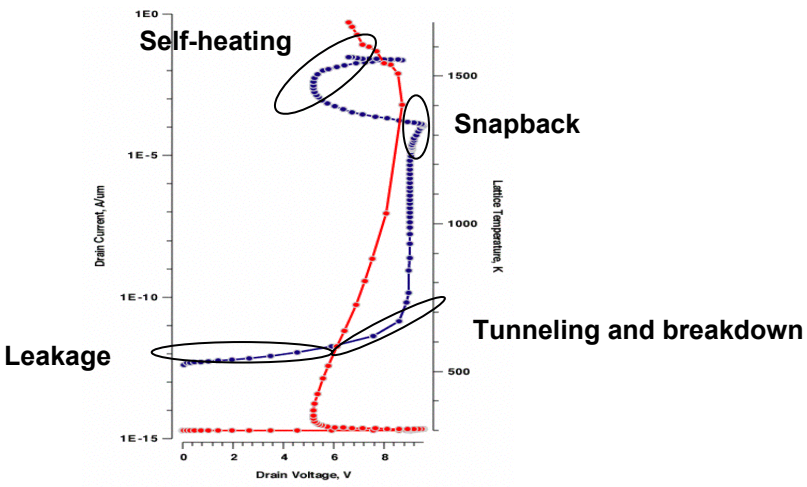


Simplified cross section of a electrostatic discharge protection device. The Position of the probing laser beam with a spot size of 1.5µm is indicated.

DESSIS: ESD Focused Features

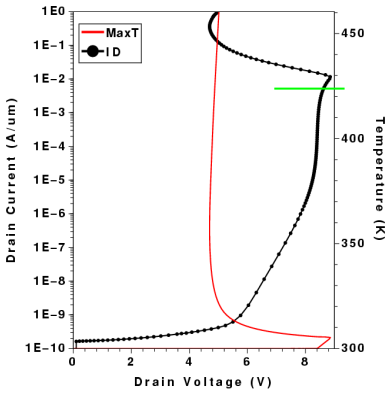
- Advanced Models for CMOS
  - Transport models: Drift-Diffusion, Energy-Balance
  - Quantization models: VanDort quantum correction, density gradient
- Thermo-electrical effects
  - Self-heating mechanisms and heat flows
- Mixed-Mode
  - Electrical test circuit
  - Package equivalent thermal network
- Impact Ionization
  - High-temperature calibrated models (University of Bologna)
- Band-to-band tunneling
  - Non-local tunneling, phonon-assisted Schenk model
- Hot Carrier Injection
  - Fowler-Nordheim tunneling
  - Degradation model at Si/SiO_2 interface

ESD Dynamics

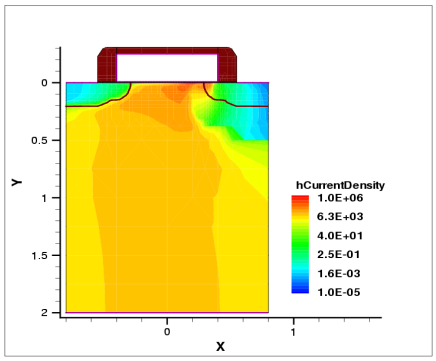


Example : ggnMOS Breakdown

Snapback characteristic



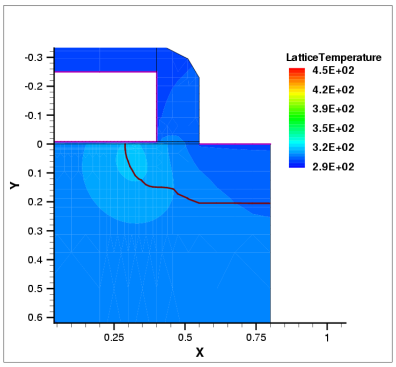
Hole Current at I_d=0.01A/µm

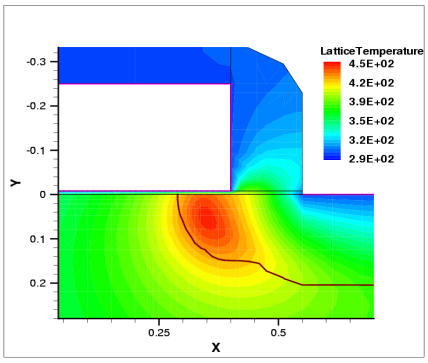


Parasitic bipolar device is triggered

Example : ggnMOS Breakdown

Lattice temperature at I_d=0.1A/µm and I_d=0.9A/µm





Parasitic bipolar saturates with device self-heating

FLOOPS: Advantages for ESD

- Most advanced diffusion models for accurate process simulation results
- Stress dependant oxidation providing more realistic geometry description
- Proven/effective auto-adaptive mesh generation
  - 2D delaunay meshes
  - Mesh refines and *de-refines* during structure formation
  - Dynamic meshing ➔no hard-coded limit on mesh size
- VLSI/DSM calibration

DESSIS: Advantages for ESD

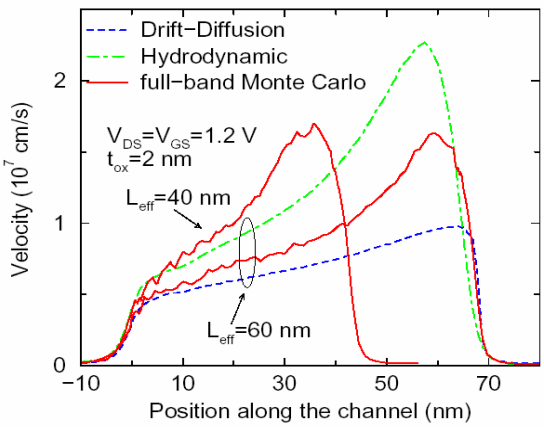
- Most advanced physical models
- Robustness with thermodynamic and hydrodynamic models
  - Transient and static analysis
  - Rock solid convergence even for extremely difficult simulation (breakdown, hydro and non-local tunneling)
- Electrical and thermal circuits
- High-efficiency linear solvers
- 2D – true 3D simulator
  - Consistent models and syntax extended

Conclusion

- ESD problems are complex and difficult to comprehend – TCAD is an ideal tool for device analysis and optimization
- ESD simulations are *the* ultimate performance test for TCAD applications
- Simulations “copy” the actual stress experiments (HBM, CDM, TLP)
- ESD TCAD is in daily use in industry

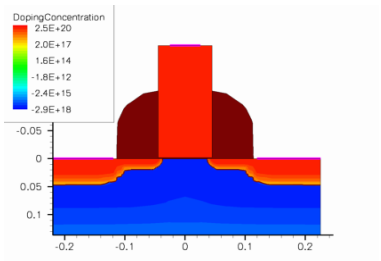
Hot Carrier Effects

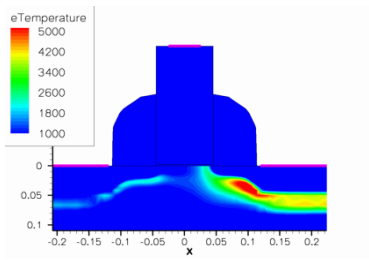
Velocity Profiles along the Channel

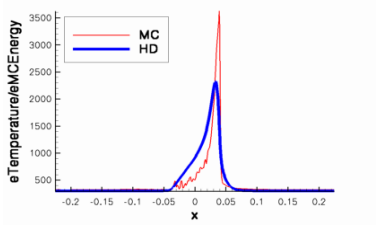


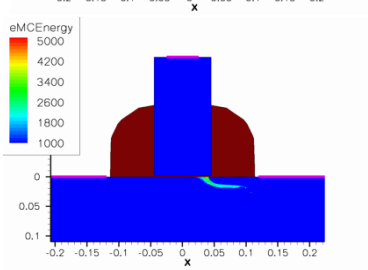
Velocity in source–side of channel determines on–current

Hydro vs. Monte Carlo

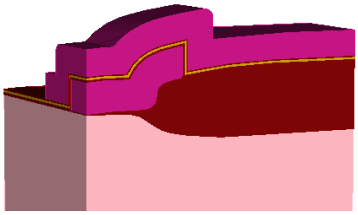




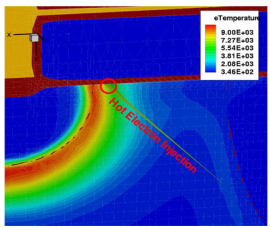




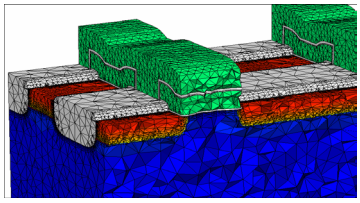
Flash Memory



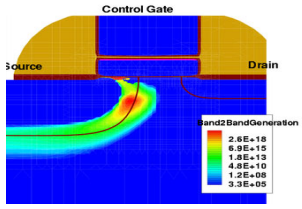
Process Emulation



Simulation of Programming



Mesh of Flash Cells



Simulation of Erasing

Degradation

Introduction

- Device degradation due to:
  - Trapping of injected charges
  - Trap generation
  - Oxide break down
  - Hot carrier effects
  - Ion Drift
  - Interdiffusion of metals
  - Stress migration
  - Mechanical effects

Introduction

Important factor in CMOS Device degradation:

- Time depended trap generation at the Si/SiO_2 interface

Processing:

- ~ $10^{12}cm^{-2}$ dangling Si bonds at the interface
- Passivation with hydrogen

Device operation:

- Hot carrier break Si-H bond
  → new dangling bond acts as interface trap

Generalized Hess Model

Electro-Chemistry of Silicon Interface Bond
Passivation and Break-Up

- Passivation with Deuterium

$$\equiv \mathrm{Si} - \mathrm{H} + \mathrm{D}_2 \rightarrow \equiv \mathrm{Si} - \mathrm{D} + \mathrm{HD}$$

- Passivation with Hydrogen

$$\equiv \mathrm{Si} - + \mathrm{H}_2 \rightarrow \equiv \mathrm{Si} - \mathrm{H} + \mathrm{H}$$

- Hot Carrier Depassivation

$$\equiv \mathrm{Si} - \mathrm{H} + \mathrm{hot\,carriers} \rightarrow \equiv \mathrm{Si}^{*} + \mathrm{H}$$

DESSIS Trap Formation Model

- First-order kinetic equations for hydrogen on Si-H bonds at the Si/SiO_2 interface

$$\frac{dn}{dt} = -k \cdot n + \gamma\left(N - n\right)$$

where

- Unbroken Si-H bond conc.: *n*
- Total Si-H bond concentration: *N*
- Depassivation rate: *k*
- Repassivation rate: γ

New model field dependent activation energy model :
Penzin, Hess et at. IEEE T-ED 50, p. 1445 (2003)

Model Parameters

Depassivation rate depends on:

- Hot carrier current through oxide
- Fowler-Nordheim current through oxide
- Si-H bond activation energy

"Hot Carrier Enhancement"

Activation energy depends on

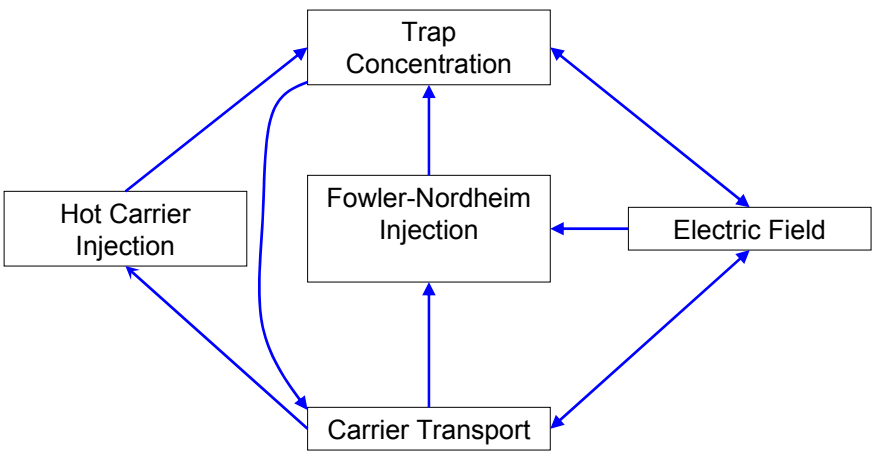
- Electric field
- Concentration of released hydrogen

"Field Enhancement"

Repassivation rate

- Computed automatically to ensure thermal equilibrium conditions
- Also user definable

Self-Consistent Transport



User Accessible Parameters

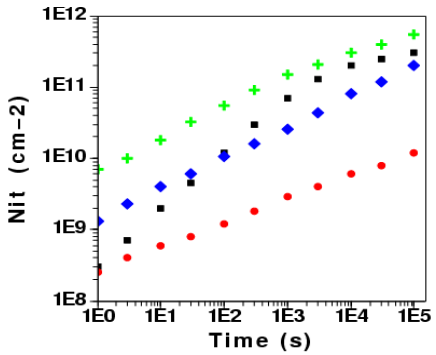
- Depassivation and Repassivation rates
- Enhancement factors for depassivation rate
  - Electric field dependency
  - Fowler-Nordheim current dependency
  - Hot carriers current dependency
  - Passivation Temperature and volume
- Activation energy
- Correction factors for activation energy
  - Electric field dependency
  - Si-H chemical potential dependency
- Total concentration of Si-H bonds

Degradation: Experimental Data

0.35 μm CMOS Technology with T_{ox} = 65 Å

Experimental stress conditions:

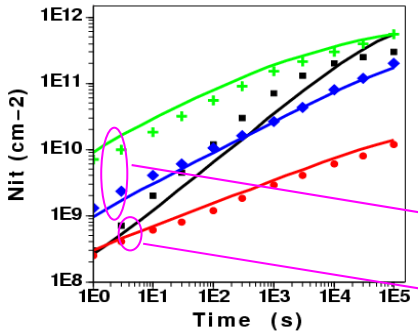
1. **V_{gs}= -9V V_{ds}=V_{bs}=0**
2. **V_{gs}= 12V V_{bs}=0 D&S floating**
3. **V_{gs}= 1V V_{bs}=-11V, V_{ds}=0**
4. **V_{ds}= 5.5V V_{gs}=2.5V, V_{bs}=0**



Experimental results cannot be described without new field enhancement model

Degradation: Generalized Hess Model

Simulation vs. experiment



Oleg Penzin, A. Haggag, W. McMahon, Eugeny Lyumkis, and K. Hess.
MOSFET Degradation Kinetics and Its Simulation.
IEEE Transactions on Electron Devices, 50(6), June 2003.

Passivation & HC Degradation by Hess

$$\equiv Si - + H_2 \rightarrow \equiv Si - H + H$$

$$\equiv Si - H + D_2 \rightarrow \equiv Si - D + HD$$

$$\equiv Si - H + \text{hot carriers} \rightarrow \equiv Si^* + H$$

Kinetic Equation for Si-H Bonds

$$dn/dt = k \cdot n - \gamma(N - n)$$

$$k = k_0 \exp(-\varepsilon_A / k_B T)\, k_H$$

HC Enhanced

$$k_H = 1 + \delta_{HC} |I_{HC}|^{\rho_{HC}}$$

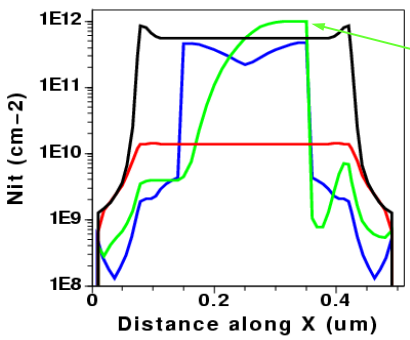
Field Enhanced

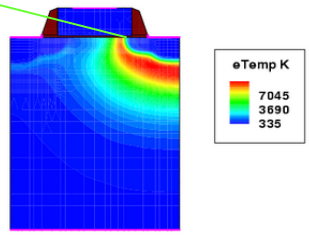
$$\varepsilon_A = \varepsilon_A^0 + \delta |F|^{\rho} + (1 + \beta_\perp F_\perp) \cdot k_B T \cdot \ln\left(\frac{N - n}{N - n_0}\right)$$

Degradation: Interface Trap Formation

Trap Distribution along the Channel for Different Stress Conditions:

- V_{gs}= -9V $V_{ss}=V_{ds}=V_{bs}=0$
- V_{gs}= 12V $V_{bs}=0$ D&S floating
- V_{gs}= 1V V_{bs}=-11V, $V_{ss}=V_{ds}=0$
- V_{ds}= 5.5V V_{gs}=2.5V, $V_{ss}=V_{bs}=0$





Prediction of Device Reliability

Device life time τ_D

- Device operation time until a critical average trap concentration is formed ($N_{crit} = 10^{11}cm^{-2}$)

Methods for extraction:

1. Direct simulation of stressed device for 30 years
2. Extrapolation from accelerated stress experiments

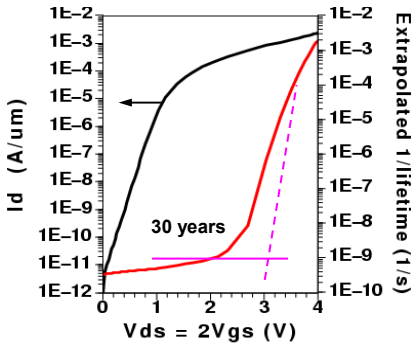
Extrapolation Procedure

1. Perform transient simulation of *stressed* device and extract
   - Effective depassivation rate k_{stress}
   - Device life time τ_{stress}
2. Perform steady state simulation for *normal* operation and extract
   - Effective depassivation rate k
3. Compute

$$\tau_D = \frac{k_{stress}}{k} \tau_{stress}$$

Simulation of Device Lifetime

Direct Simulation for 30 Years vs. Extrapolation



- High stress conditions: both methods agree
- Low stress conditions: extrapolation grossly underestimates lifetime

Pros and Cons

- Extrapolation Method
  - Fast, single simulation for τ_D vs. bias curve
  - Underestimates lifetime (no repassivation)

    good getting a lower bound quickly

- Direct Method
  - Long simulation times for each bias point
  - Accurate physics including repassivation

    accurate values for low stress conditions

Conclusion

- DESSIS features a unique degradation model
  - Rich and physical parameterization
  - Good agreement with experimental data

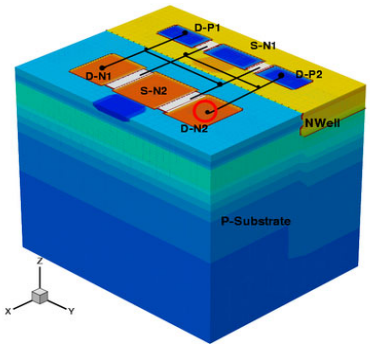
Radiation

Radiation – Single Event Upsets

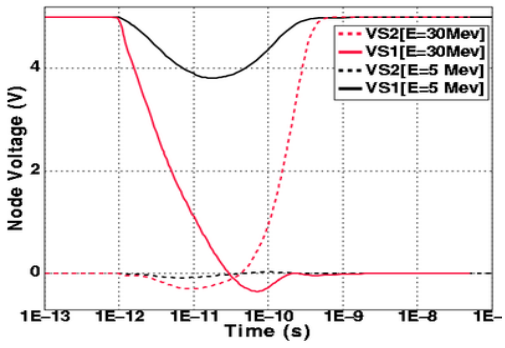
- 2D and 3D transient simulation of Single Event Upsets by:
  - Alpha particles
  - Heavy Ions
  - Neutrons – Multi-trajectories of secondary ions
- Applications:
  - 3D full cell SRAM Single Event Upset
  - 3D CMOS Inverter Latch-Up
  - 3D multi-trajectory of secondary particles from Neutron radiation

Heavy Ion: 3D SRAM Cell Upset

3D SRAM structure



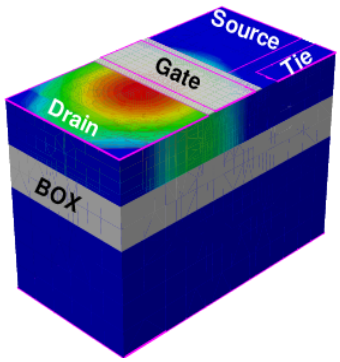
Node voltage response for 2 heavy ion energies



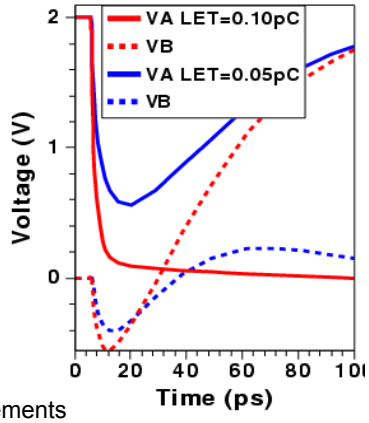
- The ion strikes into the drain of the off-nMOS
- SRAM cell flips at high incident particle energy

Heavy Ion: SOI SRAM Cell Upset

Deposited 3D charge profile



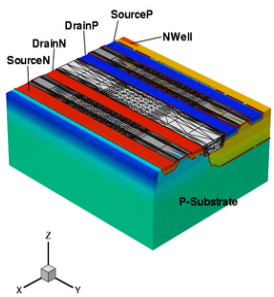
Voltage response for various ion energies



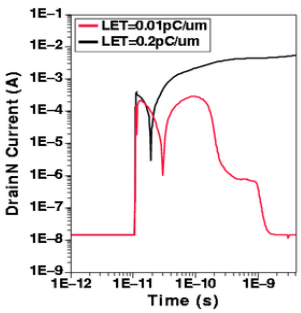
SEU can be modeled using a mixed-mode approach including part of the system as Spice elements

Heavy Ion: CMOS Inverter Latch-Up

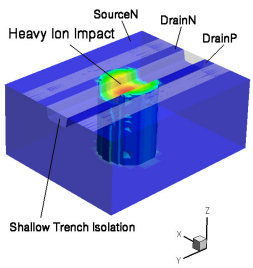
CMOS inverter structure



Current response for 2 LETs



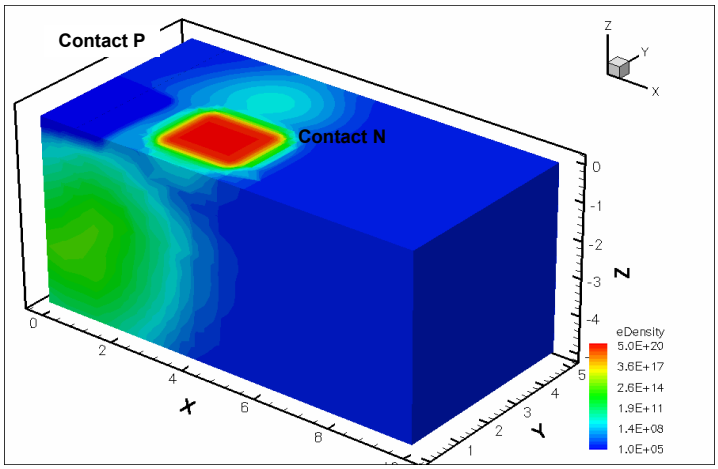
Ion impact on CMOS structure



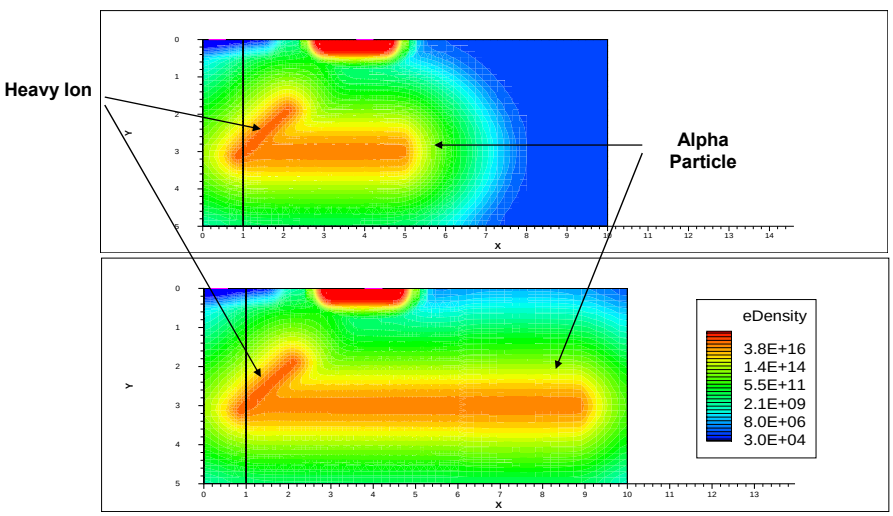
Because of parasitic bipolar effects in CMOS structure, the device latches up when the incident particle energy is high enough

Neutron Radiation

Induced electron density in 3D diode with two ion-trajectories



Neutron Radiation, Multi-tracks of Secondary Particles

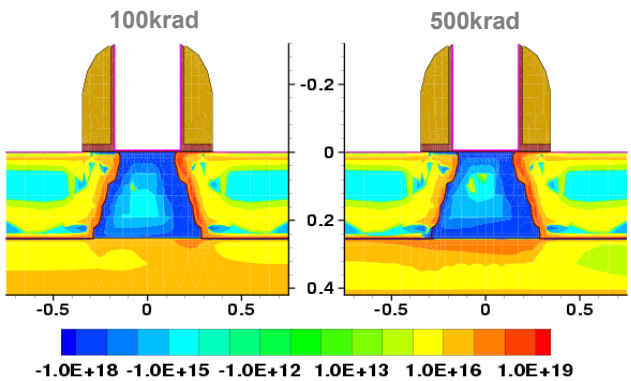


Radiation – Total Dose Effects

- Charge trap models:
  - VMODEL
  - JMODEL
- Developed in cooperation with CEA, France
- Model parameters calibrated by CEA
- Transport in insulators
  - Oxide as semiconductor
  - Spatial trap distribution
- Charge capture in insulator

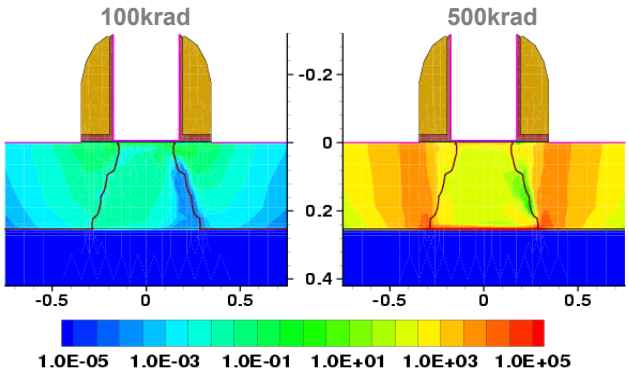
Total Dose Effect - SOI NMOS Transistor

Space Charge Distribution after irradiation



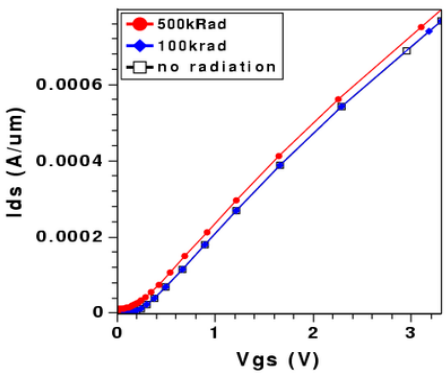
Total Dose Effect - SOI NMOS Transistor

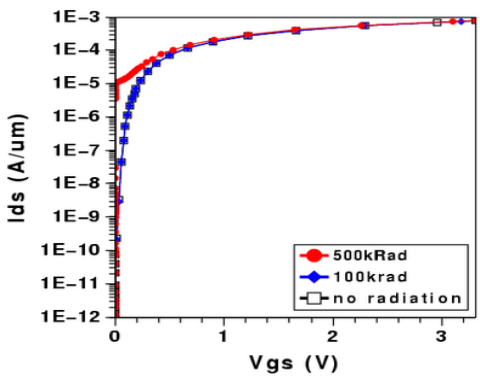
Electron Current Density Distribution



SOI NMOS Transistor

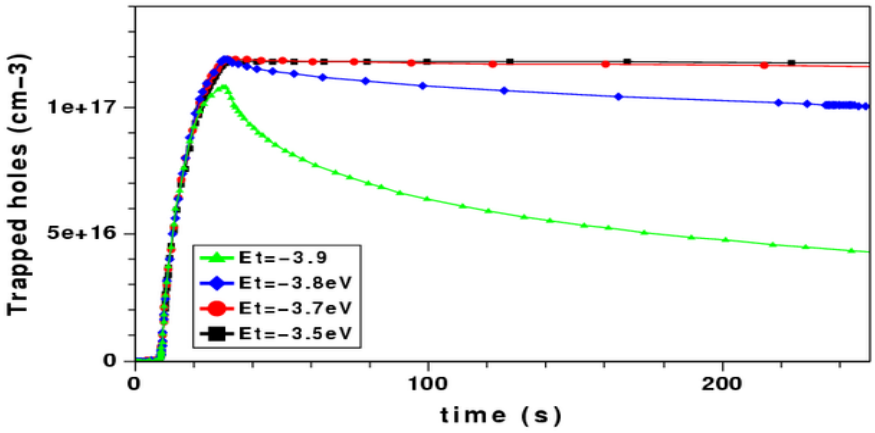
I_{ds} versus V_{gs} (V_{ds} = 3.3V) – After Irradiation





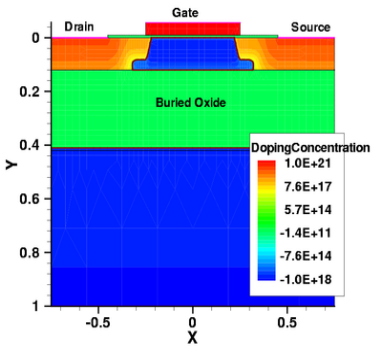
SOI NMOS Transistor

Trapped holes versus time (Vds = 3.3V) – After Irradiation

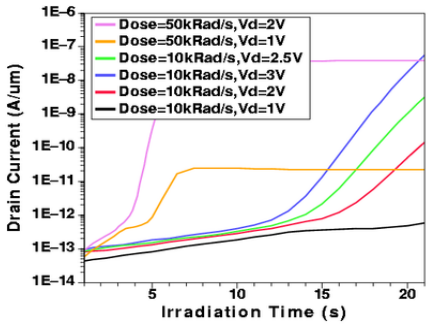


Total Dose Effect: SOI nMOSFET

SOI nMOS transistor structure



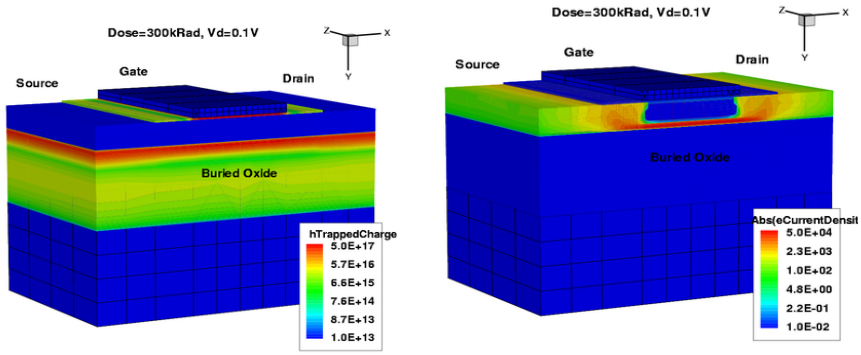
Drain current vs. irradiation time



The leakage current increases with the dose and drain bias showing electric field dependence

Total Dose Effect: 3D SOI nMOSFET

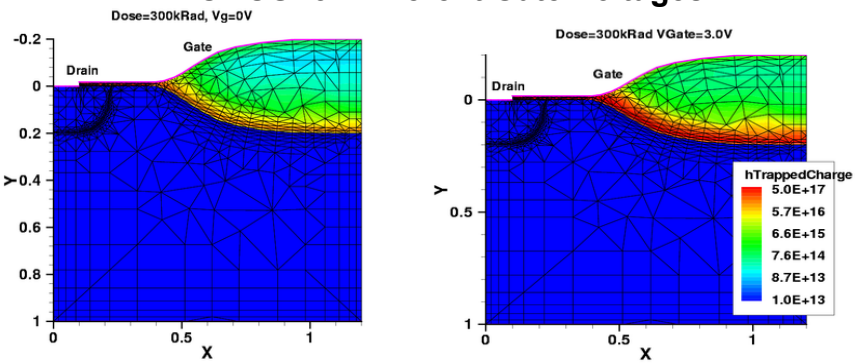
Trapped Hole and Electron Current Distributions in 3D SOI nMOS after 300kRad Irradiation



Expected trapped hole profile in the buried oxide and induced back-channel are observed in 3D

Total Dose Effect: LOCOS Isolation

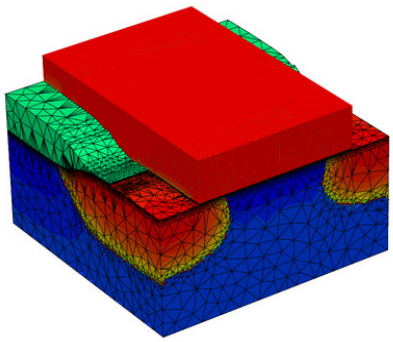
Trapped Hole Distribution in Irradiated LOCOS for Different Gate Voltages



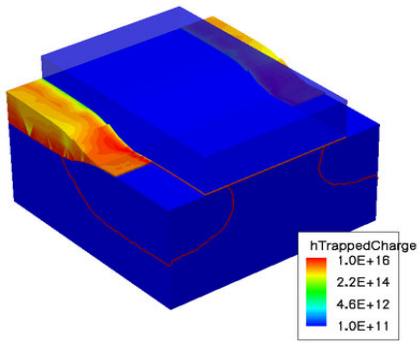
Noffset meshing resolves the interface of non-planar isolation and accurately captures trapping dependence on polarization

Total Dose Effect: 3D nMOS w/ LOCOS

Noffset meshing of 3D



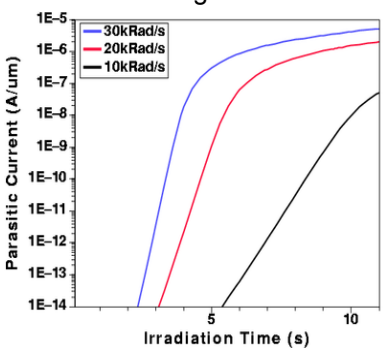
Trapped hole density after 10kRad irradiation



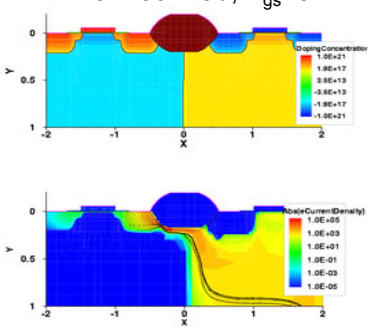
Noffset3D, normal offsetting mesh, creates fine grid along the interfaces where traps are located

Total Dose Effect – Simple CMOS Inverter

Transient evolution of the leakage current during irradiation



Electron current density distribution for 200kRad, V_{gs}=3V



Leakage current in CMOS structure appears close to the thick oxide and leads to failure of the device functionality

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