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BR1487/D
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Thermal Modeling Brochure

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Note from the Editor

One of the major challenges facing the designers of today's portable electronic equipment is thermal management. As the end users demand more and more features in handheld battery powered devices such as notebook computers and cellular phones, the designers are faced with new issues and challenges as to "how to get the heat out." Although, thermal management of power semiconductors has always been an issue, the problem of higher power in smaller packages is a major issue more than ever and will continue.

As the discrete semiconductor devices get smaller and power levels continue to increase, electronic designers need to continually challenge traditional methods of design and develop more reliable product designs.

This publication is a collection of technical papers that were published in 1996. It is intended to give insight into the latest methods of thermal measurement and modeling of the discrete surface mount packages which are so commonly used in many of the handheld battery powered applications.

The authors have strived to provide information which can save the circuit designer an appreciable amount of time, effort and expense using the latest techniques in thermal modeling of discrete surface mount packages.

Dave Hollander
ON Semiconductor

Thermal Compendium

Table of Contents

Basic Semiconductor Thermal Measurement

Gary E. Dashney

Abstract

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- Understanding basic semiconductor thermal parameters
- Semiconductor thermal test equipment
- Thermal parameter test procedures
- Using thermal parameters to solve often asked thermal questions

Thermal Characterization of the SO–8 Package for Power Semiconductor Applications

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Abstract

A very up–and–coming package for power semiconductor applications is the SO–8 (also known in the IC world as the SOIC8) package. The purpose of this work is to present the thermal characterization (with emphasis on R_{thja}), both measured and modeled, of this package configured with a power transistor. The paper presents in detail results of characterizing three different package configurations: a) dual die, b) single large die, and c) single small die. The dual die and single large die configurations were used to establish the finite element model accuracy. The model was then used to predict the thermal performance in the untested single small die configuration. The model predictions matched the measured results thus validating the modeling effort. Factors such as solder voiding, die attach technique, junction depth, convective heat transfer coefficient and die thickness that could affect the modeling results were examined and their criticality assessed. As a verification to the modeling and measurements, infrared images were also made of the devices while under test.

New Models and Techniques for Analyzing the Power Transistor and Its Thermal Environment

Kim Gauen

Abstract

In many electronic systems, power transistors perform critical system functions. They also can account for a significant portion of the total system cost. Better performance can come at a higher price, but balancing this price/performance tradeoff has not been easy for designers. Thermal issues are involved, and the tools for analyzing the electrical/thermal environment have not been available. Recently, new tools have become available and techniques are now appearing for sophisticated analysis of the power transistor and its thermal environment.

This paper describes one set of tools and some techniques for thermal/electrical analysis. Because the power MOSFET is so popular, it is one of the first devices to be characterized for such evaluations and it is the focus of this paper.

SPICE Generates Thermal Response Models of a Power Semiconductor

Gary E. Dashney
Larry Walker

Abstract

An equivalent electric circuit consisting of a resistor–capacitor network can be used to describe both the steady–state and transient thermal response of a power semiconductor device. Combined with SPICE, this network is extremely useful in determining a device's junction temperature for any input power condition or waveform that can be modeled in SPICE. This paper covers the following topics:

- Understanding basic transient thermal response of power semiconductors
- Basic transient thermal response test methods
- The thermal equivalent SPICE model
- Examples of using SPICE to model transient thermal response of power devices

Tools for Analyzing the Power Transistor and Its Thermal Environment

Kim Gauen
Heather Neal – Purdue University

Abstract

New models, tools, and techniques are now available for simulating the power transistor and its thermal environment. This paper validates one dynamically temperature dependent power MOSFET model, presents simulation results for a relatively simple thermal network, and shows how more complex networks might be analyzed.

Permissions and Credits

Title	Medium	Credit Line
Basic Semiconductor Thermal Measurement		
Thermal Characterization of the SO–8 Package for Power Semiconductor Applications		
New Models and Techniques for Analyzing the Power Transistor and Its Thermal Environment	PCIM Volume 22, No. 8, August 1996	Reprinted with Permission ©Intertec International
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Tools for Analyzing the Power Transistor and Its Thermal Environment	Proceeding of the 1996 IEEE Workshop on Power Electronics in Transportation October 24–25, 1996 Dearborn, Michigan	Reprinted with Permission ©1996 IEEE

Basic Semiconductor Thermal Measurement

Gary E. Dashney
Motorola Semiconductor Products Sector
Phoenix, Arizona

INTRODUCTION

This paper will provide the reader with a basic understanding of power semiconductor thermal parameters, how they are measured, and how they are used. With this knowledge, the reader will be able to better describe power semiconductors and answer many common questions relating to their power handling capability.

This paper will cover the following key topics.

- Understanding basic semiconductor thermal parameters
- Semiconductor thermal test equipment
- Thermal parameter test procedures
- Using thermal parameters to solve often asked thermal questions

Understanding Basic Semiconductor Thermal Parameters

Heat flows from a higher to a lower temperature region. The quantity that resists or impedes this flow of heat energy is called thermal resistance or thermal impedance.

When the quantity of heat being generated by a device is equal to the quantity of heat being removed from it, a steady state condition is achieved.

To describe the thermal capability of a device, several key parameters and terms are used. They describe the steady state thermal capability of a power semiconductor device.

Key Parameters, Terms, and Definitions

T_J = *junction* temperature

T_C = *case* temperature

T_A = *ambient* temperature

TSP = **T**emperature **S**ensitive **P**arameter

T_R = *reference* temperature (i.e., *case* or *ambient*)

R_{thjr} = junction–to–*reference* thermal resistance

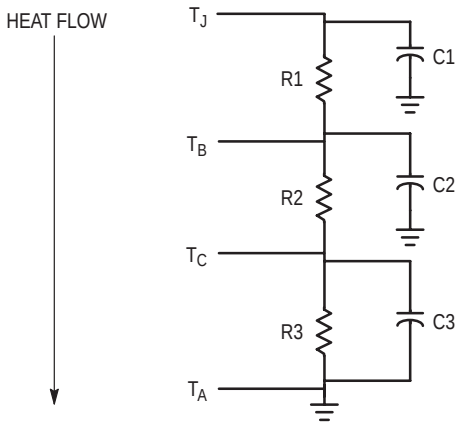
R_{thjc} = junction–to–*case* thermal resistance

R_{thja} = junction–to–*ambient* thermal resistance

$R_{thjr(t)}$ = junction–to–*reference* transient thermal resistance

P_D = power dissipation

The thermal behavior of a device can be described, for practical purposes, by an electrical equivalent circuit. This circuit consists of a resistor–capacitor network as shown.



Heat generated in a device's junction flows from a higher temperature region through each resistor–capacitor pair to a lower temperature region.

Figure 1. Thermal Electrical Equivalent Circuit

Resistors R1, R2, and R3 are all analogous to individual thermal resistance, or quantities that impede heat flow. Resistor R1 is the thermal resistance from the device's junction to its die–bond. Resistor R2 is the thermal resistance from the die–bond to the device's case. Resistor R3 is the thermal resistance from the device's case to ambient. The thermal resistance from the junction to some reference point is equal to the sum of the individual resistors between the two points. For instance, the thermal resistance R_{thjc} from junction–to–case is equal to the sum of resistors R1 and R2. The thermal resistance R_{thja} from junction–to–ambient, therefore, is equal to the sum of resistors R1, R2 and R3.

The capacitors shown help model the transient thermal response of the circuit. When heat is instantaneously applied

and or generated, there is a charging effect that takes place. This response follows an RC time constant determined by the resistor–capacitor thermal network. Thermal resistance, at a given time, is called transient thermal resistance, $R_{thjr(t)}$.

To further understand transient thermal response, refer to ON Semiconductor Application Note AN569, "Transient Thermal Resistance – General Data And Its Use." [4] A detailed discussion of this will not be included here.

Using the key parameters and terms shown earlier, only a few equations are necessary to solve often asked thermal questions.

$$R_{thjr} = (T_J - T_R) / \text{power} \quad (1)$$

$$P_D = (\text{max. device temp.} - T_R) / R_{thjr} \quad (2)$$

$$T_J = P_D * R_{thjr} + T_R \quad (3)$$

Semiconductor Thermal Test Equipment

The procedure used determines the test equipment needed for measurement. Below you will find the equipment used for both a manual and an automated approach to thermal measurement.

Manual Technique:

Power supply	*(supplies power to the device under test)*
Thermocouple	*(measures T_R)*
Multimeter	*(measures current and voltage)*
Heat exchanger	*(needed to mount device to and remove heat)*
Chiller	*(needed to remove heat from device)*
Test fixture	*(provides power and sampling pulse train)*

Automated Systems Available:

Analysis Tech	*(Phase 6, 7, 8, and 9)*
Sage	*(Star 150)*
TESEC	*(DV240)*

The automated systems shown above each provide different levels of automation. Analysis Tech has the most complete automation and TESEC the least. One nice feature of the Analysis Tech system is that it will output the 3 resistor–capacitor values for the electrical equivalent circuit. These values are very useful for modeling the thermal effects in computer simulation software such as SPICE. The level of automation you need depends both on your thermal measurement goals and available budget.

The main advantages of an automated approach are;

- Ease of use
- Less operator dependence on measurement
- Consistency
- Accuracy
- System network capability for data transfer

Thermal Parameter Test Procedure

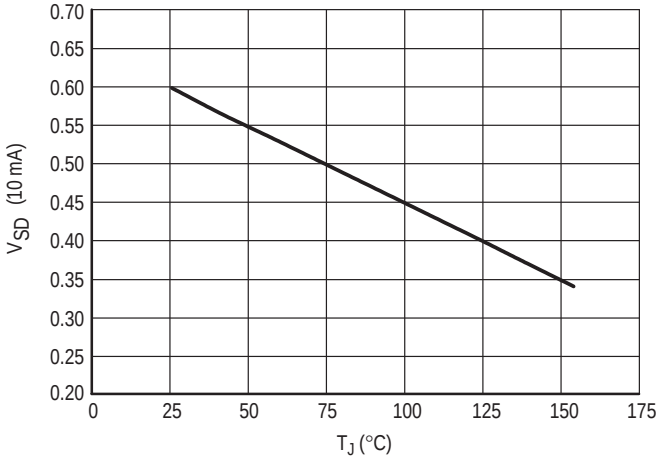
The basic procedure for measuring thermal parameters is as follows.

1. Calibrate the TSP (Temperature Sensitive Parameter).
2. Apply continuous power and TSP sampling pulses.
3. Measure T_J, T_R, and applied test power.
4. Calculate thermal resistance, $R_{thj(r)}$, and Maximum Power, P_D.

1. Calibrating the TSP, Temperature Sensitive Parameter

Since it is basically impossible to put a physical thermometer onto a device's junction to measure its temperature while under power, we must find another approach. Fortunately, we can use the device's forward junction voltage to tell us its temperature. The forward voltage drop of a diode's pn junction has a very linear relationship with temperature. We can use this relationship to tell us what the junction temperature is under any power condition.

To determine the actual voltage temperature relationship of a TSP for a given device, simply calibrate the TSP at a constant sense current over temperature as shown in Figure 2. The TSP sense current used should be small so as to not cause additional heating during calibration.



The forward voltage drop of a MOSFET body diode decreases linearly over temperature at rate of about 2 millivolts per degree Celsius when measured at a sense current of 10ma.

Figure 2. Typical Temperature Calibration Curve for a TMOS™ body diode.

Other device electrical parameters have similar linear relationships to temperature as well. The following are several other temperature sensitive parameters used in the industry to determine a device's junction temperature.

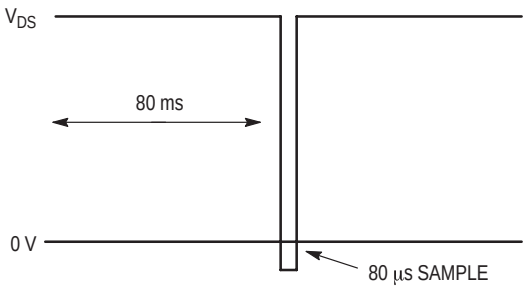
Common TSP:	Device Type:
V_{TH}, $V_{DS(on)}$, $R_{DS(on)}$	MOSFET
V_{TH}, $V_{CE(s)}$	IGBT
V_{BE}, $V_{CE(s)}$	Bipolar
V_F	Diode

Make sure to develop the actual electrical to thermal correlation of the TSP and check it for linearity prior to its use. The linearity of this parameter is critical for accurate thermal measurement.

2. Applying Continuous Power and TSP Sampling Pulses

With a properly chosen and calibrated TSP, we can now provide test signals to the device and make thermal measurements.

We begin by applying a continuous power of known current and voltage to the device. A continuous train of sampling pulses monitors the TSP, and thus the junction temperature. The TSP sampling pulse must provide a sense current equal to that used during calibration. While monitoring the TSP, adjust the applied power so as to insure a sufficient rise in T_J. Adjusting the applied power to achieve a T_J rise of about 100° above the reference temperature will generate enough temperature delta to insure good measurement resolution.



A continuous pulse train consisting of an 80 ms power pulse followed by an 80 μs diode sample is used to apply both power to the device as well as a sample pulse for TSP measurement.

Figure 3. Example of a power and sample pulse train during R_{thjc} measurement of a TMOS device.

The TSP sample time must be very short so as to not allow for any appreciable cooling of the junction prior to re–applying power. The power and sample pulse train shown in Figure 3 has a duty cycle of 99.9% which for all practical purposes is considered continuous power.

Obviously, with this much power being applied to the device under test, the device's case will get very hot. To keep the device cool while under test, we need to mount it to a heat sink of some sort. A heat exchanger with chilled water flowing through it provides a good heat sink. In this way, we can keep the device's case temperature down (i.e., near 25°C) and maintain good measurement resolution (i.e., large temperature delta between the junction and reference location).

3. Measuring T_J, T_R, and Applied Power

After T_J has stabilized, we must record its value along with the reference temperature, T_R, and applied power. To calculate the devices maximum power rating, P_D, and thermal resistance, R_{thjr}, we need to have these measurements.

The devices junction temperature, T_J, is taken from the TSP electrical measurement. With the correlation between the TSP electrical measurement and temperature already established, determining T_J is pretty much straight forward.

A thermocouple placed at the reference location measures the reference temperature, T_R. Most power semiconductor manufacture's use the devices' case, however, the lead, ambient, or all three can be used as reference locations.

Key elements to insure accurate reference temperature measurement are:

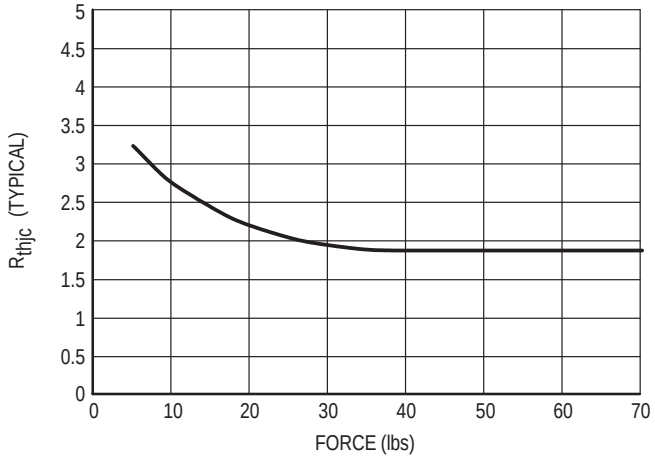
- Good thermocouple to reference contact
- Consistent thermocouple placement location

The reference thermocouple needs to make a good thermal contact to its reference location. This applies to reference locations other than ambient. Without a good thermal contact, measurement error will occur. To improve this contact, use both thermal grease and device clamping pressure as suggested.

Use thermal grease to insure good thermal conductivity and to eliminate air gaps. Applying thermal grease between the device and the heat sink used to keep the case temperature near 25°C will help in two ways. First, it will help keep the case temperature down during measurement by improving the thermal contact to the heat sink. Second, it will also improve the thermocouple to case contact as well. As stated earlier, the case is usually used as the reference location for thermal measurements. Thermal grease helps to maintain good thermal contact and insure measurement accuracy.

Applying about 40 lb of force (85 to 90 PSI) between the thermocouple and the reference location (i.e., device's case) also improves the thermal contact as shown in Figure 4. The application of pressure to the device seems to smooth out thermal grease thickness variations and eliminate air gaps at the contact interface.

Taking these precautions into consideration will help insure a good thermal contact to the reference location surface (i.e., device case).



The value of measured thermal resistance drops and becomes consistent at about 40 lb. of clamp force (85–90 PSI) insuring good thermal contact between the thermal couple and the devices case. [1]

Figure 4. R_{thjc} vs. Clamp Force for a ON Semiconductor MJF10012 TO–218 Fullpak device with uncontrolled thermal grease thickness.

The reference thermocouple needs to be placed at the same location for every device. Any change in the placement of this thermocouple will result in error or at the very least inconsistencies between measurements. A different thermal resistance exists between the junction and the location of each thermocouple placement. Usually for the best readings, the reference thermocouple should be placed at the hottest location on the package (i.e. for TO–220 devices, at the center of the die on the back side of the devices metal case). In any event, to be accurate and consistent, always place the reference thermocouple in the same location for each device measured.

4. Calculating Thermal Resistance, $R_{thj(r)}$, and Maximum Power, P_D

We can use equations (1) and (2) presented earlier, along with our measurements, to calculate the devices thermal resistance and maximum power capability.

Assuming we measured the following; T_J = 100°C, applied test power = 50 W, T_C = 25°C, and maximum device temperature rating = 150°C, we use equation (1) to calculate R_{thjc}.

$$R_{thjc} = (100 – 25)/50$$
$$= 1.5°C/W \text{ (measured value)}$$

Most manufacturer's will guardband the measured R_{thjr} reading to establish their device limits. This helps take into consideration all of the variables involved which cause inconsistencies in readings. A guardband of 25% for thermal measurements is considered good practice.

Multiplying the measured thermal resistance from above by 1.25 to guardband it by 25%, we get the following specified R_{thjc}.

$$R_{thjc} = 1.5 * 1.25$$
$$= 1.9°C/W \text{ (manufacturer's guaranteed limit)}$$

As shown in the Figure 5, the thermal resistance from junction to case is largely dependent on the die size of the device. This implies that silicon has a much larger thermal resistance, or opposition to heat flow, than that of the copper header to which it is bonded to.

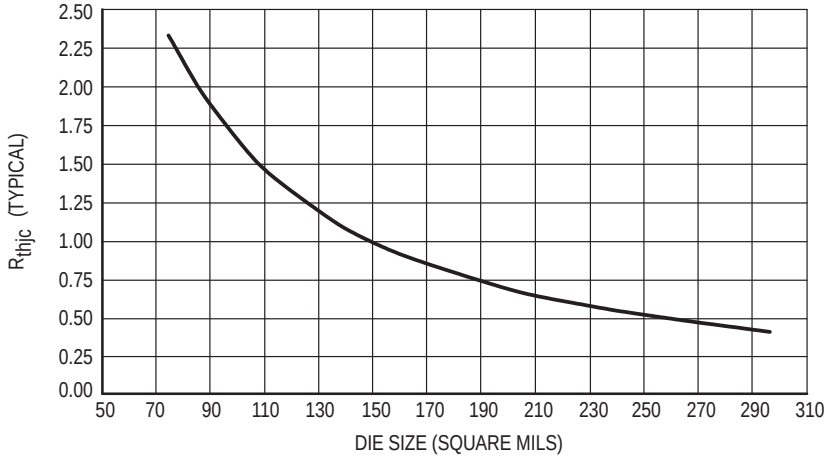


Figure 5. R_{thjc} vs. die size for TMOS® devices in TO–220, D^2PAK, DPAK & TO–247 Packages.

To determine a devices power handling capability, P_D, we use the specified R_{thjc} taken from above along with equation (2).

$$P_D = (150 – 25)/1.9$$
$$= 66 \text{ W (manufacturer's guaranteed limit)}$$

Using Thermal Parameters to Solve Often Asked Thermal Questions

One can use measured or specified thermal parameters to solve many common questions asked about power semiconductor devices. The two examples shown below use thermal parameters to solve frequently asked questions.

Example #1

Calculate the device's junction temperature: Using equation (3) with a known R_{thjc} of 1.25°C/W, case temperature of 85°C, and applied power of 35 W.

$$T_J = 35 * 1.25 + 85$$
$$= 128.8°C$$

Example #2

Calculate the power handling capability : Using equation (2) with a known R_{thjc} of 1.0°C/W, a starting case temperature of 75°C and a maximum rated T_J of 150°C.

$$P_D = (150 – 75)/1.0$$
$$= 75 \text{ W}$$

SUMMARY

This paper presents a description of basic semiconductor thermal measurement as well as the use of thermal data in real world examples. Included are terms, definitions, equations and test equipment required. This provides the reader with information useful in answering many common questions regarding the basic thermal capabilities of power semiconductor devices.

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[2] Gottlieb, Irving M., 1992, *Regulated Power Supplies*, 4th Edition, Blue Ridge Summit, Pennsylvania, TAB BOOKS: (92–105).

[3] Pshaenich, Al, "Basic Thermal Management of Power Semiconductors", ON Semiconductor Application Note *AN1083*.

[4] Roehr, Bill and Bryce Shiner, "Transient Thermal Resistance — General Data and its Use", AN569 in ON Semiconductor *Power Applications Manual*, 1990: (23–38), ON Semiconductor Literature Distribution Center, Ph. # 1 (800) 344–3860.

Thermal Characterization of the SO-8 Package for Power Semiconductor Applications

Kent Kime, Mike Lissy, Dave Shumate and Larry Walker
ON Semiconductor

ABSTRACT — A very up–and–coming package for power semiconductor applications is the SO–8 (also known in the IC world as the SOIC8) package. The purpose of this work is to present the thermal characterization (with emphasis on R_{thja}), both measured and modeled, of this package configured with a power transistor. The paper presents in detail results of characterizing three different package configurations: a) dual die, b) single large die, and c) single small die. The dual die and single large die configurations were used to establish the finite element model accuracy. The model was then used to predict the thermal performance in the untested single small die configuration. The model predictions matched the measured results thus validating the modeling effort. Factors such as solder voiding, die attach technique, junction depth, convective heat transfer coefficient and die thickness that could affect the modeling results were examined and their criticality assessed. As a verification to the modeling and measurements, infrared images were also made of the devices while under test.

INTRODUCTION

Actual measured thermal characterizations of semiconductor devices and packages can be very time consuming. If it is desired to evaluate multiple silicon and package configurations, the experimentation can take weeks. This is not acceptable in today's 10x, "first–to–market" product environment. One answer to this dilemma is thermal modeling. The goal here was to establish a verified model from which the major geometric, material and process variables affecting thermal performance can be determined.

Historically, the focus in power devices was the case–mounted part where the thermal model considered a series of resistances from junction (heat source) through the die, from die to the case and from the case to ambient. Traditional methods of viewing thermal resistance need to be expanded or at least viewed with greater understanding for surface mount packages. DPak and other case–mounted packages have been thermally characterized using R_{thjc} since a large portion of the case is attached to the board. For lead–mounted packages, SO–8, SOT–223, et al., however, the primary heat transfer is not through a board attached case but through the leads, and convection from the package surface becomes a significant factor. This can be seen in the simple parallel resistor analogy for heat dissipation shown in Figure 1, where R1 is the convection from the package surface and R2 is the conduction through the mounting surface. R1 is much greater than R2 for case–mounted packages. R1 is roughly the same order of magnitude as R2 for lead–mounted packages. Because of this, even small changes in the configuration of lead–mounted packages can drastically influence their thermal performance. Modeling makes determining this influence a manageable task.

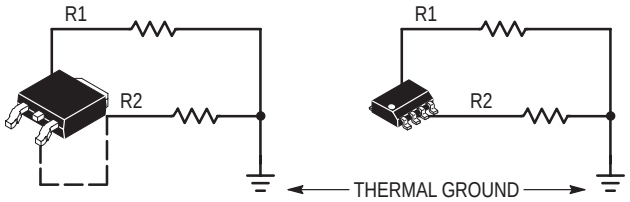

Figure 1. Parallel Resistor Analogy for Case–Mounted and Lead–Mounted Configurations

Definition of terms

DOE = Design of Experiments
DUT = Device–Under–Test
FEA = Finite–Element Analysis
FEM = Finite–Element Model
HTC = Heat Transfer Coefficient
PCB = Printed Circuit Board
P_D = Power Dissipation
R_{thja} = Thermal resistance, junction–to–ambient
R_{thjc} = Thermal resistance, junction–to–case
T_J = Junction Temperature
T_R = Reference Temperature
T_A = Ambient Temperature
TSEP = Temperature Sensitive Electrical Parameter

Device Thermal Measurements

In this section, thermal measurement techniques and the results of three experiments are discussed. Thermal characterization techniques are well established and have been standardized under such organizations as JEDEC and SEMI [1, 2]. Hence, there exists a certain level of confidence in the measured results. However, due to the nature of these measurements, there are always questions about accuracy; large percentage variations are not uncommon. The effort described in this paper establishes two key points: 1) accurate thermal modeling of power semiconductors can be accomplished with minimal experimental validation and 2) effective modeling can be used to illuminate the existence and sources of experimental error prevalent in this type of evaluation.

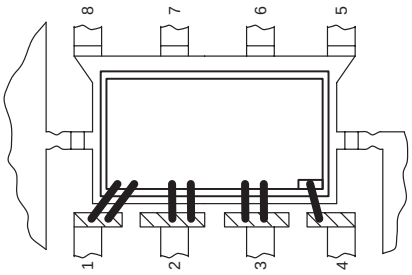

Figure 2. Device 1 – ON Semiconductor's MMSF5N03HD SO–8 package, 98 x 120 mil die, 1 die per package

In order to provide data for thermal finite–element model correlation efforts, two power semiconductor devices, shown in Figures 2 and 3, were characterized by the characterization laboratory.

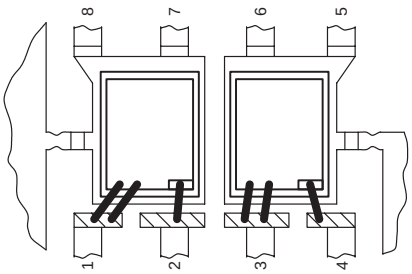

Figure 3. Device 2 – ON Semiconductor's MMDF3N03HD SO–8 package, 57 x 99 mil die, 2 die per package

Once the modeling technique was established with these two platforms, a double–blind experiment was conducted on a similar device with a slightly different configuration to demonstrate the modeling viability. The device used for this phase is shown in Figure 4.

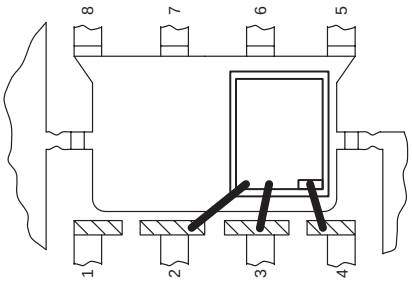

Figure 4. Device 3 – ON Semiconductor's MMSF2P02E SO–8 package, 57 x 99 mil die, 1 die per package

Since the modeling effort was launched from laboratory measured data, a verification of the laboratory results was warranted. Validation of the thermal characterization was achieved by utilizing thermal imaging techniques performed in an independent laboratory. What is fortunate about this method is that a correct temperature correlation can be established for the laboratory measurements and simultaneously thermal topographical mapping of the test coupon is provided, which can also be directly compared to the finite–element model's thermal profiles.

A. Thermal Characterization Techniques

Non–invasive, thermal resistance measurements are well established and quite mature. The general approach to thermal characterization of a semiconductor device is straightforward; many papers have been written on this topic [3]. First, the basic equation for thermal resistance used in the semiconductor industry is

$$R_{thjr} = \frac{T_J - T_R}{P_D} \quad (1)$$

Generally, T_J is measured utilizing an electrical characteristic of the device that is repeatable and an accurate function of temperature. This is usually referred to as the temperature sensitive electrical parameter (TSEP). The parameters most often used for MOSFETs are either $V_{GS(th)}$, $R_{DS(on)}$ or V_{SD} (the body diode forward voltage drop). The values of the parameter are established over the temperatures of interest, thus calibrating the TSEP "thermometer". During thermal characterization the TSEP is sampled to determine T_J. T_R is ordinarily measured with a thermocouple at the point of interest. P_D is simply the power dissipated by the device.

There are many sources for error in these thermal measurements. Also, there are many misunderstandings about the thermal resistance values. Most TSEPs for a given device have small, hard–to–measure changes over temperature. For example, V_{SD} may only change 2 mV per degree Celsius; therefore, sub–millivolt accuracy is needed to measure T_J. T_R accuracy depends on the thermocouple, its mounting techniques and its time response. To minimize heat "wicking" from the DUT small gauge conductors and four–wire measurement techniques are employed for P_D measurements. P_D can also be quite low (< 500 mW) for small surface mount devices which makes it difficult to measure accurately.

A key factor in understanding thermal resistance measurements is that if the application configuration is different from that of the measured device, the thermal results will be different. Thermal data on manufacturers' data sheets is designed for comparison with other manufacturers' devices and to give the user a place to begin their thermal management solution.

Test devices were mounted on 2 x 2 x 0.06 in. FR4/G10 printed circuit boards. The printed circuit pattern is a 1 x 1 in., 2 oz. copper pad with 10 mil separations for the leads. Figure 5 shows the test coupon layout. Due to some tester limitations, test devices were mounted to the PCB with the gate and source leads shorted together, essentially making the device into a rectifier. Since the body diode was the chosen TSEP, this change was thermally insignificant. Once mounted on the PCB and its support structure, the devices were placed for measurement in the center of a standard still–air chamber. The still–air chamber is a 1 ft. x 1 ft. x 1 ft. sealed chamber that prevents external sources of air movement around the DUT from affecting the measurements. Only natural convection is allowed. The test setup is then interfaced to the Analysis Tech™ Semiconductor Thermal Analyzer.

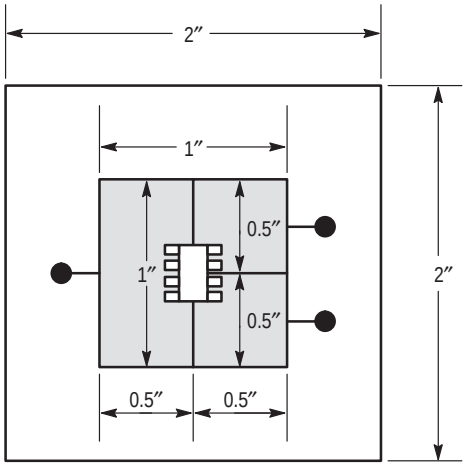

Figure 5. Thermal Test Coupon Layout

Almost all thermal analyzer equipment operates on the same principle. The DUT is powered by the tester for ≈99.9% of the cycle and the TSEP is measured for the other 0.1%. For steady–state thermal resistance, power is applied until T_J statistically stabilizes. T_R and P_D are measured simultaneously with T_J and, thus, thermal resistance is measured. For transient or pulsed power conditions, the pulse is applied and the TSEP is measured before and after it, indicating the ΔT_J during the pulse. For measuring thermal resistance as a function of time, the two methods most commonly used are referred to as cooling–curve and heating–curve techniques.

Briefly, in the cooling–curve scenario, the device is heated by applying P_D until T_J is at the desired value. After stabilization, power is removed from the device, and T_J and T_R are measured at precise time intervals during cool down. Using Equation 1, and the values measured, a thermal resistance versus time relationship is obtained.

For the heating–curve method, successive power pulses of programmed widths which produce the same ΔT_J are applied. The device is allowed to cool between pulses. These pulses are continued until steady–state T_J is reached. ΔT_R and P_D are measured simultaneously with ΔT_J; hence, the thermal resistance versus time characterization is produced. Generally, the heating–curve method is considered the more accurate technique due to the higher resolution created by the consistent ΔT_J, and because this testing technique operates the device in the manner it's most likely to be used.

B. Thermal Test Results

As mentioned before, three devices were characterized in the laboratory: two devices before FEA and one after. Both transient and steady–state thermal resistance values were obtained. The data is shown in Table 1 and Figures 6 through 8.

Figures 6 through 8 show the transient response curves generated for the devices' data sheets. Note the RC thermal networks that can be used in circuit simulator programs to determine T_J under any power input conditions. These thermal resistance versus time curves were generated using the heating–curve method. The curves shown are normalized at 10 seconds.

Table 1. Thermal Characterization Data for Three Devices mounted on 1 in. sq. Cu area PCB.

Device	Measured Steady–State R_{thja}	FEM Predicted Steady–State R_{thja}
MMSF5N03HD	70.3°C/W	70.1°C/W
MMDF3N03HD	87.0°C/W	84.5°C/W
MMSF2P02E	74.6°C/W	72.2°C/W

C. Device Infrared Thermal Imaging

As mentioned before, to help "triangulate" on the correct results for this characterization, thermal imaging was employed. The point here is to provide an independent "sanity check" for both the modeling and the laboratory measurements.

The thermal imaging procedure is fairly straightforward. First, as with standard thermal characterizations, power must be applied which raises the junction temperature to a known value. Again, this requires device TSEP calibration. Fortunately, in the case of a rectifier, the only parameter needed by the imaging laboratory is the current required (to the exact mA) to produce the desired T_J. Only steady–state correlation was obtainable with the thermal imaging equipment available at the Mechanical Engineering Laboratory.

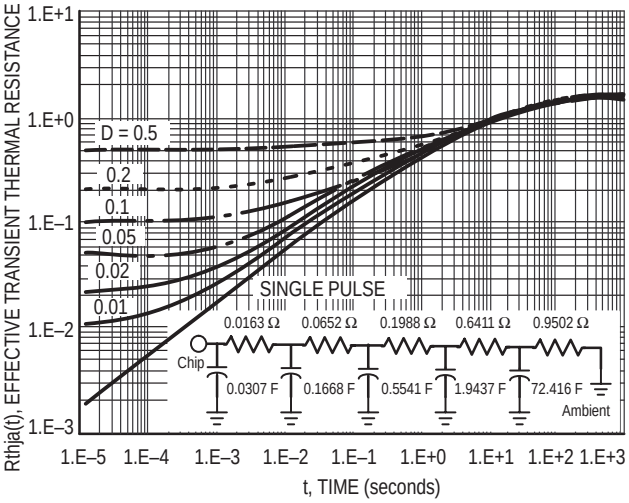

Figure 6. Transient Thermal response for MMSF5N03HD mounted on 1 in. sq. Cu area PCB.

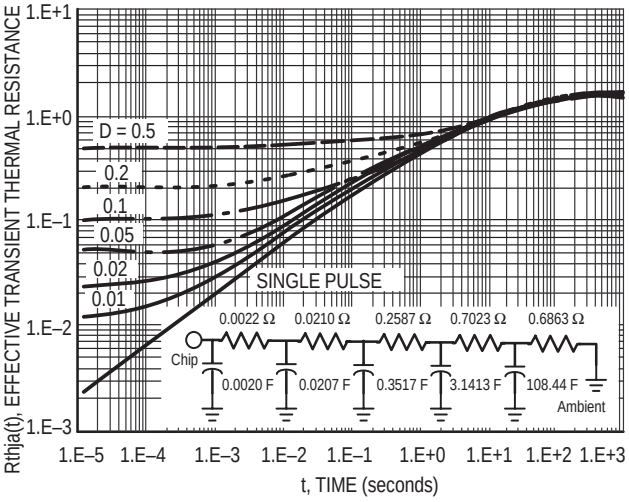

Figure 7. Transient Thermal response for MMSF2P02E mounted on 1 in. sq. Cu area PCB.

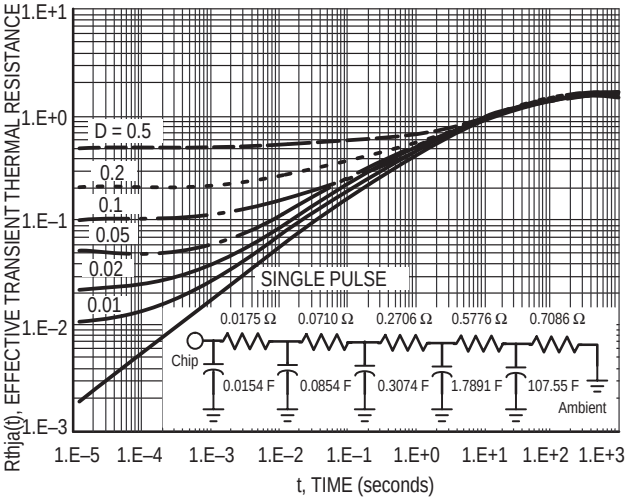

Figure 8. Transient Thermal response for MMDF3N03HD mounted on 1 in. sq. Cu area PCB.

Once a sample is prepared for emmissivity differences and mounted in the IR camera setup, the current is applied and the device temperature is allowed to stabilize. Thermal image photographs are then taken in which distinct temperature points are identified and the thermal profile is mapped. An IR image of the steady–state thermal profile of Device 1 is compared to FEA predictions in Figure 9 and Figure 10.

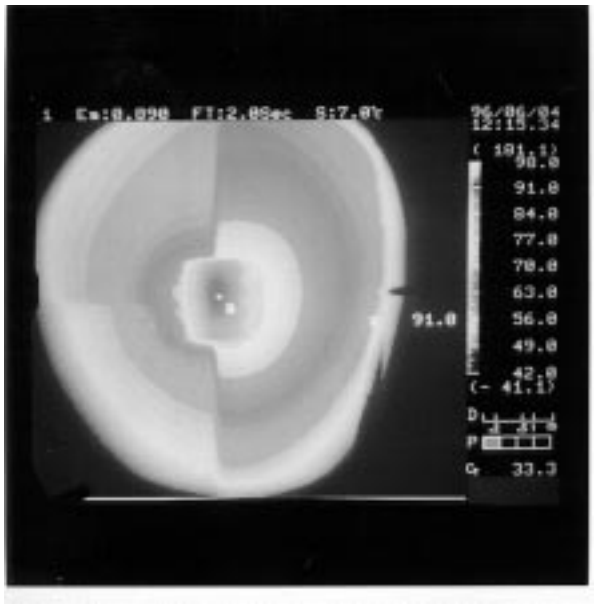

Figure 9. Thermal image of SO–8 package mounted on test coupon with power applied of 0.96 W.

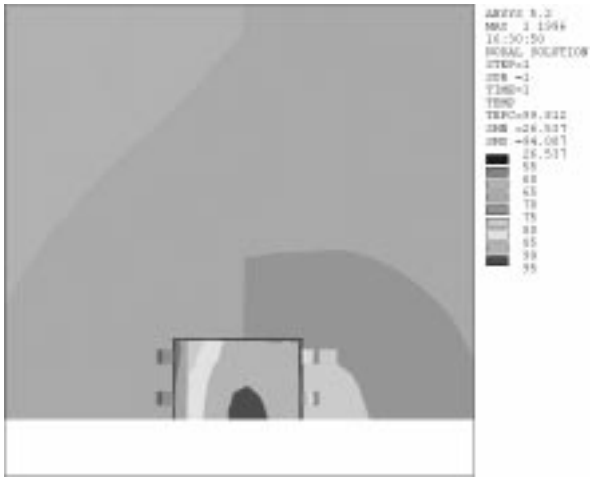

Figure 10. FEA steady–state temperature distribution on Device 1, half symmetry model at 0.96 W.

The maximum measured device surface temperature of 91°C compares well with the 93°C predicted by FEA. The measured and modeled steady–state thermal contours agree to within two to three degrees Celsius.

Finite Element Modeling

The finite–element analysis presented in this paper was performed in three stages. First, following DOE methodology, finite–element modeling was used to determine the relative importance of key variable factors related to the thermal performance of the SO–8 package. Next, the results of the DOE were used to provide direction to achieve correlation between the finite–element model predictions and thermal test results for Devices 1 and 2. Finally, the correlated SO–8 model was used to predict the thermal performance of Device 3.

A. Finite–Element Model Description

1. MODEL GEOMETRY

Three–dimensional solid models of the three different SO–8 configurations were made using IDEAS™ solid modeling software. The solid models were meshed with linear tetrahedral elements using the free–meshing capability in IDEAS. IDEAS was then used to translate the resulting meshes into ANSYS™ format. Boundary conditions were applied and the solutions run and post–processed using ANSYS.

2. BOUNDARY CONDITIONS

The boundary conditions consist of power applied to the die and heat transfer coefficients (HTCs) applied to external surfaces of the model. Power is applied to each model by specifying a heat flux over the active area of the die surface. The total power applied depends on the configuration: 2 watts to Device 1, 1.5 watts to Device 2, and 2.25 watts to Device 3.

Convective heat transfer to the air surrounding the part and test board is included by applying HTCs to the package top and both the upper and lower surfaces of the test coupon. The HTCs were calculated based on the approach used for free convection from horizontal flat plates outlined in [4, 5]. The interested reader will find the calculations for the HTCs used in this analysis in Appendix A. All surfaces without HTCs are assumed to be adiabatic.

B. Analytical DOE using FEA

1. EXPERIMENTAL DESIGN

The first phase of the analysis process involved using finite–element modeling to determine which parameters have the greatest influence on the thermal performance of the SO–8 package. The authors selected 6 parameters (listed in Table 2) believed to be of primary importance in determining package thermal performance. A designed experiment was generated in which each of these factors was varied from a selected minimum to maximum value. This was a factorial class 2^{6-2} with 16 runs plus 2 centerpoints (18 runs total) experiment. The range of variation of each factor is listed in Table 2. These ranges were selected by the authors to bracket what is commonly observed. The response variable was R_{thja} on the 1 inch copper pad. The general result of this first experiment was used to design a second experiment to investigate package design factors.

2. EXPERIMENTAL PROCEDURE

The experiment was conducted analytically using the ANSYS model of Device 1. In order to eliminate any effects that mesh density might have on the solutions, the same number of nodes and elements was used in each of the runs.

The procedure was to first use IDEAS to generate a mesh with the proper die and epoxy thicknesses. The mesh was transferred to ANSYS where the appropriate material properties were defined (silver epoxy and solder conductivities) and boundary conditions (power and HTCs) applied. A steady–state thermal solution was then performed and post–processed using ANSYS. The ANSYS results were then used to calculate a steady–state R_{thja} for each run using Equation 1 with T_R equal to T_A.

3. RESULTS OF DOE

The first experiment indicated that HTC was the only statistically significant variable. Device suppliers generally have no control over HTC and thus the impact of the other variables was desired. To see the significance of the other variables, a new factorial experiment (2^{5-1} with 16 runs) in which the HTC was kept constant was designed and conducted. Table 3 shows the inputs and responses. The analysis indicated that several input variables were significant such as die thickness, die attach thickness, solder board voiding and device junction depth. No interactions were statistically significant. An “F” value of 159 and a “p” value of less than 0.01% indicated the significance of this experiment. The analysis of the residuals indicates no non–linear dispersion and all of the assumptions of the analysis of variance were met (see Montgomery [6]).

Table 3 shows the relative strength of each of the pooled model variables. Die thickness has the strongest effect on the model. Tables 2 and 3 illustrate the predicted responses. The overall response variation from the experiment was only 3°C /Watt. Another main point of this analysis is that no interactions are significant.

Combining the results of the two designed experiments shows that HTC is the most significant variable. In order to get accurate modeling data, it is necessary to know the HTC value for the environmental conditions. The others variables do not play a significant role in the thermal model for steady–state R_{thja}.

C. FEA Correlation with Thermal Measurements

Prior to finite–element modeling of these parts, thermal testing of Devices 1 and 2 was performed. The data from this testing was used for correlation of the FE model. The results of the DOE show that for prediction of steady–state thermal performance the HTC values dominate other factors. The correlation efforts focused on adjusting the HTCs to match the test results. Other factors (die thickness, silver–epoxy thickness, etc.) were set to nominal values and not varied.

Table 2. Summary of DOE #1

DOE #1	Range	Effect	% Effect
Die thickness (mils)	8–15	0.16	1.8
Die attach thick (mils)	.25–.60	0.32	3.6
% silver in die attach	60 – 80	0.06	0.7
% Solder void	0 – 25	0.12	1.3
Junction depth	top – bot	0.11	1.2
HTC from nominal	±20 %	8.19	91.4

Table 3. Summary of DOE #2, with HTC held constant

DOE #2	Range	Effect	% Effect
Die thickness (mils)	8–15	0.34	35.4
Die attach thick (mils)	.25–.60	0.24	25.0
% silver in die attach	60 – 80	0.05	5.2
% Solder void	0 – 25	0.15	15.6
Junction depth	top – bot	0.18	18.8

Using the procedure outlined in Appendix A convective HTCs were calculated for Devices 1 and 2. These calculated values provided a good starting point, but required adjustment in order to obtain agreement between analysis and test. This is a normal practice in modeling to calibrate the work. The adjustment involved simply multiplying the calculated HTCs by a constant pre–factor. The value of the pre–factor was determined by running several steady–state thermal solutions for each configuration. Good correlation was achieved for a pre–factor of 1.2.

The results of the transient thermal analyses are compared to the test data Figures 11 and 12. Plots of R_{thja} vs. Time for both Devices 1 and 2 are presented. Examination of the plots shows very good correlation for time greater than 500 seconds. For time less than 500 seconds, the analysis consistently under predicts the R_{thja} of the parts. An explanation for this is that the overall package R_{thja} can be considered a combination of junction–to–case and case–to–ambient thermal resistances. The correlation technique used here has concentrated on the case–to–ambient heat transfer aspects of the package which, as the DOE showed, dominate the steady–state thermal behavior of these parts. For short times, before the package has experienced much heating, case–to–ambient convective heat transfer plays a smaller role and other parameters, such as the thermal conductivities and enthalpies of the materials used in the package, have a greater influence. A more complete assessment of the important factors in the short time portion of a thermal transient could be obtained by performing a DOE using transient (rather than steady–state) thermal analysis. Such an exercise would require a substantial amount of computation time and is an issue the authors hope to address in the future.

A final note concerning Figures 11 and 12, the analysis curves are based on R_{thja}'s determined using the die average, not maximum, temperature at each time point for T. The authors feel that using the die average temperature more closely matches what is actually measured using the heating–curve test technique described earlier in this paper.

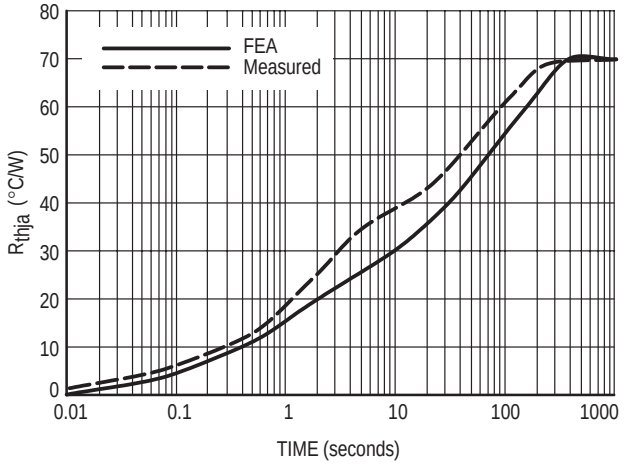

Figure 11. Measured and Modeled R_{thja} for Device 1

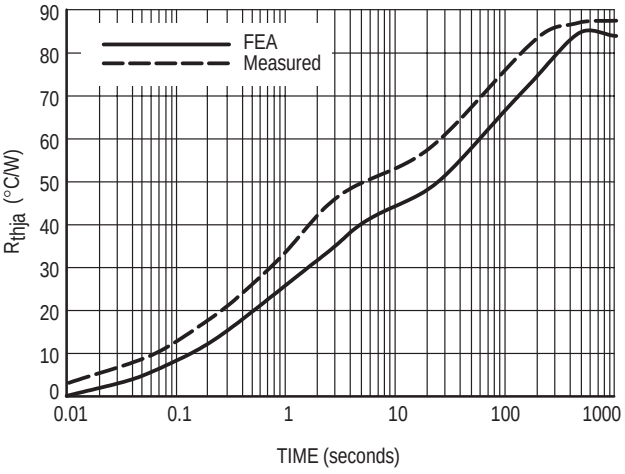

Figure 12. Measured and Modeled R_{thja} for Device 2

D. Device 3 Thermal Performance Prediction

The purpose of the analysis presented to this point has been to determine the proper boundary conditions for our thermal test configuration. The next step was to use that information to verify the capability of the model to predict the thermal performance of a previously untested device.

The results of the thermal FEA of Device 3 are shown in Figure 13. The data labeled "FEA" was generated using convective HTCs calculated with the procedure in Appendix A and a pre–factor of 1.2 as in the previous analyses. It is known from previous efforts that the "FEA" curve probably correlates only for times greater than 500 seconds. It was seen for Devices 1 and 2 that for times less than 500 seconds the analysis consistently under states the R_{thja}. The "Estimate" curve in Figure 13 was generated by assuming for Device 3 the same average percentage difference between measurement and test as observed in Devices 1 and 2.

After completing the above analysis and arriving at an estimate of the transient thermal performance of Device 3, this configuration was built and tested. The data from this testing is labeled “Measured” in Figure 13. The measured data matches the estimated very well across the entire transient, with a maximum deviation of approximately 10% in the 10 to 20 second range.

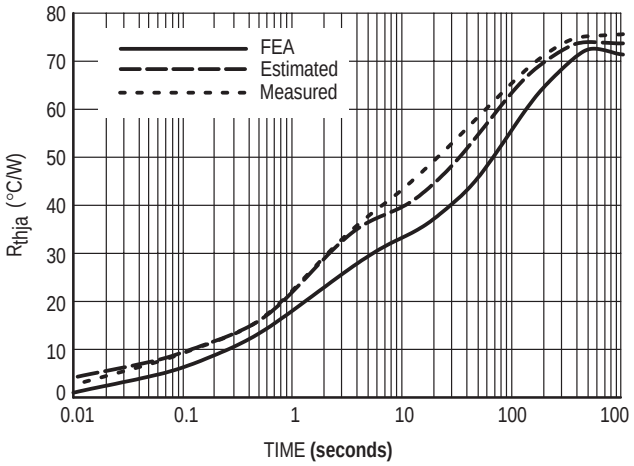

Figure 13. Predicted and Measured R_{thja} for Device 3

CONCLUSIONS

The original intent of this work was to match the modeled predictions with measured thermal data. This was accomplished with a two–phase DOE. During the process, several factors were discovered:

- In predicting steady–state R_{thja} for lead–mounted devices, HTC dominates. Package design and assembly parameters are insignificant.
- Test configuration has a large influence on the measured Rthja, which, for power devices, is quite a paradigm shift from the typical R_{thjc} measurements. In the modeling realm, it is critical to use the exact configuration or R_{thja} can be completely in error.
- Models of this type must be correlated and calibrated to measured values. Otherwise, significant prediction errors may occur.
- Infrared measurements are an excellent way to verify measured and modeled values of R_{thja}.
- Determining HTC for free convection is very complex and critical to model construction. The accuracy of the FEA thermal predictions depends on correct HTC values.

One practical result of this work is that it allowed ON Semiconductor to re–specify the power and drain current capability of ON Semiconductor’s MiniMOS™ (SO–8 MOSFET) portfolio to match or exceed competitors’ claims. This directly resulted in increased sales and allows ON Semiconductor to be considered for design into sockets that were previously unavailable because of inequitable specifications.

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[6] Montgomery, Douglas C., DESIGN AND ANALYSIS OF EXPERIMENTS, John Wiley & Sons 1991.

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ACKNOWLEDGMENTS

Special THANKS to Bob Buhrman, Ed Clemente, and Tanya Fowler for their support.

APPENDIX A:

Calculation of HTC for Natural Convection to Air

A. Introduction:

As shown in the body of this report, for the devices tested, accurate determination of HTCs is of primary importance to achieve good agreement between FEA and measurements. This is because the primary heat transfer mechanism to the outside environment is convection.

B. Procedure for HTC Calculation:

The authors used an approach outlined by Zahn, Stout, and Billings [4]. In their paper, a procedure for determining HTCs for natural convection from parts mounted on horizontal test boards is defined. The work of Zahn et al. relies heavily on the results of a previous study by Chambers and Lee [5]. The approach here is to use their method to calculate

separate HTCs for the top of the SO–8 package, the surface of the copper cladding, the remaining top surface of the test board, and the entire bottom surface of the test board. This is, perhaps, beyond how Zahn, et al. intended their method be used. The intent here is not to claim that the use of this method is scientifically rigorous, but instead to use it in the hopes that it will give a good starting point for achieving correlation with data measured in the lab.

Equations 10 and 11 of Zahn, et al. states for horizontal flat plates,

$$\overline{h}_{pup} = 0.653k^{0.857}\left(\frac{g\beta}{v^2}\Pr\right)^{0.143}\left(\frac{q^{0.143}}{P^{0.428}}\right) = z_{up}\left(\frac{q^{0.143}}{P^{0.428}}\right) \quad \text{(A1)}$$

and,

$$\overline{h}_{pup} = 0.979k^{0.863}\left(\frac{g\beta}{v^2}\Pr\right)^{0.137}\left(\frac{q^{0.137}}{P^{0.452}}\right) = z_{dn}\left(\frac{q^{0.137}}{P^{0.452}}\right) \quad \text{(A2)}$$

Where $\overline{h}_{pup}$ and $\overline{h}_{pdn}$ are uniform heat transfer coefficients on upward and downward facing horizontal surfaces in units of W/(m$^{2\cdot}$°C). The other parameters are defined as follows:

k = conductivity of air

g = acceleration of gravity

β = volumetric thermal expansion coefficient of air

v = kinematic viscosity of air

Pr = Prandtl number for air

z = composite parameter

q = heat generation rate per unit area

P = characteristic length defined as plate area divided by perimeter

The maximum steady–state junction temperature for the devices considered here is 150°C, so we used properties for air at 150°C to calculate z_{up} and z_{dn} for our case. The values used, and the resulting z_{up} and z_{dn} are as follows:

k = 0.03536 W/m·°C

g = 9.81 m/sec^2

β = 1/423K = 0.002364 K^{-1}

v = 2.88e^{-5} m^2/sec

Pr = 0.686

Resulting in:

z_{up} = 0.41 and z_{dn} = 0.54

Thus Equations 1 and 2 above are reduced to:

$$\overline{h}_{pup} = 0.41\left(\frac{q^{0.143}}{P^{0.428}}\right) \quad \text{(A3)}$$

and,

$$\overline{h}_{pdn} = 0.54\left(\frac{q^{0.137}}{P^{0.452}}\right) \quad \text{(A4)}$$

For the ANSYS solutions, Equation A3 was used to calculate HTCs for the upper surface of the SO–8 package, the surface of the copper cladding, and the upper surface of the test board. Equation A4 was used to calculate a uniform HTC for the lower surface of the test board. Determination of the values of P for each of the four HTCs calculated is straightforward – divide the region area (m^2) by the perimeter (m) to determine a value for P in meters. Selecting the values of q to use for each surface is not so simple. The authors chose a scheme in which the total power applied to the package is divided among the four surfaces as follows: 10% through the package top, 40% from the surface of the copper cladding, 10% from the remainder of the test board upper surface, and 40% from the bottom of the test board. This seemed reasonable as the area of the package top surface is only 2.5% of the area of the copper cladding thus more of the total power will go through the cladding than the package top, even though the package top reaches a higher temperature.

The HTCs determined for the three SO–8 configurations are summarized in Table A1. Note that the only reason for the differences in HTCs between configurations is that the total power is different. Also note that the best correlation between model and test was achieved by increasing the HTC values listed in Table A1 by a factor of 1.2. Each configuration requires measurement calibration to determine an accurate HTC correction factor.

Surface	Width (m)	Length (m)	Area (m^2)	Perimeter (m)	P (m)	q (% of Total Power)
Package Top	0.00338	0.00475	1.61E–05	0.01626	9.87E–04	10
Copper Cladding	0.0254	0.0254	6.45E–04	0.1016	6.35E–03	40
FR4 Board Top	0.0508	0.0508	1.94E–03	0.2032	9.53E–03	10
FR4 Board Bottom	0.0508	0.0508	2.58E–03	0.2032	1.27E–02	40

Table A1: Calculated HTC Values for Devices 1, 2 and 3

Calculated HTC Values					
Device	Total Power (Watts)	Package Top (W/m^2 C)	Copper Clad (W/m^2 C)	FR4 Top (W/m^2 C)	FR4 Bottom (W/m^2 C)
1	2	30.534	9.898	5.833	8.527
2	1.5	29.304	9.499	5.598	8.197
3	2.25	31.053	10.066	5.932	8.666

New Models and Techniques for Analyzing the Power Transistor and its Thermal Environment

By Kim Gauen
Motorola Semiconductor Products Sector

INTRODUCTION

In many electronic systems, power transistors perform critical system functions. They also can account for a significant portion of the total system cost. Better performance can come at a higher price, but balancing this price/performance tradeoff has not been easy for designers. Thermal issues are involved, and the tools for analyzing the electrical/thermal environment have not been available. Recently, new tools have become available and techniques are now appearing for sophisticated analysis of the power transistor and its thermal environment.

This paper describes one set of tools and some techniques for thermal/electrical analysis. Because the power MOSFET is so popular, it is one of the first devices to be characterized for such evaluations and it is the focus of this paper.

Know Your Transistor's Operating Temperature

Probably the two most important parameters for keeping a power MOSFET within its safe operating area are its silicon temperature, often referred to as its "junction temperature (T_J)," and the voltages appearing across its terminals. Steady state current handling capability is certainly important, but it is usually bounded by the maximum rated junction temperature and not by effects such as wirebond limitations, metal migration of the source metal, or insufficient gate voltage.

There are several reasons why it is important to know a power MOSFET's junction temperature. First, junction temperature affects reliability. High temperature and the associated thermal cycling accelerate several failure mechanisms. Second, parameters that affect junction temperature also influence system cost. An overly conservative designer might use a power transistor that is unnecessarily large and expensive for the application. On the other hand, using a transistor that is undersized might result in the designer selecting a heat sink that is larger and more expensive than necessary. Third, knowing T_J will help the designer understand how the system will operate under various loading conditions and temperatures. MOSFET junction temperature affects its breakdown voltage, on–resistance, threshold voltage, switching speed, and transfer characteristics — all of which can cause changes in system level performance. For example, changing a MOSFET's switching speed is likely to affect the system's noise performance, and the MOSFET is certainly less efficient at higher temperatures due to a significant increase in $R_{DS(on)}$. With cost, system performance, and reliability at stake, the designer needs good tools for determining junction temperature and evaluating design tradeoffs.

Traditional Method of System Design

The traditional way to size a power transistor is to estimate the on–resistance requirements and the associated on–state losses and switching losses and then to estimate the size of the heat sink needed for the anticipated load currents and ambient temperature. The system is then assembled and tested and (sometimes) the transistor's case temperature is measured under "worst case" conditions. Heat sink or transistor size is then modified, and the system is retested and refined until the results are acceptable.

The limitations of this approach are well known. First, system complexity and lack of time often limit the engineer's ability to completely analyze the system prior to assembling hardware. Therefore, the first prototype is based on calculations, educated guesses, and intuition. Good analysis tools and techniques can produce a much better first pass implementation in hardware.

Second, determining "worst case" conditions might not be easy. For example, the highest junction temperature usually occurs at the maximum anticipated ambient temperature, but sometimes that is not the case. For some loads, currents are significantly higher at cold temperatures. If a large load such as a motor has a very long thermal time constant, the power transistor could see high currents for a long time relative to the thermal time constant of it and its heat sink. It would be helpful to have a method of quickly evaluating the effects of these and other changing conditions.

The third problem with the traditional approach is that it is cumbersome to evaluate system trade–offs with hardware. Heat sinks must be built and changed, the system must be tested under various conditions, loads must be built, ambient temperatures must be controlled, etc.

Other difficulties are related directly to analyzing the thermal system. The first problem is that junction temperature is not easy to measure. Using an infrared camera to view an unencapsulated die would be ideal, but few designers have this option.

More likely, a designer places a thermocouple on the heat sink next to the MOSFET or directly on the MOSFET's tab. But under transient conditions or at high power, these measurements are probably at least several degrees lower than the actual junction temperature.

The most accurate way to monitor the junction temperature of a plastic encapsulated MOSFET is to use one of its temperature sensitive parameters, or TSPs. The MOSFET's TSPs are its on–resistance, the forward voltage drop of its body diode, its threshold voltage, and its breakdown voltage. All four require that each test device be calibrated over temperature, which is time consuming. The first two TSPs are the ones most commonly used.

In circuits where the MOSFET is on continuously, using $R_{DS(on)}$ as the TSP works fairly well. A low voltage MOSFET, however, may give a signal that is too low for accurate measurement. Therefore, this method works best for high on–resistance (high voltage) devices. Monitoring the forward voltage drop of the body diode gives very good results, but it is difficult to build the circuitry that interrupts the normal drain to source load current and forces a small source to drain sense current in the body diode. The technique of using the body diode is discussed in detail in References [1] and [2].

Even if the system is characterized perfectly, there are remaining roadblocks to accurately predicting junction temperature. Power waveforms are often complex, making analysis very difficult. The graphical methods described in Reference [3] can help, but they are unwieldy with complex waveforms. Next, there is the issue of how to monitor junction temperature to verify simulation results. Finally, it is important to provide power inputs to the thermal network and thermal inputs to the electrical system. Until recently, the only way to provide thermal feedback was to do it iteratively with successive simulation runs, one for each new junction temperature estimate. That approach suffices for steady state conditions, but it is not accurate for transient analysis since it cannot track junction temperature variations throughout the simulation.

Requirements for Accurate Models

To accurately model the electrical/thermal system a designer needs:

1. an accurate model of the MOSFET that is temperature dependent
2. a model of the MOSFET that supports passing information between the electrical and thermal environments during the simulation (these models are "dynamically" temperature dependent)
3. an accurate model of the MOSFET's thermal environment
4. tools that support the above models for easy simulation and analysis

Each of the above requirements can now be met, and the pieces have been assembled into a very effective analysis tool.

The first requirement is an accurate and robust model of the power MOSFET that is also temperature dependent. This model should accurately predict the I–V characteristics for the forward range of operation, as well as leakage, reverse recovery and breakdown characteristics of the drain–source body diode. The electrical model must also describe the nonlinear gate drain (and gate source for negative V_{GS}) capacitances that are key to accurate transient simulations.

In the language of simulation a "robust" model is one that does not cause convergence problems, which are most commonly the result of discontinuities in the model. Many SPICE based subcircuit models have been introduced over the years in an attempt to describe the non linear power MOSFET capacitances; however, the macro modeling approach introduces discontinuities. Although such discontinuities may be acceptable in a purely electrical simulation environment, the complexity of the dynamic electro–thermal system requires models with superior convergence qualities.

So far, the model we have discussed is a "static" thermal model. This means that the designer can assign any reasonable temperature to the model prior to simulation. However, device temperature will remain constant throughout the simulation, regardless of power dissipation. Instead of this static model, we require a "dynamic" thermal model that allows the device temperature to change as electrical energy is converted to heat, as it does in a real device. To accomplish this, the temperature parameter, used inside the MOSFET model to adjust the electrical parameters for thermal effects, must now become an independent variable solved by the simulator. When temperature is an independent variable, the simulator must solve a set of simultaneous nonlinear differential equations for temperature and heat flow as well as for voltage and current for each node and each time step.

The third requirement, having accurate models of the thermal environment, is a bit tricky to meet because there is no standard methodology for obtaining such models. The system designer has difficulty obtaining thermal models of heat sinks and extracting thermal models of the MOSFET from the information provided on the MOSFET data sheets. Neither the power transistor user nor the semiconductor manufacturer has a very good handle on characterizing the thermal interface between the case and the heat sink. However, techniques are available to get such models. The best technique depends on the pulse width of interest.

Transient thermal response curves for power transistors have been around for a couple of decades. A curve like the one shown in Figure 1 is generated by observing the response of the transistor's junction temperature to a step function of power dissipation. One can develop a thermal R–C network from a transient thermal response curve.

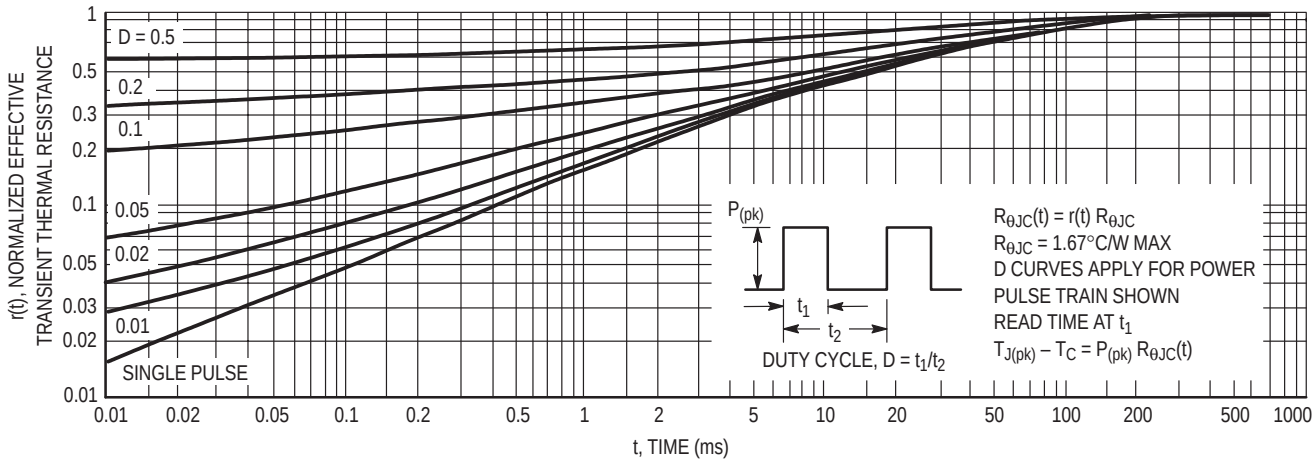

Figure 1. It is possible to generate thermal models from transient thermal response curves such as this one for a 4 A, 500 V MOSFET in a TO–220 package.

These curves are perfectly adequate for analysis — if the power transistor's case temperature is known and the power dissipation waveform is relatively simple. The accepted definition of "case temperature" is the temperature of the hottest part of the transistor's tab, which is the spot on the tab just behind the power transistor die, as shown in Figure 2. Unfortunately, monitoring this temperature is not easy and a tab or heat sink temperature is often measured instead. So, the situation that is easiest to analyze is one where the case temperature doesn't change, as would happen under brief transient conditions or when the tab is attached to a known and constant temperature — an "infinite heat sink."

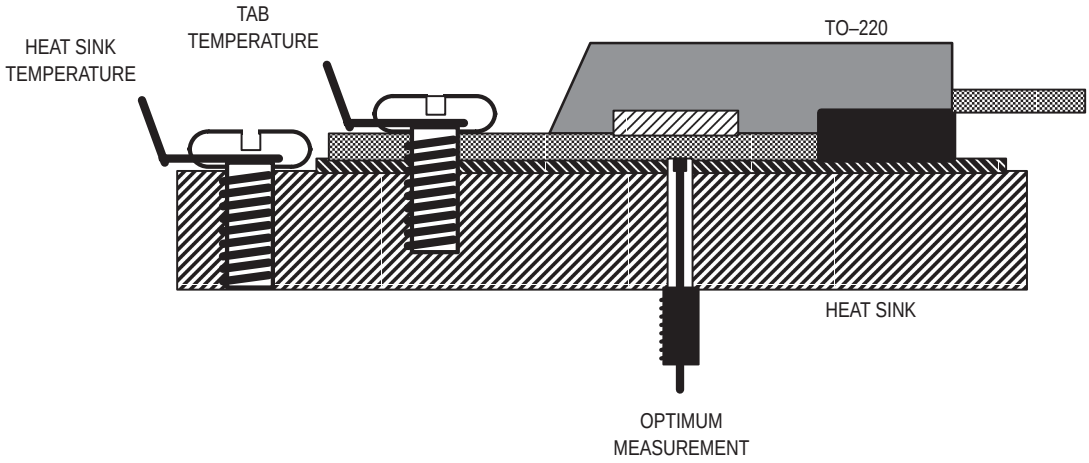

Figure 2. The standard way to measure the heat sink of a power transistor is to place a thermocouple through the heat sink and against the back of the transistor's tab, just opposite the center of the die.

Steady state conditions are also fairly easy to characterize and then model. One could characterize the system's thermal resistances (junction to tab, tab to heat sink, heat sink to ambient), put the steady state models into the simulator, and again the modeling should go smoothly. But for many cases, i.e., for power pulses more than a few milliseconds yet not DC, an approach that defines the entire thermal system is needed.

An effective method is to treat the power transistor and its heat sink as a unit and characterize the assembly just as one would characterize a power transistor — in effect, developing a transient thermal response curve for the entire thermal system. This method inherently addresses the thorny problem of trying to define the thermal interface if the power transistor and the heat sink are characterized separately. The interface is simply one part of the network, and the empirical tests automatically include its effects. The last circuit example in this paper shows how to use this technique.

The fourth and final requirement is for a simulator that can support thermal as well as electrical models, allowing the electrical system to affect the thermal and visa versa. In system simulators such as SPICE the system variables are constrained to voltage and current. In order to simulate non–electrical systems in these types of simulators, the non electrical system must be written in terms of equivalent electrical elements, or macro–models. Macro modeling techniques

of electro–thermal systems suffer from their inability to directly adjust the internal electrical model parameters for the non–electrical changes in the system. To circumvent this limitation, the user is forced to make gross adjustments to the external nodes of the circuit through controlled sources or other elements.

Simulators such as Analogy's SABER provide a modeling language which separates the simulation "engine" from the models. (Analogy's hardware description language is MASTTM.) This allows the user to develop models as a system of through and across variables that are not constrained to voltage and current. Thus, the relationship between electrical and thermal energy can be described directly in the model. The SABER simulator uses a dynamic thermal version of the MPV3 MOSFET model (MPV3X), which is the basis of the library of ON Semiconductor MOSFET models provided with the 4.0 release of SABER.

A Simple Example

A simple example illustrates the basic modeling concepts and some of the analysis possibilities. Assume that the desired load current conducted by a pair of MTP75N05HDs is 35 A and that the load current lasts for an indefinite time. Also assume that the heat sink is a 40 mm by 20 mm by 12 mm piece of aluminum with no fins. Such a heat sink has a large thermal capacity and low cost, but poor thermal resistance. So, the question might be, "In a 25°C environment, how hot do the power transistors get and how long does it take to reach steady state conditions?" Without good evaluation tools or actual hardware, it is difficult to tell if the transistors will slip into a thermal runaway condition.

The first step is to characterize the heat sink. A single MOSFET was mounted to the heat sink and was controlled to step its power dissipation from 0 to a constant and continuous 7.87 W. The MOSFET's tab was monitored until the system became stable. From the power dissipation and the difference between the tab and ambient temperatures, the thermal resistance is easily calculated. For this heat sink in a 30°C environment:

$$T_{tab} - T_{amb} = P_D * R_{th\_hs}$$

$$152°C - 30°C = 7.87 * R_{th\_hs}$$

Therefore, $R_{th\_hs} = 15.5°C/W$

Like all others, this heat sink consists of a network of distributed thermal resistances and capacitances. The construction and complexity of a heat sink determines how to select the lumped elements that model its thermal network. In cases like this, a single thermal resistance and capacitance model the heat sink well enough for purposes here.

With the assumption that a single R–C network is adequate, the task is now to determine the heat sink's thermal capacitance. Figure 3 shows how the transistor's tab temperature varies with time, and the data suggest a tau of about 420 seconds. That sets the thermal capacitance to 27 J/°C. Simulating with an Rth_hs of 15.5°C/W, a Cth of 27 J/°C and a power dissipation of 7.87 W yields a response that is within measurement error of the actual system response. This system is relatively easy to model since the power dissipation in the MOSFET is held constant by gate drive circuitry and the thermal network is quite simple.

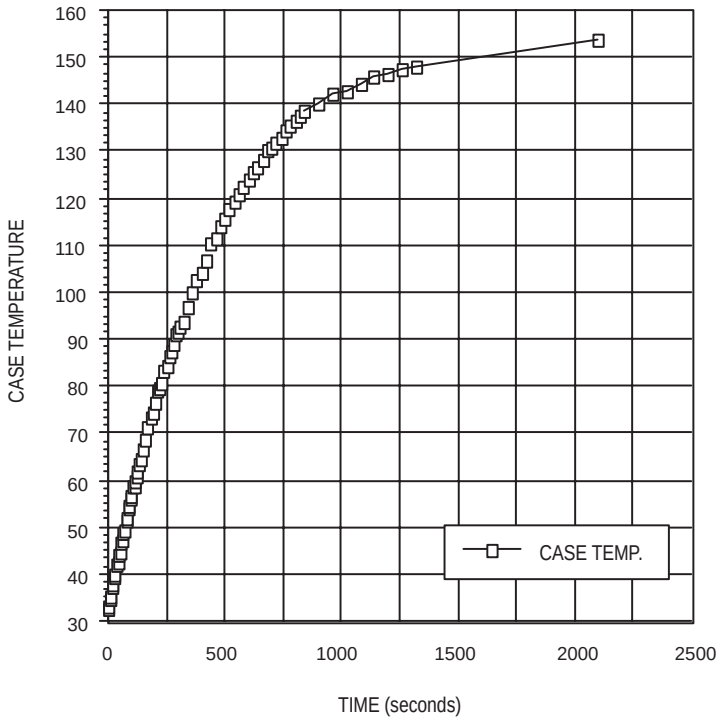

Figure 3. Thermal response of 40 x 20 x 12 mm Al heat sink

A more difficult test of the models and the simulation methodology is to revisit the conditions and requirements of the initial application. In this case, two MOSFETs were mounted to the same heat sink and they were forced to conduct 17.5 A continuously at an ambient and initial heatsink temperatures of 20.7°C. The added difficulty of this simulation is that the power dissipation of the MOSFET causes the heat sink and junction temperatures to increase, which increases on–resistance and further increases power dissipation. The change in $R_{DS(on)}$ cannot be ignored because it increases by about 70% for a 100°C rise in junction temperature. The first simulation was simpler because the power dissipation was held constant since the MOSFET was forced by gate drive circuitry to operate as a constant current source.

The results of the simulated $V_{DS(on)}$ and the actual tab temperature data are shown in Figure 4. Again, the empirical and simulated curves are the same within a couple of degrees and about 10 mV. For this example, the tab temperature is very close to the junction temperature since the MOSFET's power dissipation is less than 3.5 W. The results track nicely only because SABER's MOSFET model is dynamically temperature dependent. The model correctly predicted the final junction temperature and that the system would not go into thermal runaway. Additionally, the MOSFET's $V_{DS(on)}$ in simulation matched the empirical results even as junction temperature changed, further validating the model.

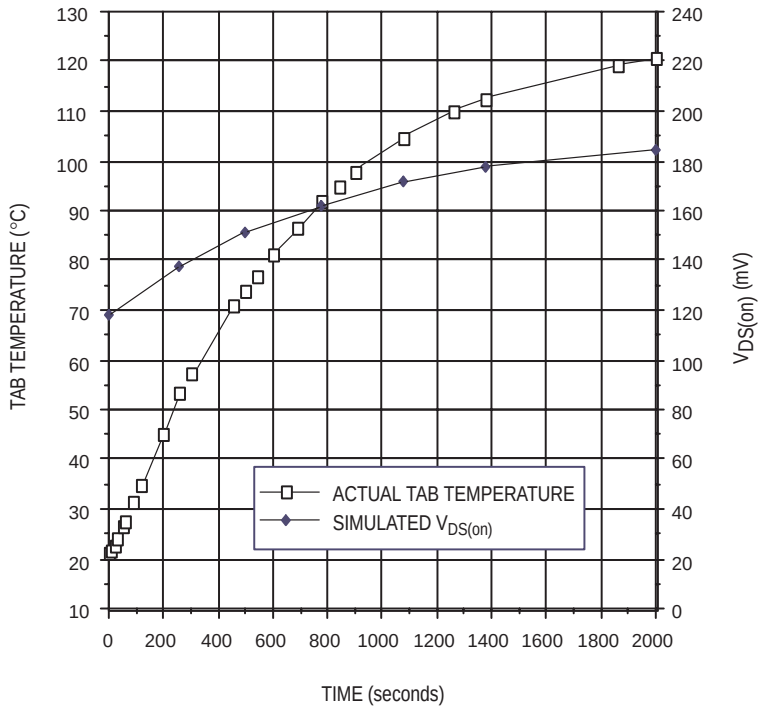

Figure 4. One of two MTP75N06HDs conducting a total continuous current of 35 A. Simulation results closely matched empirical results.

A More Complex Example

The above example validates the general concept for a relatively simple circuit. Adding pulse width modulation to the circuit further illustrates the technique's strengths, but it also uncovers some limitations. This final example also validates the technique of developing and using a transient thermal response curve for a MOSFET attached to a heat sink.

Like the other examples, the first step in this analysis is to determine the system's thermal model. But this time we are interested in the system's thermal response to very narrow power pulses that occur during switching transitions as well as the comparatively very long response of the heat sink. In fact, we are interested in responses to pulse widths varying about nine orders of magnitude; so it's likely that there are new measurement challenges.

Until recently, thermal response test equipment had maximum pulse width capability of at most a few seconds. The advent of surface mount power devices and the much longer thermal response time of the transistor/circuit board combination bought about the need for equipment that can apply a power pulse and measure the response for several minutes. One vendor of this new equipment is Analysis Tech, and their Phase 9 automatic transient thermal response tester was used in this study.

The Analysis Tech Phase 9 can be used to measure the thermal response of the system of interest here, i.e., a power

transistor mounted to moderate size heat sink. For this exercise an MTP15N06V (a 15 A, 60 V MOSFET) was mounted to a Wakefield 667–10ABPP heat sink. The Wakefield heat sink is finned and is 1″ tall, 1.35″ wide, and 0.5″ deep.

For MOSFET data sheet characterization, the transient thermal response is normally taken with the device mounted to an infinite (water cooled) heat sink. The infinite heat sink fixes the MOSFET's case temperature to a known value which serves as the reference temperature for the characterization. Instead of a water cooled heat sink, the Wakefield heat sink was used, and the reference temperature was the ambient temperature.

The thermal response of the MOSFET on the water cooled heat sink and the response on the Wakefield 667–10ABPP heat sink are shown in Figure 5. Note that at narrow pulse widths the two curves are very similar, as there is insufficient time to transfer enough power into the heat sink to raise its temperature. At about 0.3 seconds, the two curves begin to diverge as the temperature of the Wakefield heat sink begins to rise while the water cooled heat sink maintains a steady case temperature.

RC networks for both thermal circuits are included in Figure 5. They were automatically generated by the Analysis Tech Phase 9. Off the shelf programs such as Sauna™ can extract the thermal Rs and Cs from transient thermal response curves. The dashed lines, which are for the most part hidden by the empirical data points, indicate the response of the suggested RC equivalent networks.

Note that the final data point is taken around 600 s, before the MOSFET/Wakefield heat sink system is completely stable. At the time of the test this was thought to be the pulse width limitation of the tester. (The actual limitation is 10,000 seconds.) An alternate test using simple equipment that is only good for steady state produced a reading of 18.1°C/W for the total thermal resistance from junction to ambient. Therefore, in the final model of the MOSFET/ Wakefield heat sink, Rth_3 was changed from 11.44 to 15.66°C/W. (The Wakefield 667–10ABPP is specified to be 12.66°C/W in still air at 6 W.)

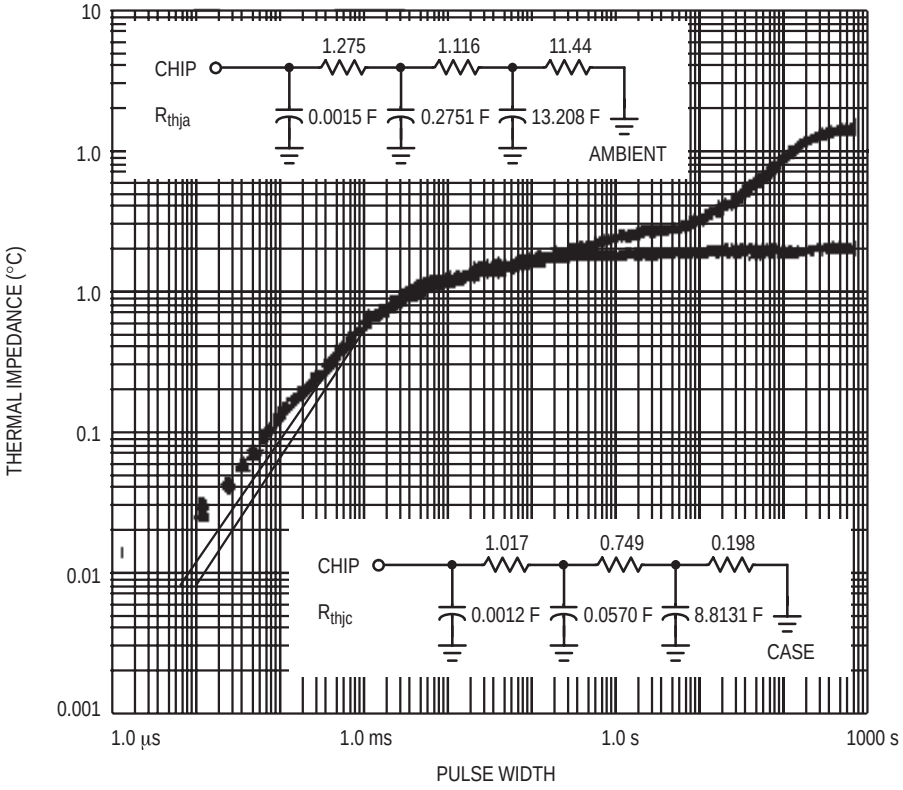

Figure 5. Thermal response of the MOSFET on a water cooled heatsink and on a Wakefield heatsink.

Figure 6 shows the entire thermal/electrical system. The MOSFET's gate was driven by a 10 V, 100 Hz, 50% duty cycle voltage source. A brute force attempt at simulating hundreds of seconds of operation unveils a limitation of the tools and this methodology. The simulation proceeds rapidly as long as the MOSFET is on or off, but during switching, the simulator slows down to accurately model the transitions. Even though the circuit is very simple and the switching frequency is low by most standards, it took several minutes on an HP 9000 Model 735 to simulate each second of operation. To get useful data without excessive simulation times, the simulation was conducted in two runs, one to ob-

tain the circuit's response during the first fourteen seconds and the other to determine its steady state response.

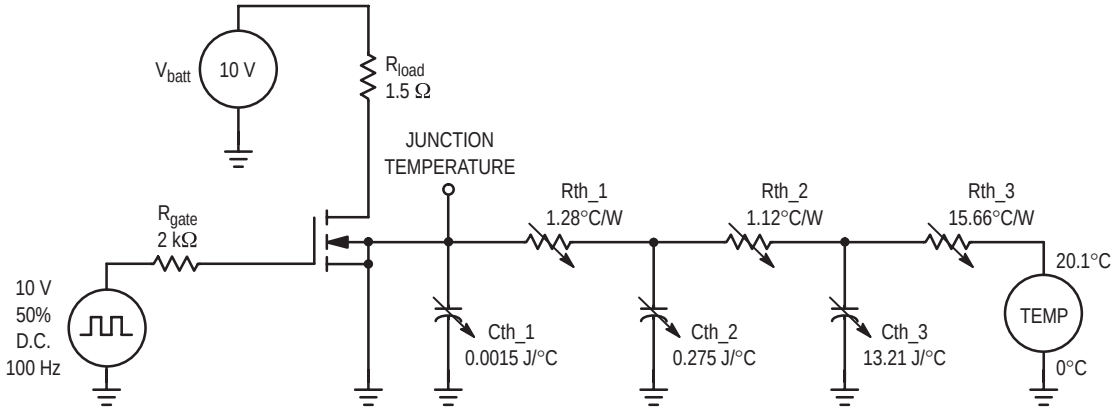

Figure 6. Schematic of electrical/thermal system. The values of the discrete thermal Rs and Cs shown are chosen to give a response most similar to that of the system's distributed elements.

Figure 7 shows the junction temperature variation during the first 1.1 s of operation. Two features are clear: the junction temperature swings about five degrees each period and the average temperature within a cycle begins to increase more slowly at around 300 ms as the heat sink's large thermal capacitance comes into play. The junction temperature during the first 14 seconds of simulation is shown in Figure 8. The junction temperature swing within a cycle, the rise in the average temperature during the first second, and the gradual rise thereafter are controlled by the three thermal capacitances.

Figure 9 shows the temperature appearing at Cth_2 and Cth_3. This graph clearly illustrates the initial charging of the heat sink's large thermal capacity. It also shows that temperature ripple on Cth_2 is in the 0.1°C range and that there is essentially no ripple on Cth_3. Heat flow from the heat sink and into the environment is shown in Figure 10. As would be excepted, no heat flows initially and heat flow steadily increases as the heat sink's temperature rises.

A test lasting 14 seconds lends itself to methods of verification. A thermocouple placed on the MOSFET's tab read 25.0°C at 14 seconds. The model's discrete thermal capacitances and resistances are chosen to provide a response similar to the actual response of the distributed Rs and Cs of the heat sink. They do not represent physically discrete capacitances associated with specific elements of the circuit. Therefore, the tab temperature should not be expected to be equal to the temperature appearing at any of the three thermal capacitances. However, the change in the tab temperature can be tracked, and it should follow the temperature rise of the body of the MOSFET and the heat sink. That indeed proves to be the case, because between 5 and 14 seconds the simulated tab temperature increases at the same rate as the temperature of Cth_2 and Cth_3.

A second simulation and an alternate method is needed to get results at steady state without very long simulation times. The trick is to decrease the size of the thermal capacitances so that they are more easily charged to their final temperatures. Keeping some thermal capacity in the system keeps the junction temperature from swinging wildly with variations in power dissipation. Without any capacitance, variations in power dissipation generate unrealistically large swings about the steady state value. These swings might be high enough to cause problems in the simulation. The waveforms in Figure 11 represent the system's performance with Cth_2 set to 0.03°J/C and Cth_3 set to zero. The steady state value of the empirical test was 63.4 degrees, which matches very well with the simulation.

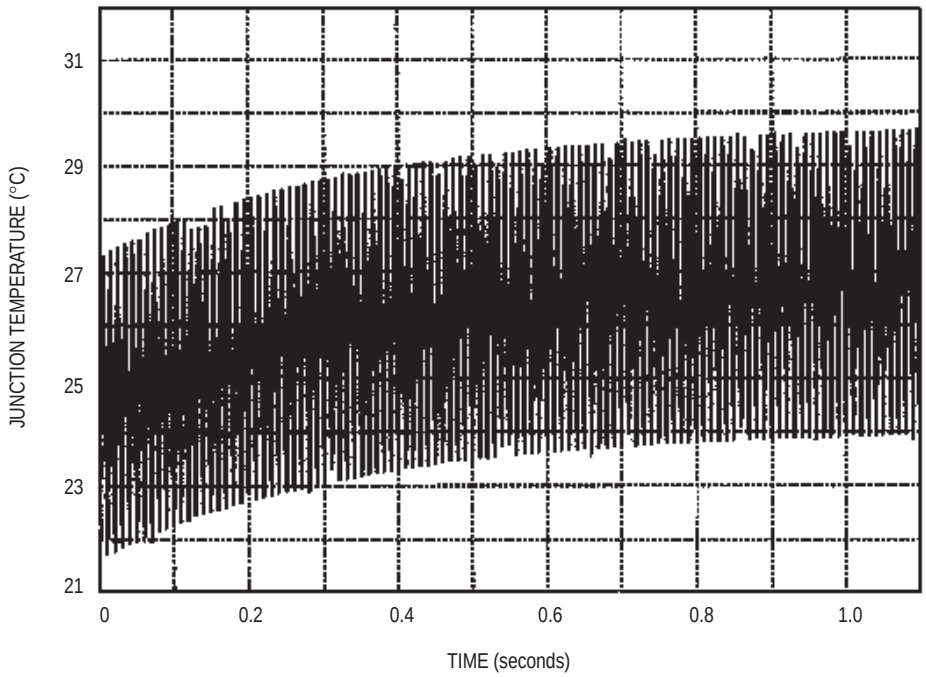

Figure 7. Junction temperature during the first 1.1 seconds of operation

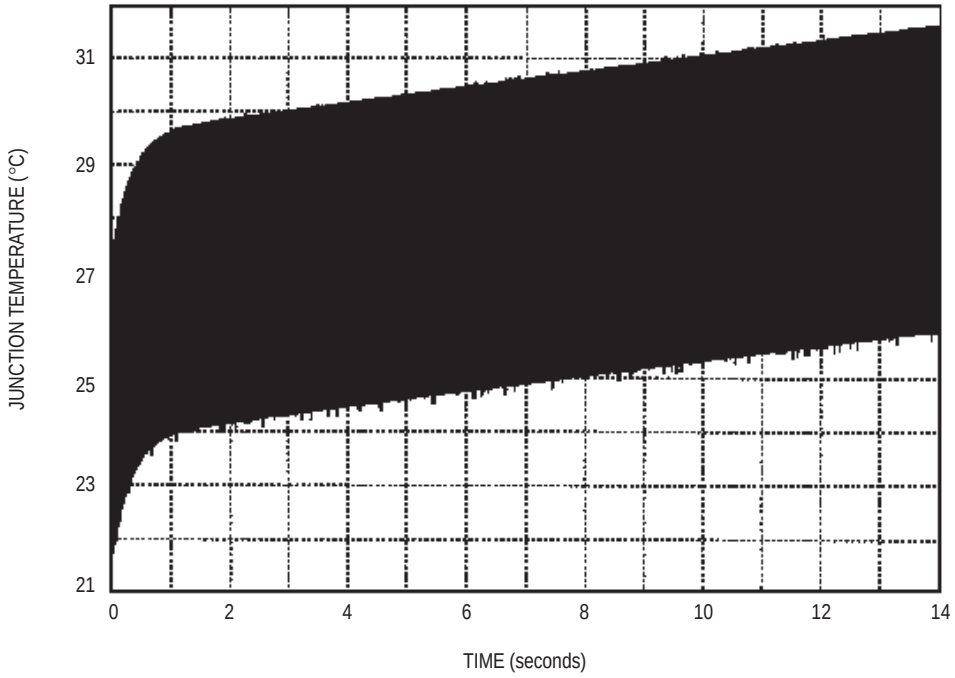

Figure 8. Junction temperature during the first 14 seconds of operation

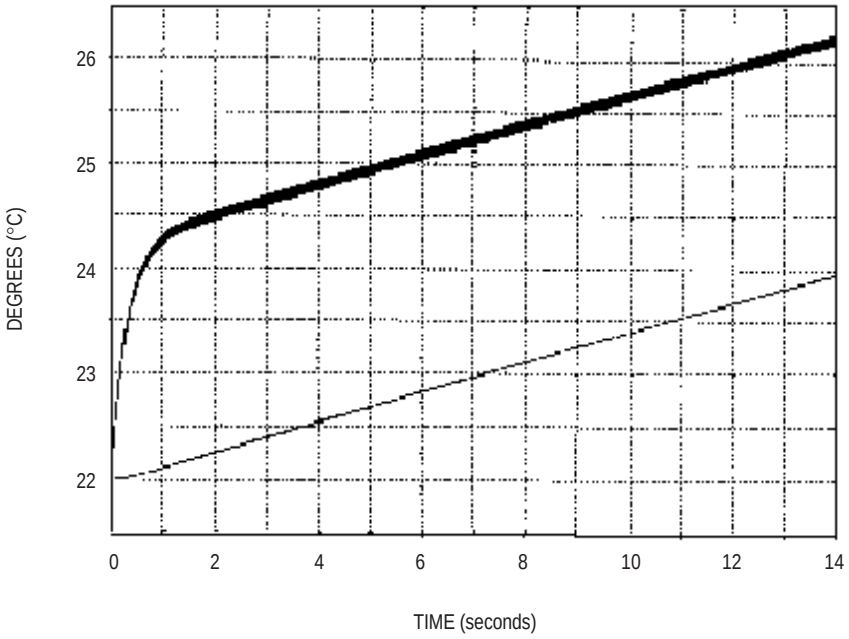

Figure 9. Temperature rise at Cth_2 and Cth_3 clearly show the different thermal time constants that make up the thermal response

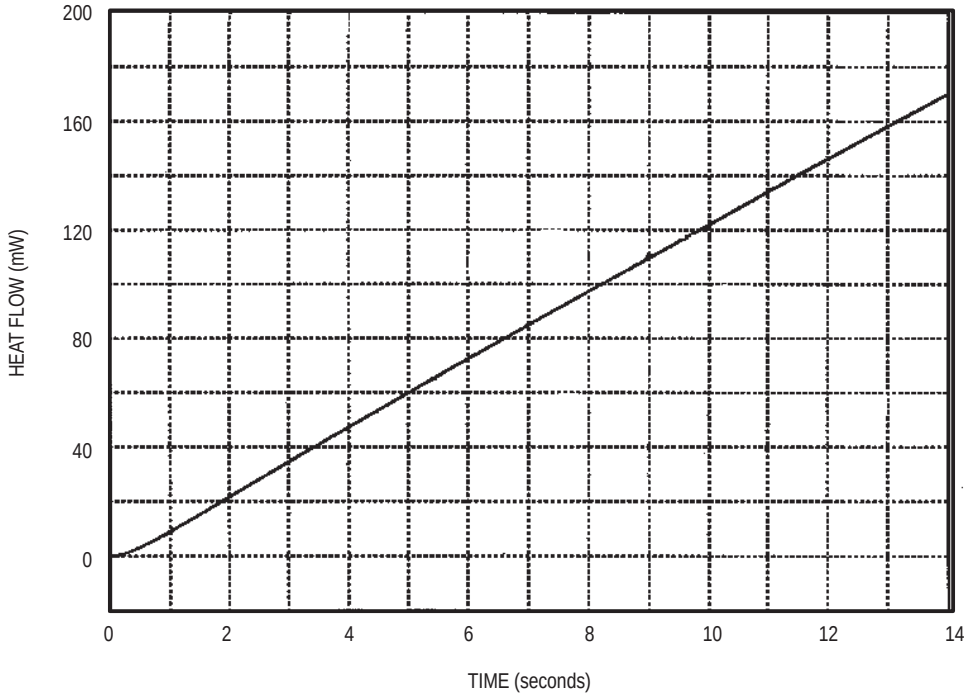

Figure 10. Simulation shows that little heat flows into the environment during the first 14 seconds of operation.

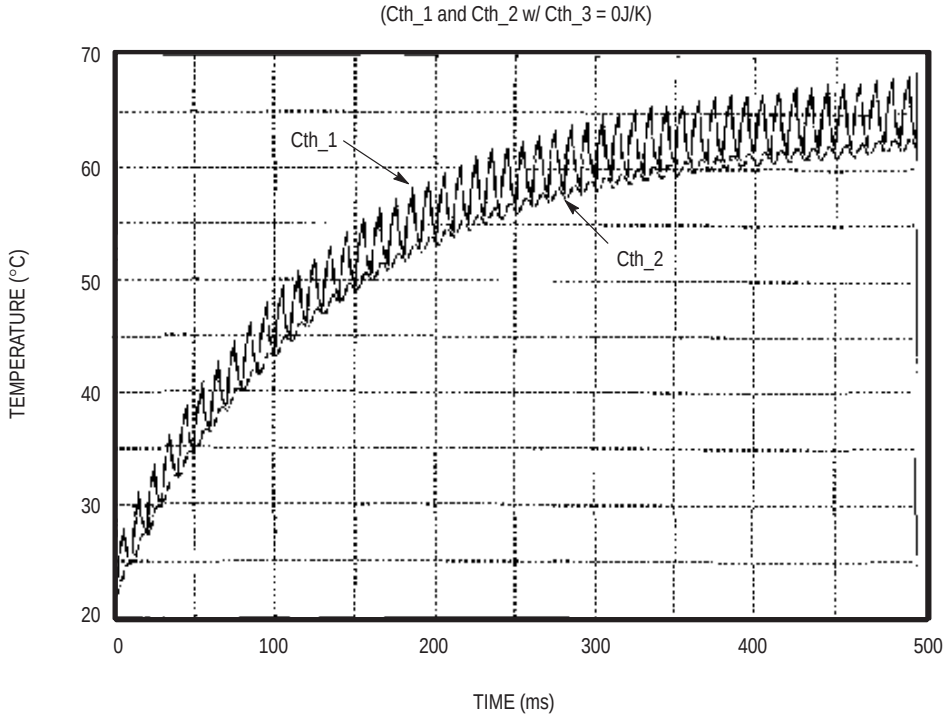

Figure 11. Dramatically reducing the size of the largest thermal capacitances allows the simulator to quickly find solutions for steady state conditions.

Other Tips

When using Analogy's SABER program, it is good to know how the program assigns default values of thermal resistance. The program looks to see if the user specifies Rth_hs or Rth_jc. If the user defines Rth_hs, SABER uses that value and the value of Rth_jc specified on the manufacturer's data sheet. If Rth_hs is not specified, SABER uses the value of Rth_ja specified on the manufacturer's data sheet in place of Rth_jc and Rth_hs. Rth_ja is the device's junction to ambient thermal resistance without a heat sink, and its value for a TO–220, for example, is quite large, 62.5°C/W. Defaulting to such a large thermal resistance might cause unrealistic junction temperatures and invalid results or even convergence problems.

In release 4.0 of SABER, Analogy's thermal models do not contain thermal capacitance. To add your own thermal network, including thermal capacitance, set the MOSFET's Rth_hs and Rth_jc to very small values (0.001 °C/W was used in these simulations) and then add your own thermal network, including thermal capacitances and thermal resistances.

SUMMARY

The tools and techniques described here proved to be an effective means of predicting power transistor junction temperature of two different MOSFETs operating in three types of circuits with two different heat sinks. This methodology is also useful for understanding how circuit performance varies with changes in the power transistor, the thermal interface between it and the heat sink, and the heatsink itself. The uniqueness of the approach is the use of a combination of newly developed tools, all of which are readily available to the power electronics community.

ACKNOWLEDGMENTS

Special thanks to Gary Dashney, Tanya Fowler, and Larry Walker of ON Semiconductor for developing the technique of measuring transient thermal response of systems with very long thermal response times and for characterizing the MOSFET/heatsink assembly used in this study.

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SPICE Generates the Thermal Response Models of a Power Semiconductor

Gary E. Dashney, Lab Manager
Larry Walker, Characterization Engineer
ON Semiconductor
Phoenix, Arizona

INTRODUCTION

An equivalent electric circuit consisting of a resistor–capacitor network can be used to describe both the steady–state and transient thermal response of a power semiconductor device. Combined with SPICE, this network is extremely useful in determining a device's junction temperature for any input power condition or waveform that can be modeled in SPICE.

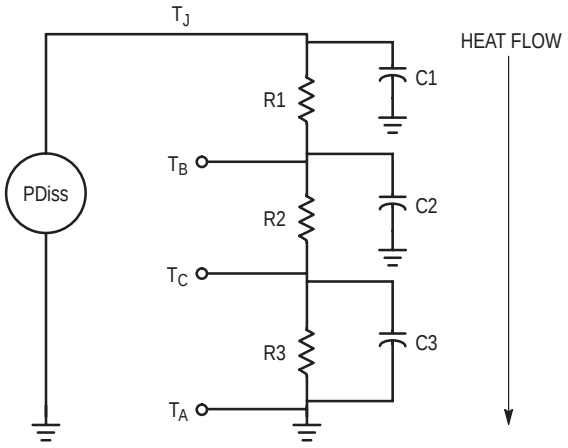
This paper will cover the following topics:

- Understanding basic transient thermal response of power semiconductors
- Basic transient thermal response test methods
- The thermal equivalent SPICE model
- Examples of using SPICE to model transient thermal response of power devices

Understanding Basic Transient Thermal Response of Power Semiconductors

Having already described the basic thermal parameters of power semiconductors in "**Basic Semiconductor Thermal Measurement"**, [1] this paper will focus primarily on the thermal equivalent circuit and how it applies to transient and steady–state thermal analysis.

The thermal behavior of a power semiconductor device can be described by a resistor–capacitor network as shown in Figure 1. This network shows the most commonly used thermal equivalent model for a power semiconductor. More elements (RC sections) can be added to increase the model detail as required. The third order model shown in Figure 1 is relatively simple yet accurately describes the thermal performance of a power semiconductor device.



Heat generated in a device's junction flows from a higher temperature region through each resistor–capacitor pair to a lower temperature region.

Figure 1. Thermal Electrical Equivalent Circuit

The thermal circuit shown in Figure 1 is governed by three basic equations which are similar to the three forms of Ohm's law.

Thermal Equation	Electrical Equivalent	
$R_{th} = \Delta T/P_D$	$R = V/I$	(1)
$\Delta T = P_D * R_{th}$	$V = I*R$	(2)
$P_D = \Delta T/R_{th}$	$I = V/R$	(3)

Where:

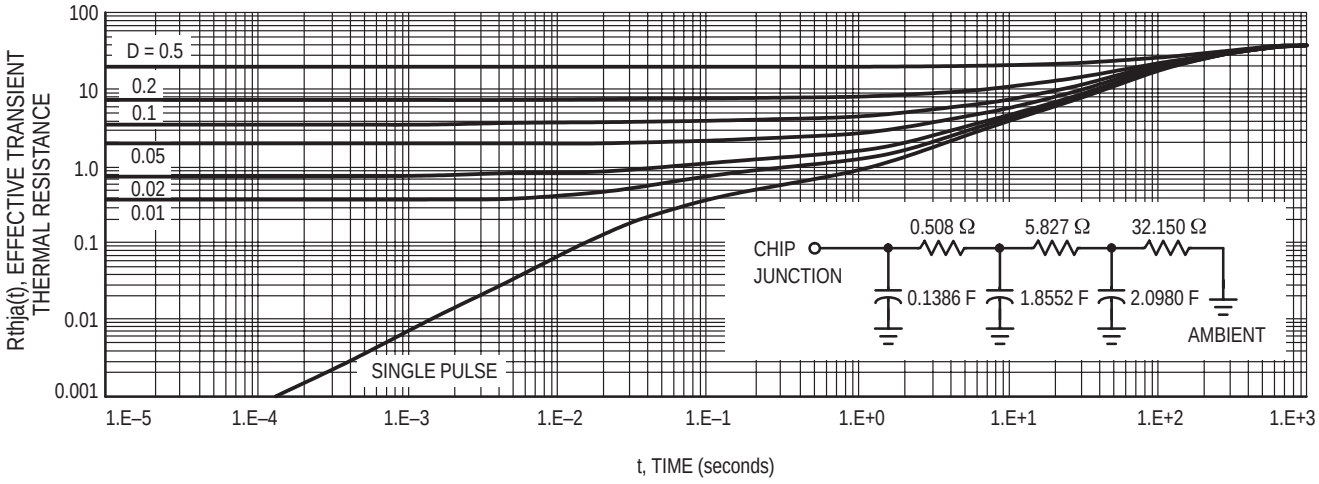
- R_{th}, thermal resistance, is analogous to resistance
- ΔT is analogous to a voltage drop
- P_D, power dissipation, is analogous to current flow
- a *voltmeter* is analogous to a thermometer

Resistors R1, R2, and R3 in Figure 1 are all analogous to individual thermal resistances, or quantities that impede heat flow. Resistor R1 represents the thermal resistance from the device's junction to its die–bond. The "junction" of a power semiconductor, whether it be a pn interface or a schottky barrier, is the location where heat is generated within the device. Resistor R2 represents the thermal resistance from the die–bond to the device's case. Resistor R3 repre-

sents the thermal resistance from the device's case–to–ambient. The steady–state thermal resistance from the junction to some reference point is equal to the sum of the individual resistors between the two points. For instance, the thermal resistance, R_{thjc}, from junction–to–case is equal to the sum of resistors R1 and R2. The thermal resistance, R_{thja}, from junction–to–ambient, therefore, is equal to the sum of resistors R1, R2, and R3.

The capacitors shown in Figure 1 help model the transient–thermal–response of the device. When heat is instantaneously applied and or generated, a thermal charging takes place as heat passes from one point to another with–in the device. This charging effect and/or transient thermal response, as it is traditionally called, follows an RC time constant determined by the resistors and capacitors in the thermal network.

The thermal resistance at any given point in time is equivalent to the total impedance of the circuit under applied power at that time. The total impedance of the network would initially be small and increase over time as the capacitors charge (see Figure 2). As time progresses and the capacitors fully charge, a steady–state condition is reached. When a steady–state condition is reached, the total impedance is simply the sum of the resistors R1, R2, and R3. The total impedance as a function of time is called transient thermal resistance, $R_{thjr(t)}$.



The device shown is mounted on a standard 2 inch square FR4 board with minimum recommended pads. The initial transient thermal resistance starts out very low and increases over time until it reaches its steady–state value.

Figure 2. Transient thermal response curve for an MTV32N20E D3Pak surface mounted power MOSFET device with RC values shown.

Basic Transient Thermal Response Test Methods

The old traditional method of measuring transient thermal response is as follows:

1. Heat the device by applying power until it reaches steady–state
2. Remove the power from the device and begin sampling the TSP (**T**emperature **S**ensitive **P**arameter)
3. Reduce the collected TSP data and normalize it for graphing

This is known as the cooling curve method because the thermal response is measured while the device is cooling. Theory states that the cooling curve is identical to the heating curve, but it is the heating not the cooling of the device that the circuit designer is really interested in. The collected data, therefore, would have to be re–arranged and presented as a heating–curve similar to that shown in Figure 2.

Generally, the best approach to quantify the transient thermal behavior of a device is to generate a heating characterization curve. This is usually done by applying constant power pulses for varying lengths of time and measuring the thermal impedance for this time period. Unfortunately, the applied pulses, for all practicality, are usually rectangular. The data obtained, therefore, represents only rectangular pulses. With this type of transient data (i.e.. rectangular heating pulse) the user must apply his own design conditions by adjusting for non–rectangular pulses. This is usually done with some sort of equivalent and/or superposition technique. [3]

One big advantage that some of the latest test equipment provides is the generation of the RC network values shown in Figures 1 and 2. The RC network values are derived by using error–minimization routines to solve the differential equations that describe the thermal circuit behavior. Actual versus simulated thermal response data for the MTV32N20E device is shown in Figure 4. The RC network derived by these testers provides both the designer and the device manufacturer with a tremendous tool. Thermal circuit RC networks can also be extracted from the collected data by using such software as Sauna™ from Thermal Solutions (313–761–1956).

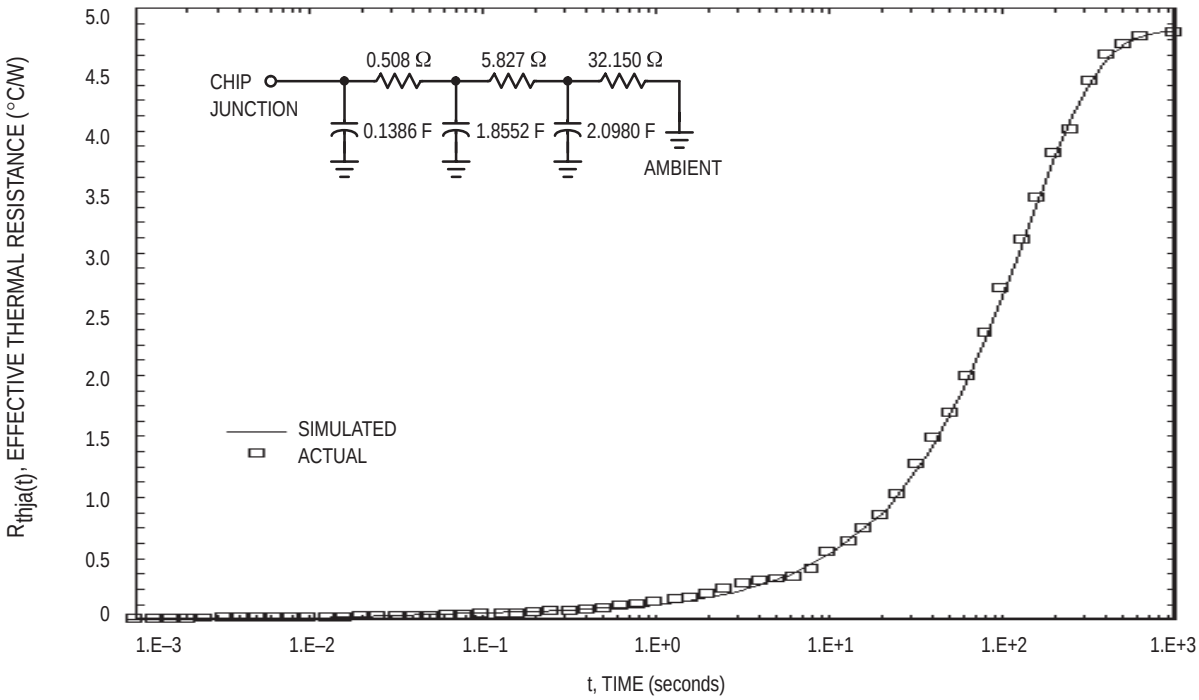


Figure 3. Simulated and actual transient thermal response curves and the thermal equivalent circuit for the MTV32N20E power MOSFET device mounted on a 2 in. x 2 in., 2 oz. Cu, FR4 board with the minimum recommended footprint.

The main advantages of using an RC network for thermal modeling are:

- Individual thermal resistances and time constants of the device's internal package can be shown
- Provides the opportunity to determine where package enhancements can be made to improve thermal performance
- The ability to simulate the device's thermal behavior using SPICE under any power pulse condition

The Thermal Equivalent SPICE Model

Using SPICE, equations (1), (2), and (3), and the RC network derived from the transient thermal response measurements, a model of the thermal behavior for a device under various power conditions can be generated. This provides the designer with a direct way to determine a device's operating junction temperature under the unique electrical conditions of the application circuit, thus insuring circuit reliability.

The p–channel MOSFET, MMSF4P01Z, packaged in an SOIC8 platform will be used to demonstrate the application of this thermal modeling technique. Shown in Figure 4 is the transient thermal response for the MMSF4P01Z along with its synthesized or derived equivalent thermal RC network. A sample SPICE input deck for the thermal circuit is illustrated in Figure 5. It should be recalled that current in the electrical circuit is analogous to power dissipation in the thermal circuit (equation 3), hence, the reason for the current sources in the circuit program. Figure 5 represents the SPICE input deck which produces the input and output waveforms of Figure 6. As can be seen, multiple power inputs can be used to create fairly complex power dissipation waveforms. Keep in mind that the input stimulus to the thermal circuit is power, which is the product of the voltage and current applied to the device of interest.

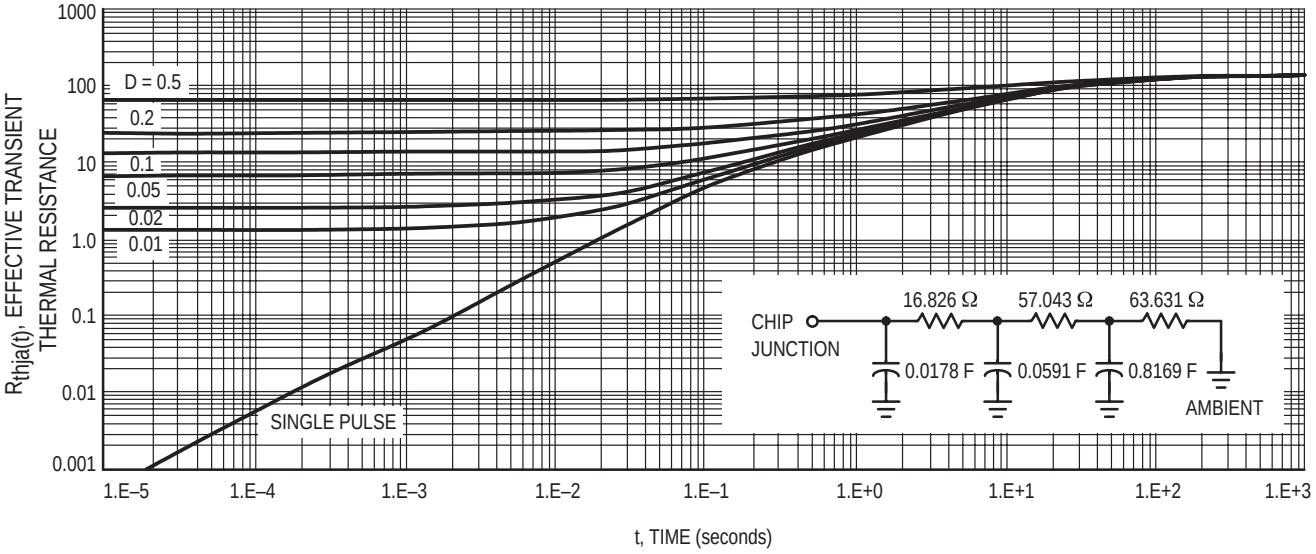


Figure 4. Transient thermal response curve and thermal equivalent circuit for the MMSF4P01Z power MOSFET device mounted on a 2 in. x 2 in., 2 oz. Cu, FR4 board with the minimum recommended footprint.

```
THERMAL RESPONSE SIMULATION – MMSF4P01Z
*
IPDISS1  0   1    PULSE(0A 1A 0S 10MS 1US 1US 20MS)
IPDISS2  0   1    PULSE(0A 20A 0S 10MS 1US 1US 20MS)
CT1      1   0    17.8296M
RT1      1   2    16.8620Ω
CT2      2   0    59.0954M
RT2      2   3    57.0433Ω
CT3      3   0    816.901M
RT3      3   0    63.6307Ω
*
.TRAN 1MS 0.2S
*
.OPTIONS LIMPTS=20000 RELTOL=0.002
.PROBE
.END
```

Figure 5. SPICE input deck used to simulate the thermal circuit of MMSF4P01Z and generate the input and output waveforms seen in Figure 6. Concerning the units in the SPICE deck, “M” means 10^{-3} and “U” means 10^{-6}.

Many courses, books and other forms of instruction are available concerning programming and operating SPICE software.[5] These subjects are not the intended scope of this paper. As stated before, Figure 6 represents the input and output waveforms of the SPICE input deck of Figures 3 and 4. Figures 6, 7, and 8 demonstrate the use of the same thermal circuit with other input patterns applied. The solid waveform in these figures is the input power to the thermal circuit. The dashed line represents the junction temperature of the device with this input power applied. As one can probably tell from Figures 3 and 8, it takes several hundred seconds for the MMSF4P01Z to reach a stable thermal condition, i.e. steady–state. What is pleasantly apparent, is that with a given RC network, which leads to a simple SPICE input deck, and the power input waveform information, the junction temperature condition can be easily ascertained. Of course, everything has a limit. If very complex input power waveforms which have short time intervals with respect to steady–state stabilization time are applied for extremely long time periods, one may run out of simulation capability. Figure 9, for example, represents approximately 4000 data points. The simulation for that particular example produced around 9000 data points all the way out to 1000 s.

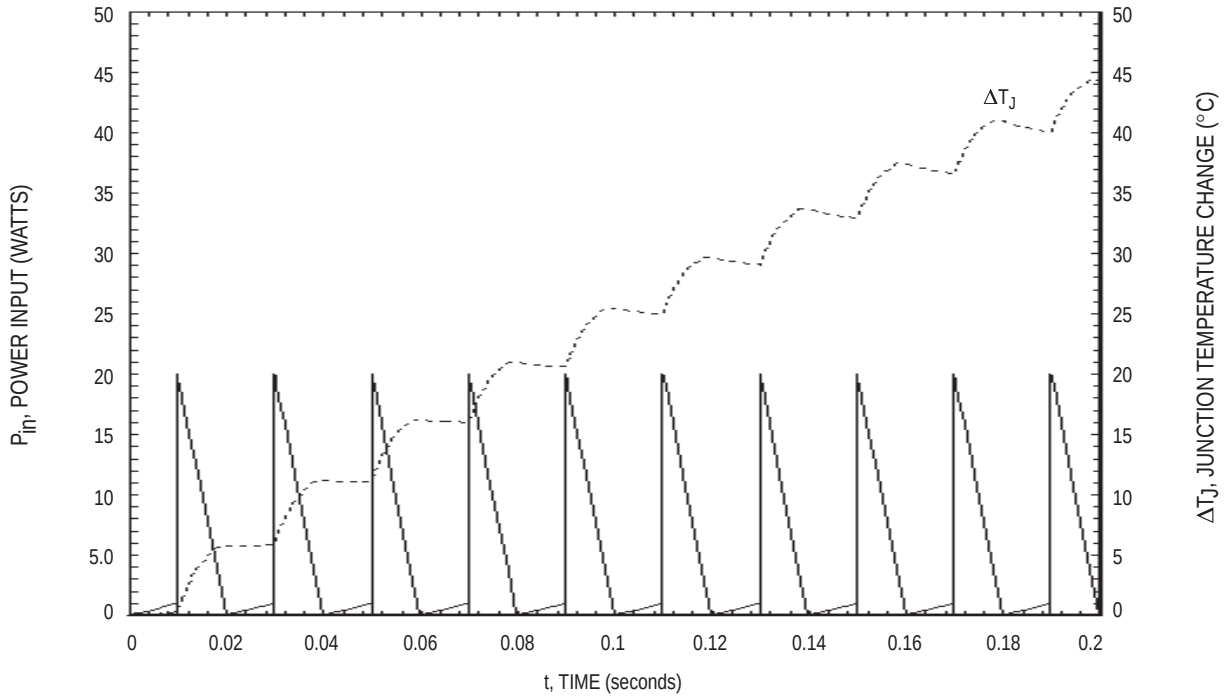


Figure 6. Input (power) and output (temperature) waveforms for the SPICE simulation of the thermal circuit given in Figures 3 and 4 with a complex waveform as input.

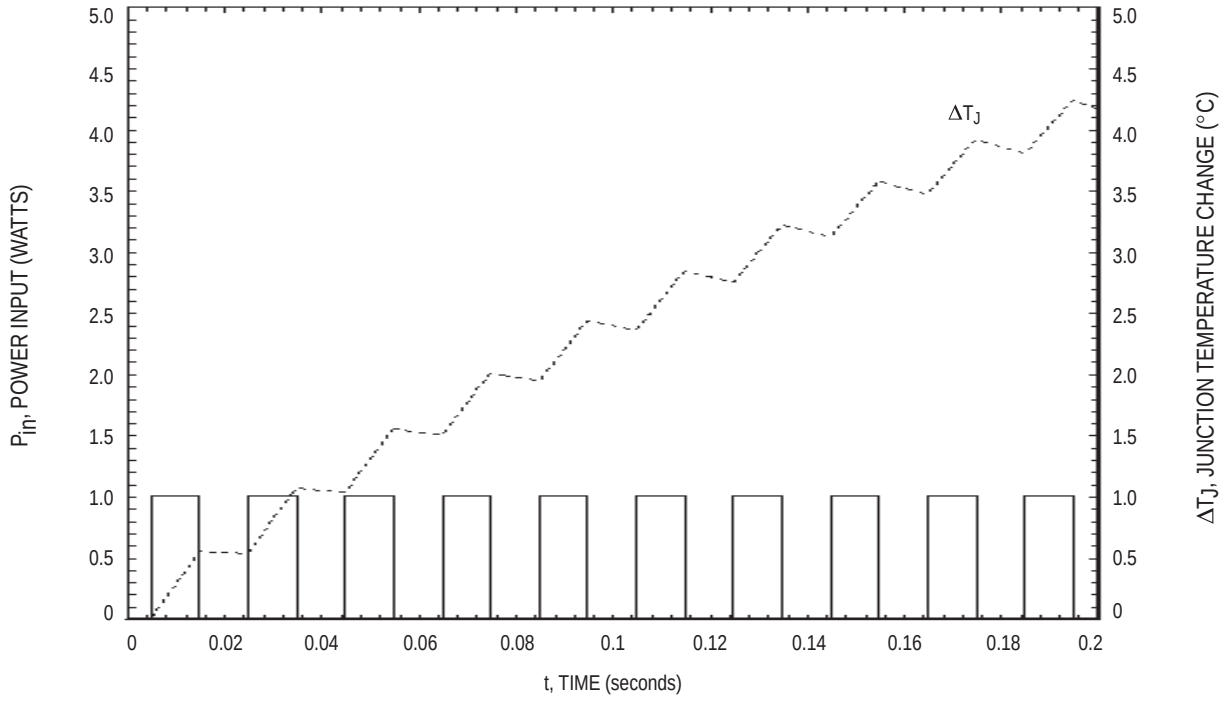


Figure 7. Input (power) and output (temperature) waveforms for the SPICE simulation of the thermal circuit given in Figures 3 and 4 with a simple square waveform as input.

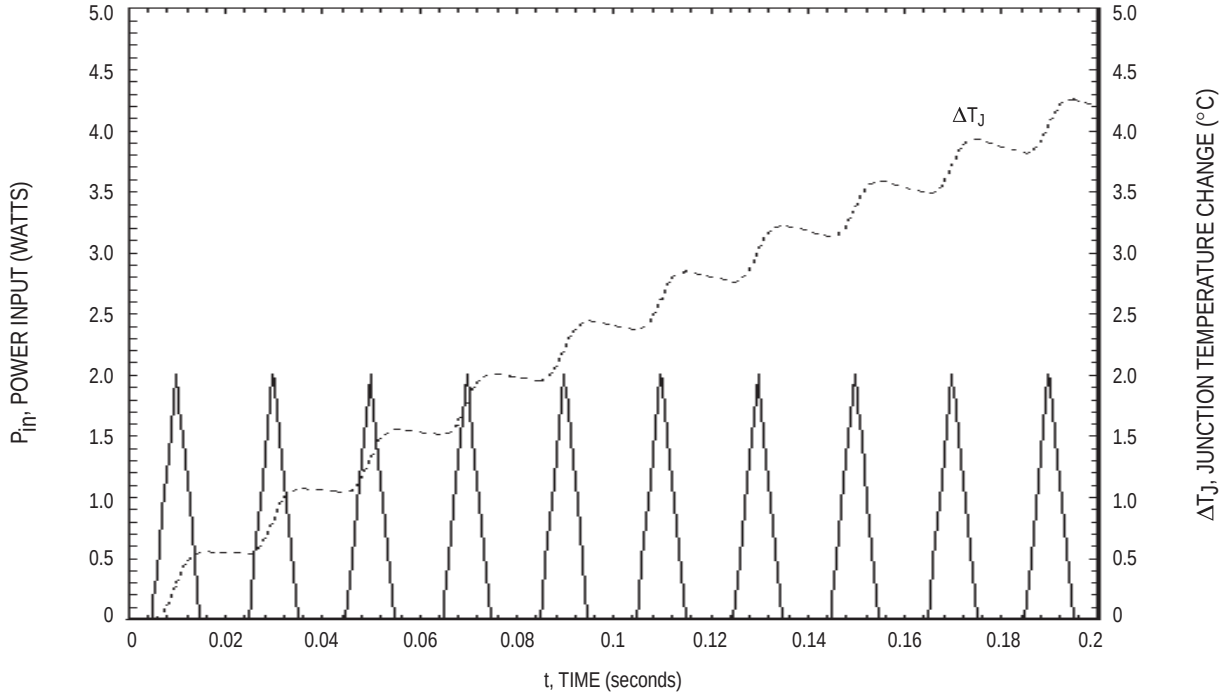


Figure 8. Input (power) and output (temperature) waveforms for the SPICE simulation of the thermal circuit given in Figures 3 and 4 with a simple triangular waveform as input.

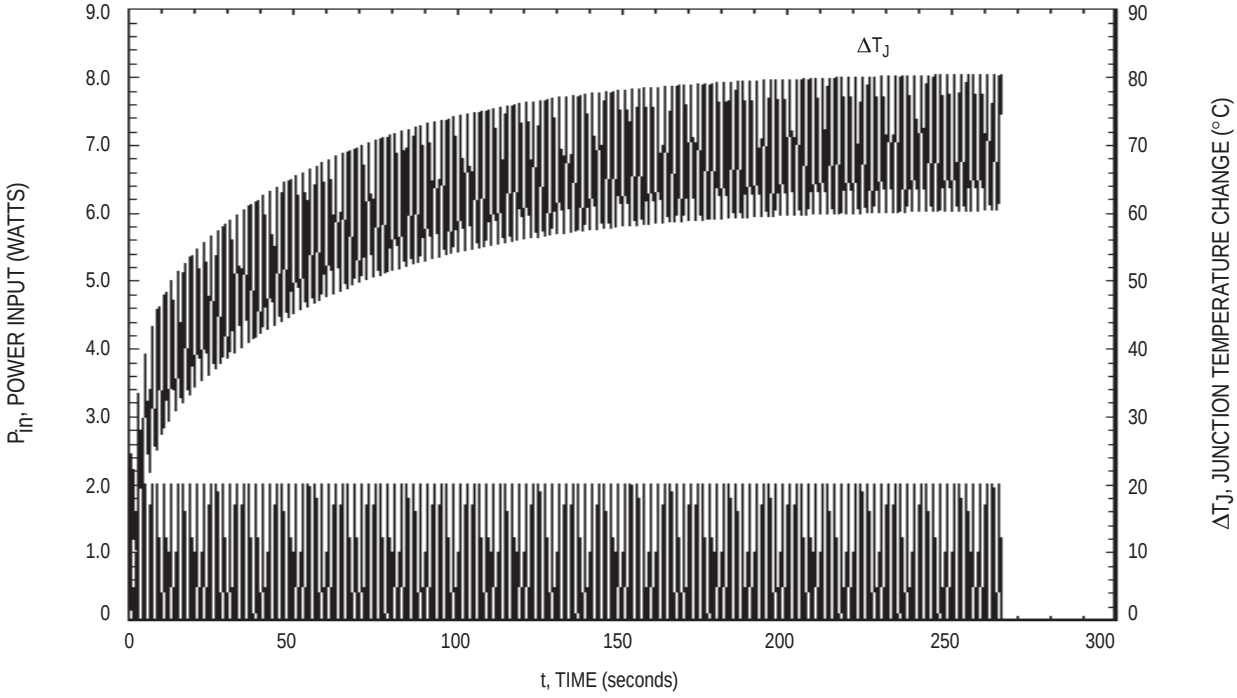


Figure 9. Input (power) and output (temperature) waveforms for the SPICE simulation of the thermal circuit given in Figures 3 and 4 with a low frequency triangular waveform as input. The analysis was carried out until the junction temperature had practically reached steady−state.

SUMMARY

In many situations, the design engineer is faced with the challenge of taking the manufacturers' specifications and characterization data and applying them to their unique application. For power semiconductor thermal performance, the hurtle is taking a thermal characterization for a device based on rectangular power pulse waveforms and transforming this information into useful results for a completely different power application. The attempt of this paper was to present a technique that can greatly reduce this obstacle. Given the RC thermal equivalent network for a device, the known input power waveforms and a circuit simulator, it is a fairly straight forward process to ascertain exactly the junction operating condition of the device. Realizing the power of this tool, some manufacturers, such as ON Semiconductor, are beginning to include this thermal circuit information in their data sheets.

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[1] Dashney, Gary E., "Basic Semiconductor Thermal Measurement", 1995, ON Semiconductor.

[2] Gottlieb, Irving M., 1992, *Regulated Power Supplies*, 4th Edition, Blue Ridge Summit, Pennsylvania, TAB BOOKS: (92–105).

[3] Roehr, Bill and Bryce Shiner, "Transient Thermal resistance — General Data and its Use", AN569 in ON Semiconductor *Power Applications Manual*, 1990, DL140/D: (23–38), Ph. (800–441–2447).

[4] Sofia, Dr. John W., "Analysis of Thermal Transient Data with Synthesized Dynamic Models for Semiconductor Devices", Analysis Tech, Wakefield, MA 01880, Ph. (617) 245–7825.

[5] Tuinenga, Paul W., SPICE: A Guide to Circuit Simulation and Analysis Using PSpice®, Second Edition, © 1992 Prentice–Hall, Inc.

Tools for Analyzing the Power Transistor and Its Thermal Environment

Kim Gauen, Motorola SPS
Heather Neal, Purdue University

ABSTRACT – New models, tools, and techniques are now available for simulating the power transistor and its thermal environment. This paper validates one dynamically temperature dependent power MOSFET model, presents simulation results for a relatively simple thermal network, and shows how more complex networks might be analyzed.

INTRODUCTION

Power transistors continue to play an important role in modern society. They are critical in a myriad of energy conversion applications, so they must perform reliably, efficiently, safely, and economically. This service comes at a cost. The 1996 power transistor market is expected to be $1.2B, and the forecast for the year 2000 is $1.6B.

Designers using power transistors must meet ever tightening cost targets and ever increasing performance goals – and in less design time. Without new tools to assist designers, new products may not meet targeted introduction dates or performance specifications.

Because the power transistor naturally dissipates heat during power conversion, power electronic circuit analysis must include a study of the thermal environment and thermal effects on the power transistor. Until now such evaluations were difficult and time consuming, but the introduction of new tools and the development of new techniques are improving the design process.

The power MOSFET's popularity made it the choice for the focus of this paper. The concepts described herein are useful for all power electronic devices and are only limited by the availability of models that describe their electrical and thermal behavior.

New Modeling Tools

Two new developments in modeling the power transistor are:

1. the development of simulators that can work as comfortably in an interactive thermal and electrical domain as well as just the electrical domain
2. the appearance of new power transistor models that support the new simulation tools.

Few simulators support thermal as well as electrical models, allowing the electrical system to affect the thermal and vice versa. For example, in SPICE based simulators system variables are constrained to voltage and current. In order to simulate non–electrical systems in these types of simulators, the nonelectrical system must be written in terms of equivalent electrical elements, or macro–models. Macro modeling techniques of electro–thermal systems suffer from their inability to directly adjust the internal electrical model parameters for the non–electrical changes in the system. To circumvent this limitation, the user is forced to make gross adjustments to the external nodes of the circuit through controlled sources or other elements.

A second approach possible with SPICE based simulators is to write a completely new model. This is challenging since the model must be compatible with the underlying SPICE code. The complexity of the task and the possibility of disrupting the operation of the SPICE code makes macro modeling a more feasible and popular option. But as discussed above, macro modeling has its own set of problems, not the least of which is a large number of additional nodes, which will increase simulation time.

Simulators such as Analogy's SABER provide a modeling language which separates the simulation "engine" from the models. This allows the user to develop models as a system of through and across variables that are not constrained to voltage and current. Thus, the relationship between electrical and thermal variables can be described directly in the model with a hardware description language. Analogy's hardware description language is MAST™.

The second requirement is having an accurate and robust power transistor model that is also "dynamically" temperature dependent. ("Dynamic" temperature dependence is explained below.) This model should accurately predict the I–V characteristics for the forward range of operation, as well as leakage, reverse recovery and breakdown characteristics of the drain–source body diode. The electrical model must also describe the nonlinear gate–drain (and gate–source for negative V_{GS}) capacitances that are key to accurate transient simulations.

In the language of simulation a "robust" model is one that does not cause convergence problems, which are most commonly the result of discontinuities in the model. Many SPICE based subcircuit models have been introduced over the years in an attempt to describe the nonlinear power MOSFET capacitances; however, the macro modeling approach introduces discontinuities. Although such discontinuities may be acceptable in a purely electrical simulation environment, the complexity of the dynamic electro–thermal system requires models with superior convergence qualities.

To date, the models common throughout the industry have been "static" thermal models. This means that the designer can assign any reasonable temperature to the model prior to simulation. However, device temperature will remain constant throughout the simulation, regardless of power dissipation.

Instead of this static model, we require a “dynamic” thermal model that allows the device temperature to change as electrical energy is converted to heat. To accomplish this, the temperature parameter used inside the MOSFET model to adjust the electrical parameters for thermal effects must now become an independent variable solved by the simulator. When temperature is an independent variable, the simulator must solve a set of simultaneous nonlinear differential equations for temperature and heat flow as well as for voltage and current for each node and each time step.

The SABER simulator uses a dynamic thermal version of the MPV3 MOSFET model (MPV3X). This model is the basis of the library of ON Semiconductor MOSFET models provided with the 4.0 release of SABER.

Validating the MOSFET Model

Validating the dynamically temperature dependent MOSFET model is a prerequisite to verifying its general usefulness. Designers are normally most interested in the MOSFET’s on–resistance (to understand on–state losses) and its switching characteristics (to estimate switching losses). Table 1 shows $R_{DS(on)}$ data and other simulated and empirical DC characterization data at room and elevated temperature. Small differences between the simulated and empirical results should be expected since the devices measured here were not the same units used to generate the model.

Table 1. Measured and Simulated DC Characteristics of the MTP15N06V

	Measured		Simulated	
	25°C	150°C	25°C	150°C
$R_{DS(on)}$ @ 10 A	103 mΩ	210 mΩ	101 mΩ	198 mΩ
Diode Vf @ 10 A	0.93 V	0.80 V	0.91 V	0.80 V
BVdss @ 1 mA	73 V	81 V	75.4 V	83.9 V
V_{GS} @ 10 A	6.1 V	6.1 V	5.9 V	6.0 V
Vth @ 1 mA	2.90 V	2.29 V	2.88 V	2.30 V

Measurement errors and differences in measurement equipment and techniques probably account for some of the differences in Table 1.

The MOSFET characteristics that determine switching behavior are its input capacitance and its transfer characteristics. The gate charge test is a low frequency test that yields much information about input capacitance. Figures 1 and 2 show the modeled and actual waveforms from a gate charge test.

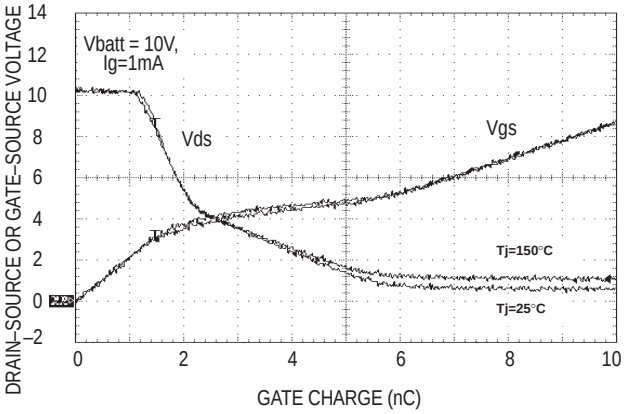


Figure 1. Measured High and Low Temperature Charge Waveforms of the MTP15N06V

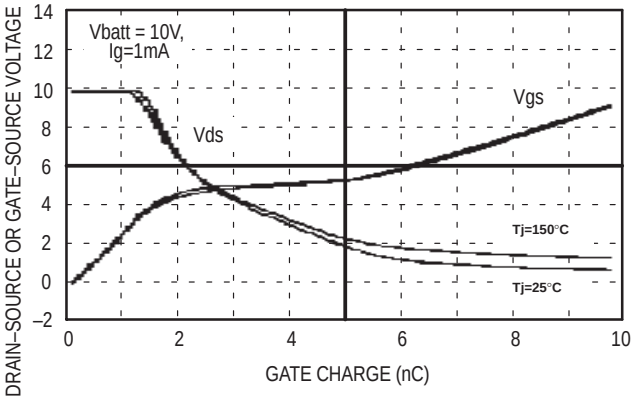


Figure 2. Simulated High and Low Temperature Charge Waveforms of the MTP15N06V

The high temperature V_{GS} waveform closely tracks the low temperature curve, and the V_{DS} waveform changes primarily because the $R_{DS(on)}$ affects the on–state voltage. The slopes of V_{GS} and V_{DS} waveforms can be related to the input capacitances at their specific operating voltage. The capacitances influence the shape of the gate charge waveforms and, by extension, all MOSFET switching waveforms. A known source of error in the actual waveforms shown here is that the load resistor had an inductive component which was estimated to be 3.1 μH.

As can be seen from Figures 1 and 2, the MOSFET’s switching speeds are largely temperature invariant. The characteristic that varies with T_J (junction temperature) is the gate voltage’s amplitude during the “plateau” region. Since the plateau voltage is determined by the transfer characteristics (I_D vs. V_{GS} at V_{DS} = 15 V), it is important that the transfer characteristics be modeled well. Again, considering measurement error and likely variation among devices, the simulated and measured results in Figures 3 and 4 match pretty well.

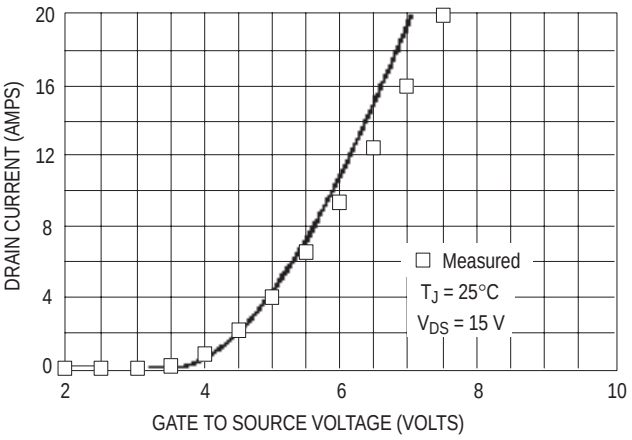


Figure 3. Measured and Simulated Transfer Characteristics of the MTP15N06V at 25°C

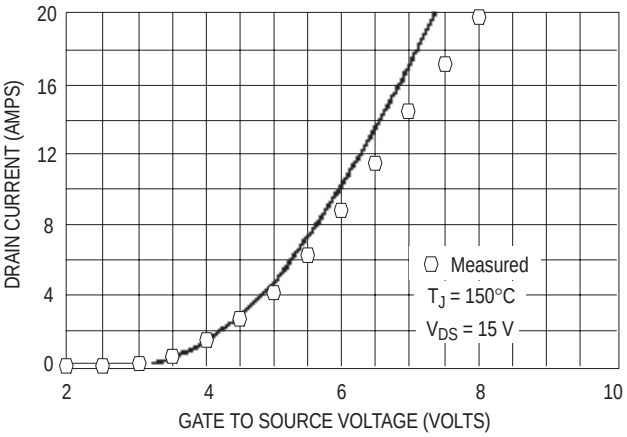


Figure 4. Measured and Simulated Transfer Characteristics of the MTP15N06V at 150°C

Measured and simulated turn on and turn off waveforms at low and high temperature are shown in Figures 5a, 5b, 6a, 6b, 7a, 7b, 8a and 8b.

In the turn off waveforms a 103 pF capacitor was added across the MOSFET's drain and source terminals to account for parasitic circuit capacitance and capacitance associated with the load resistor. The matching switching waveforms complete the validation of the MOSFET model. The next task is to generate accurate thermal models of the MOSFET and its environment.

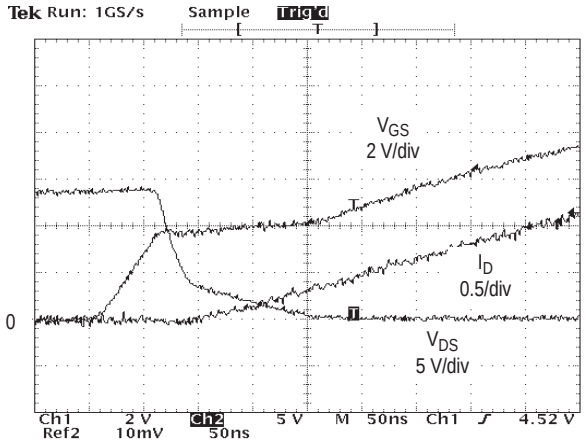


Figure 5a. Measured Turn On of an MTP15N06V at 33°C (50 ns/div)

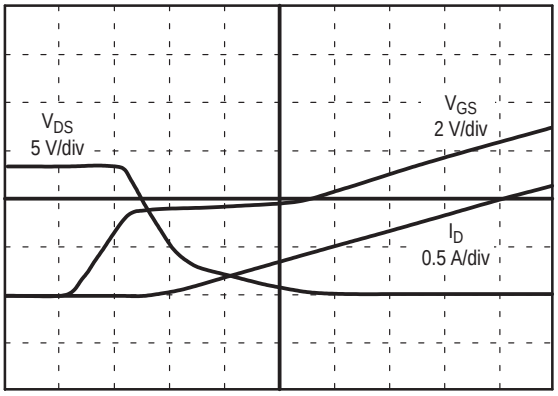


Figure 5b. Simulated Turn On of an MTP15N06V at 33°C (50 ns/div)

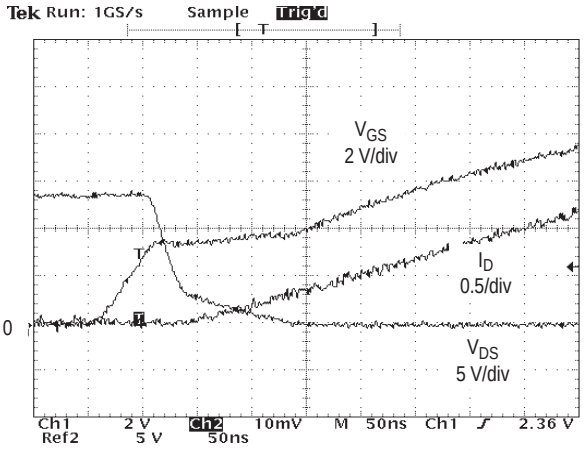


Figure 6a. Measured Turn On of an MTP15N06V at 116°C (50 ns/div)

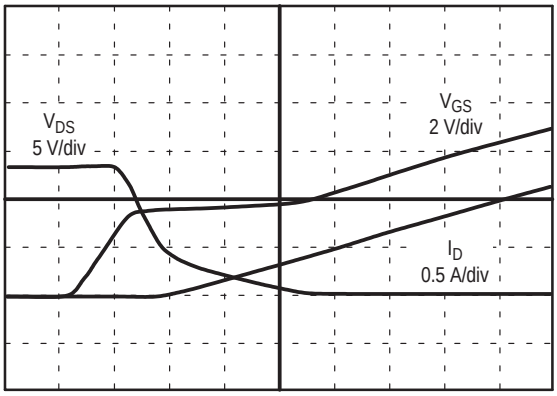


Figure 6b. Simulated Turn On of an MTP15N06V at 116°C (50 ns/div)

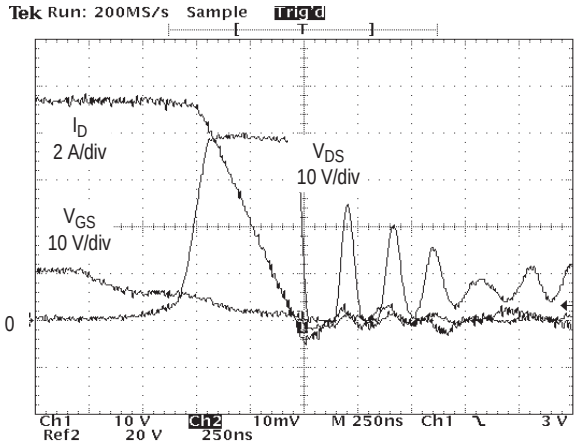


Figure 7a. Measured Turn Off of an MTP15N06V at 33°C (250 ns/div)

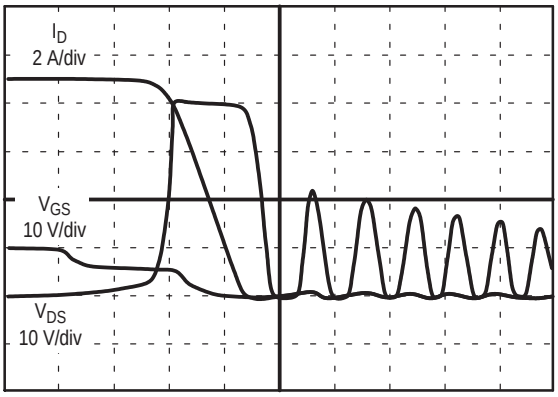


Figure 7b. Simulated Turn Off of an MTP15N06V at 33°C (250 ns/div)

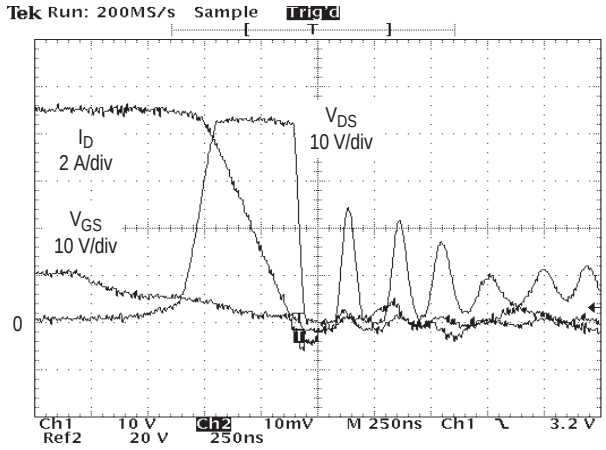


Figure 8a. Measured Turn Off of an MTP15N06V at 116°C (250 ns/div)

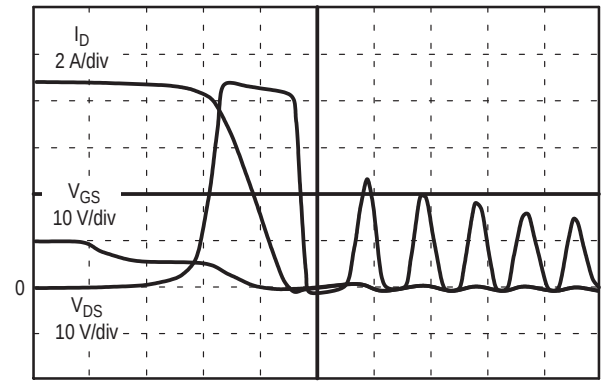


Figure 8b. Simulated Turn Off of an MTP15N06V at 116°C (250 ns/dv)

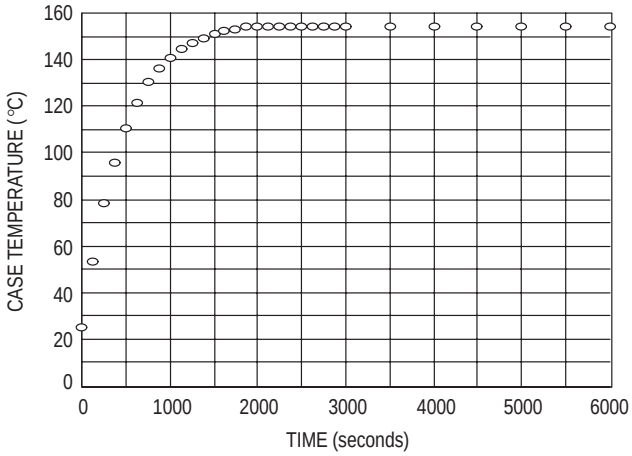


Figure 9. Measured Case Temperature with 7 W Load

Characterizing a Simple Thermal Network

For those unaccustomed to working in the thermal domain, Table 2 serves as a quick reminder of the basic thermal relationships.

The ultimate requirement in characterizing a power transistor's thermal environment is to obtain an accurate thermal model of any transistor/heatsink combination. To validate the modeling process, we took an intermediate stage, i.e., reduced the complexity of the heatsink so that a simple thermal RC network would adequately model the entire thermal network. For this purpose we used a 40 by 20 by 12 mm aluminum heatsink that had no fins. The thermal resistance and the thermal capacitance of this heatsink are both much larger than those of the MOSFET, so the MOSFET's thermal characteristics can be ignored for now. For this characterization, a TO–220 was attached to the heatsink and forced to dissipate a step input of 7 W. Figure 9 shows how the MOSFET's tab temperature increased in response to its power dissipation.

Table 2. Relationship Between Fundamental Thermal and Electrical Parameters

	Electrical	Thermal
Through Variable	Current (A)	Heat Flow (J/s)
Across Variable	Difference in Voltage	Difference in Temperature
Resistance	Electrical Resistance	Thermal Resistance
Ohm's Law	$\Delta V = I \cdot R$	ΔT=Heat Flow times R
Unit of Capacitance	Coulombs/Volt	Joules/°C

Once the thermal response of a network is known, choosing the number of thermal Rs and Cs to be used in the model and assigning values to each is usually an exercise in compromise. The trick is to maintain simplicity without affecting modeling accuracy. The actual thermal network of the aluminum heatsink used here is a jumble of distributed Rs and Cs, and it is not possible to model it exactly. Fortunately, the model only needs to be accurate enough to give useful and meaningful results.

Since the characteristics of our aluminum heatsink are dominated by its large thermal capacity and its large heatsink to ambient thermal resistance, a single RC network is all that is required. (Ways to model more complex thermal networks will be discussed at the end of this paper.)

Actual characterization data supports using a simple RC network. The simulated tab temperature rise for a 7 W load matches the curve shown in Figure 9. The thermal resistance used in the model was determined from the steady state data and the thermal capacitance was calculated from the thermal resistance and the circuit's thermal time constant, which was about 461 seconds. The chosen value of C was substantiated by estimates using the heatsink's mass and aluminum's specific heat.

By choosing the thermal R from the steady state conditions and the thermal C from the temperature at one tau, the simulation is forced to match the actual heatsink temperature rise at those two times. All other points match well because the assumption that the network can be modeled as a single RC is accurate. Now that the heatsink is modeled and the MOSFET model has been verified, we have all the elements required to model a simple thermal/electrical system.

Constant Current Load

Simulating a simple constant current load turns out to be not only a challenge but an impossible task for most tools for modeling power electronics. It is well known that a MOSFET's $R_{DS(on)}$ can double from 25°C to 175°C. The positive temperature coefficient causes the MOSFET's $R_{DS(on)}$ to increase with temperature, which causes additional power dissipation and an even greater increase in junction temperature. When load current is high or heatsinking is poor, the MOSFET's junction temperature may never stop increasing, resulting in "thermal runaway."

It's difficult to determine the conditions at which thermal runaway will occur because of the feedback inherent in the electrical/thermal network. Near the point of runaway the final junction temperature is especially sensitive to changes in ambient temperature, $R_{DS(on)}$, the temperature coefficient of $R_{DS(on)}$, and the thermal stackup. The simulation must accurately model all these factors or the results may be far from actual behavior.

Figure 10 shows the case temperature rise of an MTP15N06V subjected to two stepped loads, one with the transistor dissipating 7 W and another with the transistor dissipating conduction losses due to a continuous drain current of 6.0 A. Initially the power dissipation for the 6 A load is about 3.6 W, but as junction temperature increases, the power dissipation eventually exceeds 7 W. Because power dissipation gradually increases with time, the system takes much longer to stabilize with the fixed drain current.

The empirically generated curves in Figure 11 clearly show the catastrophic results of increasing the load current from 6.0 to 6.5 A. The system moves from stability to thermal runaway, and the MOSFET would have been destroyed had the test not been stopped.

The conditions of Figure 11 were simulated and are shown in Figure 12. Considering the sensitivity of the network near thermal runaway, the results match those of Figure 11 very well. Note that $V_{DS(on)}$ climbs unabated due to the continuing increase in temperature and $R_{DS(on)}$.

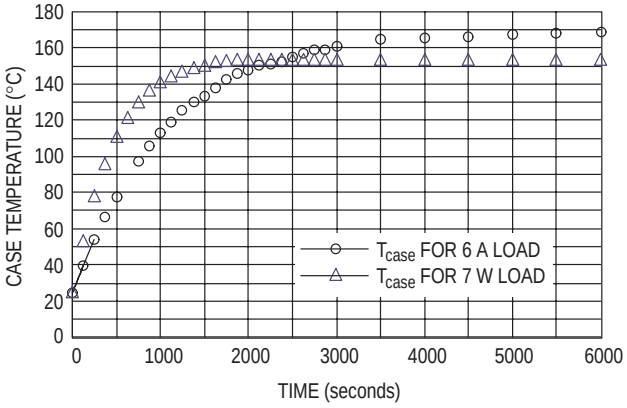


Figure 10. Measured Case Temperature for 7 W and 6 A Loads

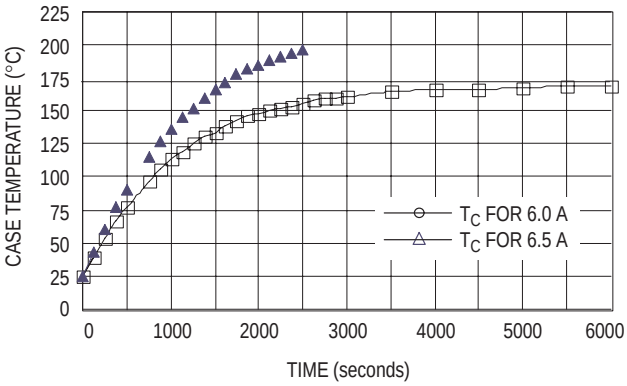


Figure 11. Measured Case Temperature Rise with 6 and 6.5 A Loads

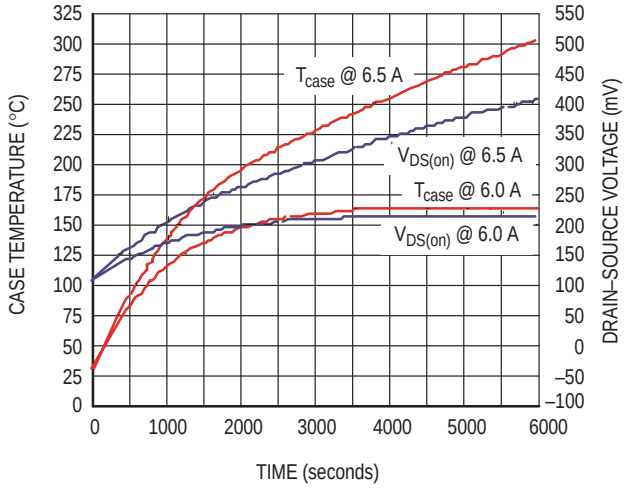


Figure 12. Simulated Case Temperature and $V_{DS(on)}$ with 6.0 and 6.5 A Loads

Characterizing Complex Thermal Networks

So far, the examples of thermal networks shown here have been very simple and therefore limited to a small class of applications. A much broader technique for characterizing thermal environments is needed.

There are at least three ways to obtain models of complex thermal systems. One is to use finite element analysis to determine the thermal response and generate a thermal network that a program like SABER can use. This approach is promising for many circuits, especially those of moderate complexity.

A second approach works with very complex as well as simple thermal networks. With this method a power transistor is mounted to its heatsink and is placed in an environment similar to that of the actual application, which may include several thermal interfaces, forced air cooling, elevated ambient temperature, etc. Next, the thermal response of the system is measured with a well established technique, i.e., transient thermal response testing using the temperature sensitive parameters of the power component. This is how junction–to–case transient thermal response curves are generated for data sheets. The technique is simply extended to include the entire thermal stackup. Thermal Rs and Cs can be determined from the transient thermal response curves.

A transient thermal response curve is shown in Figure 13. The upper waveform is the transient thermal response of the TO–220 on a Wakefield 667–10ABPP heatsink. A thermal network that gives a similar response is shown at the top of the graph. The lower waveform is the transient thermal response of the same TO–220 on an infinite heatsink. This lower curve is the junction–to–case transient thermal response that appears on most power MOSFET data sheets. An equivalent thermal circuit is shown for that case, too.

Unfortunately, measuring transient thermal response requires specialized test equipment that quickly switches the device under test from a powered mode to a test mode. Commercial test circuits are available and schematics for building the circuits have been published (Ref. [1] and [2]).

If the power pulse of interest has a width greater than a few seconds, measuring the tab temperature rise, as was done in the testing in this paper, is an option. There will be an error introduced because of the difference between the tab and the junction temperatures. If the power dissipation is low and if the pulse width exceeds the thermal time constant of the package, then the junction to tab temperature difference will be small and a thermal model can be built from tab temperature readings.

Both response curves shown in Figure 13 can be described with only three RC pairs. Such thermal networks add only a few simple nodes to the netlist and do not appreciably increase simulation time at each timestep. However, thermal time constants tend to be far greater than electrical time constants. Therefore, a combined thermal/electrical simulation make take some time to reach steady state values if the power components are being switched, even at fairly low frequencies. Additional techniques need to be developed for this broad case of applications.

One approach might be to assume that the switching losses are relatively constant with temperature (not a bad assumption with power MOSFETs) and then model only the on–state losses. Estimated switching losses could be injected into the thermal network to include their contribution to the junction temperature rise.

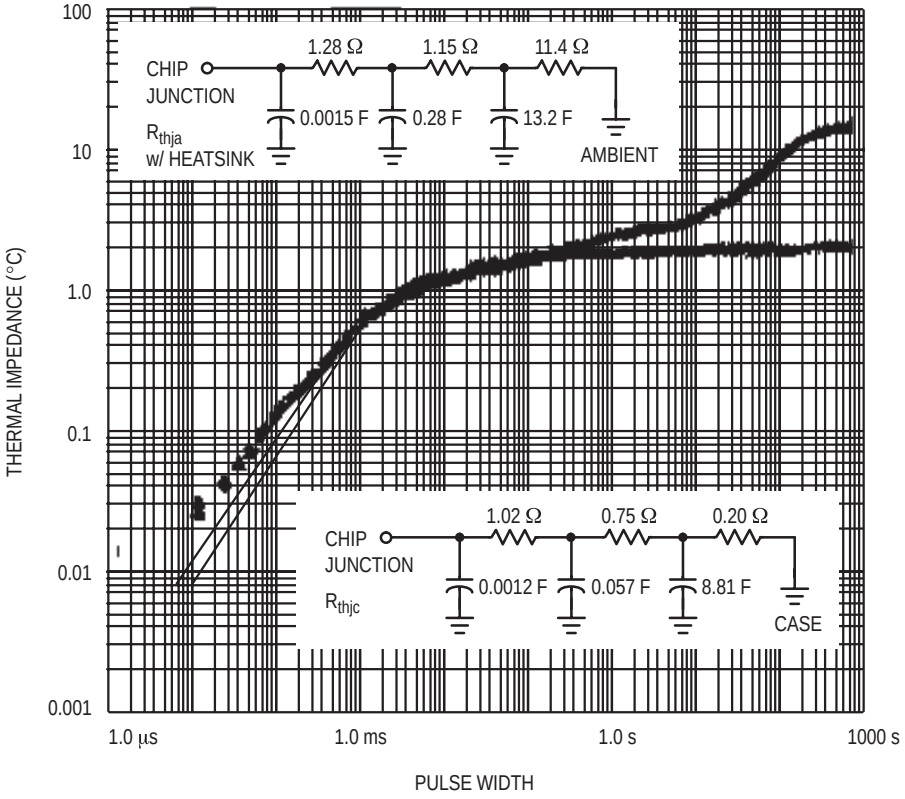


Figure 13. Transient Thermal Response of a MOSFET on a Wakefield Heatsink and an Infinite Heatsink.

REFERENCES

[1] G. Dashney, “Basic Semiconductor Thermal Measurement,” ON Semiconductor Semiconductor Products Sector (602–244 3471).

[2] A. Pshaenich, “Basic Thermal Management of Power Semiconductors,” ON Semiconductor Application Note AN1083.

[3] Brice Shiner, Bill Roehr, “Transient Thermal Resistance — General Data and Its Use,” ON Semiconductor Application Note AN569.

[4] A. Hefner, D Blackburn, “Thermal Component Models for Electrothermal Network Simulation,” IEEE Transactions on Components, Packaging, and Manufacturing Technology — Part A, Vol. 17, No. 3, September 1994.

[5] “Modeling Thermal Networks in Electrical Circuits,” Engineering Note No. 110, Analogy, Inc., Beaverton, OR.

[6] Dr. J. Sophia, “Analysis of Thermal Transient Data with Synthesized Dynamic Models for Semiconductor Devices,” Analysis Tech, Wakefield, MA 01880.

Appendix A Thermal Data on Power Surface Mount Packages

Device Type	Technology	Package	Die Size (mils)	Die Size (mm)	$R_{\theta JA}$ (°C/W)	Notes	$R_{\theta JA}$ (°C/W)
Rectifier	GaAs	D^2PAK	112 x 112	2.84 x 2.84	77.8	Air	3.3
Rectifier	Silicon/Schottky	D^2PAK	114 x 114	2.89 x 2.89	91.38	min	2.19
Rectifier	Silicon/Schottky	D^2PAK	114 x 114	2.89 x 2.89	52.29	1”, SS	
MOSFET	Silicon	D^2PAK	115 x 102	2.92 x 2.59	50	min	1.86
Rectifier	Silicon/Schottky	D^2PAK	128 x 128	3.25 x 3.25	90.19	min	4
Rectifier	Silicon/Schottky	D^2PAK	128 x 128	3.25 x 3.25	59.74	1”, SS	
MOSFET	Silicon	D^2PAK	145 x 145	3.68 x 3.68	50	min	1.29
Rectifier	Silicon/Schottky	D^2PAK	170 x 170	4.31 x 4.31	88.02	min	1.26
Rectifier	Silicon/Schottky	D^2PAK	170 x 170	4.31 x 4.31	54.46	1”, SS	
MOSFET	Silicon	D^2PAK	171 x 227	4.34 x 5.77	76.73	min	0.61
MOSFET	Silicon	D^2PAK	171 x 227	4.34 x 5.77	53.04	1”, SS	
MOSFET	Silicon	D^2PAK	180 x 175	4.57 x 4.44	50	min	1
Rectifier	Silicon/Schottky	D^2PAK	180 x 180	4.57 x 4.57	88.26	min	1.02
Rectifier	Silicon/Schottky	D^2PAK	180 x 180	4.57 x 4.57	56.67	1”, SS	
MOSFET	Silicon	D^2PAK	186 x 190	4.72 x 4.82	50	min	0.93
Rectifier	GaAs	D^2PAK	80 x 80	2.03 x 2.03	76.8	Air	3.77
Rectifier	Silicon/Schottky	DPAK	100 x 100	2.54 x 2.54	134.17	min	112.21
Rectifier	Silicon/Schottky	DPAK	100 x 100	2.54 x 2.54	67.53	1”, SS	2.43
MOSFET	Silicon	DPAK	102 x 102	2.59 x 2.59	118.12	min	1.72
MOSFET	Silicon	DPAK	115 x 102	2.92 x 2.59	71.4	min	1.86
Rectifier	Silicon/Schottky	DPAK	62 x 62	1.57 x 1.57	131.67	min	3.22
Rectifier	Silicon/Schottky	DPAK	62 x 62	1.57 x 1.57	63.95	1”, SS	
MOSFET	Silicon	DPAK	75 x 75	1.91 x 1.91			3.43
Rectifier	Silicon/Schottky	DPAK	80 x 80	2.03 x 2.03	123.34	min	2.5
Rectifier	Silicon/Schottky	DPAK	80 x 80	2.03 x 2.03	62.09	1”, SS	
MOSFET	Silicon	DPAK	89 x 89	2.26 x 2.26	71.4	min	2.38
MOSFET	Silicon	DPAK	89 x 89	2.26 x 2.26	92.29		2.61
MOSFET	Silicon	Micro8™	35 x 70	0.89 x 1.78	239.36	min	21.37
MOSFET	Silicon	Micro8™	35 x 70	0.89 x 1.78	121	1”, SS	26.66
MOSFET	Silicon	Micro8™	70 x 85	1.78 x 2.16	199.24	min	
MOSFET	Silicon	Micro8™	70 x 85	1.78 x 2.16	94.67	1”, SS	
MOSFET	Silicon	Micro8™	70 x 85	1.78 x 2.16	107.67	0.5”, min	
Rectifier	Silicon	Powermite™	40 x 40	1.01 x 1.01	247.2	min	19.5
Rectifier	Silicon/Schottky	Powermite™	40 x 40	1.01 x 1.01	254.9	min	
Rectifier	Silicon/Schottky	Powermite™	40 x 40	1.01 x 1.01	83.1	1”, SS	
Rectifier	Silicon/Schottky	SMA	39 x 39	0.99 x 0.99	243.95	min	
Rectifier	Silicon/Schottky	SMA	39 x 39	0.99 x 0.99	85.74	1”, SS	
Rectifier	Silicon/Schottky	SMA	39 x 39	0.99 x 0.99	250.57	min	
Rectifier	Silicon/Schottky	SMA	39 x 39	0.99 x 0.99	104.47	0.7”, SS	
Rectifier	Silicon/Schottky	SMA	39 x 39	0.99 x 0.99	87.53	1”, SS	

NOTES:
1. Derating applied to all numbers
   $R_{\theta JX} < 20$: #*1.25
   $20 < R_{\theta JX} < 100$ #*(1+)0.25–0.15*((#–20)/80)))
   $R_{\theta JX} > 100$ #*1.1
2. $R_{\theta JA}$ is on min pad unless noted
3. DXPAK $R_{\theta JA}$ is on min pad unless noted

Appendix A Thermal Data on Power Surface Mount Packages

Device Type	Technology	Package	Die Size (mils)	Die Size (mm)	$R_{\theta JA}$ (°C/W)	Notes	$R_{\theta JA}$ (°C/W)
Rectifier	Silicon/Schottky	SMA	45 x 45	1.14 x 1.14	253.76	min	
Rectifier	Silicon/Schottky	SMA	45 x 45	1.14 x 1.14	101.53	0.7”, SS	
Rectifier	Silicon/Schottky	SMA	45 x 45	1.14 x 1.14	86.4	1”, SS	
Rectifier	Silicon/Schottky	SMA	49 x 49	1.24 x 1.24	251.1	min	
Rectifier	Silicon/Schottky	SMA	49 x 49	1.24 x 1.24	86.7	1”, SS	
Rectifier	Silicon	SMA	52 x 52	1.32 x 1.32	88.3	1”, SS	
Rectifier	Silicon	SMA	52 x 52	1.32 x 1.32	240.7	min	
Rectifier	Silicon	SMA	52 x 52	1.32 x 1.32	247.5	min	
Rectifier	Silicon/Schottky	SMA	52 x 52	1.32 x 1.32	250.01	min	
Rectifier	Silicon/Schottky	SMA	52 x 52	1.32 x 1.32	103.97	0.7”, SS	
Rectifier	Silicon/Schottky	SMA	52 x 52	1.32 x 1.32	85.57	1”, SS	
Rectifier	Silicon/Schottky	SMB	39 x 39	0.99 x 0.99	219.07	min	
Rectifier	Silicon/Schottky	SMB	39 x 39	0.99 x 0.99	80.82	1”, SS	
Rectifier	Silicon/Schottky	SMB	39 x 39	0.99 x 0.99	208.1	min	
Rectifier	Silicon/Schottky	SMB	39 x 39	0.99 x 0.99	78.1	1”, SS	
Rectifier	Silicon	SMB	46 x 46	1.16 x 1.16	79.26	1”, SS	
Rectifier	Silicon	SMB	46 x 46	1.16 x 1.16	234.41	min	
Rectifier	Silicon	SMB	60 x 60	1.52 x 1.52	75.44	1”, SS	
Rectifier	Silicon	SMB	60 x 60	1.52 x 1.52	231.63	min	
Rectifier	Silicon/Schottky	SMB	62 x 62	1.57 x 1.57	225.65	min	
Rectifier	Silicon/Schottky	SMB	62 x 62	1.57 x 1.57	77.38	1”, SS	
Rectifier	Silicon/Schottky	SMC	62 x 62	1.57 x 1.57	164	min	
Rectifier	Silicon/Schottky	SMC	62 x 62	1.57 x 1.57	70.7	1”, SS	
Rectifier	Silicon/Schottky	SMC	62 x 62	1.57 x 1.57	71.6	1”, SS	
Rectifier	Silicon/Schottky	SMC	62 x 62	1.57 x 1.57	164.4	min	
Rectifier	Silicon	SMC	71 x 71	1.80 x 1.80	74.7	1”, SS	
MOSFET	Silicon	SO–8	34 x 68	0.86 x 1.73	176.6	min	
MOSFET	Silicon	SO–8	34 x 68	0.86 x 1.73	105.4	1”, SS	
MOSFET	Silicon	SO–8	34 x 68	0.86 x 1.73	66.33	1”, 10S	
BIPOLAR	Silicon	SO–8	51 x 54	1.3 x 1.37	186.6	min	
BIPOLAR	Silicon	SO–8	51 x 54	1.3 x 1.37	126.3	0.7”, SS	
BIPOLAR	Silicon	SO–8	51 x 54	1.3 x 1.37	108.4	1”, SS	
BIPOLAR	Silicon	SO–8	56 x 84	1.42 x 2.13	185.7	min	
BIPOLAR	Silicon	SO–8	56 x 84	1.42 x 2.13	116.2	0.7”, SS	
BIPOLAR	Silicon	SO–8	56 x 84	1.42 x 2.13	99.6	1”, SS	
MOSFET	Silicon	SO–8	57 x 99	1.45 x 2.51	166.1	min	
MOSFET	Silicon	SO–8	57 x 99	1.45 x 2.51	97.8	1”, SS	
MOSFET	Silicon	SO–8	57 x 99	1.45 x 2.51	61.7	1”, 10S	
MOSFET	Silicon	SO–8	57 x 99	1.45 x 2.51	85.6	1”, SS	
MOSFET	Silicon	SO–8	57 x 99	1.45 x 2.51	49.33	1”, 10S	
MOSFET	Silicon	SO–8	58 x 99	1.47 x 2.51	160.8	min	
MOSFET	Silicon	SO–8	89 x 150	2.26 x 3.81	145.13	min	
Rectifier	Silicon/Schottky	SO–8	90 x 90	2.29 x 2.29	138.5	min	

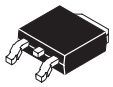
NOTES:
1. Derating applied to all numbers
   $R_{\theta JX}$ < 20: #*1.25
   20 < $R_{\theta JX}$ < 100 #*(1+)0.25–0.15*((#–20)/80)))
   $R_{\theta JX}$ > 100 #*1.1
2. $R_{\theta JA}$ is on min pad unless noted
3. DXPAK $R_{\theta JA}$ is on min pad unless noted

Appendix A Thermal Data on Power Surface Mount Packages

Device Type	Technology	Package	Die Size (mils)	Die Size (mm)	$R_{\theta JA}$ (°C/W)	Notes	$R_{\theta JA}$ (°C/W)
MOSFET	Silicon	SO–8	98 x 120	2.49 x 3.04	133.2	min	
MOSFET	Silicon	SO–8	98 x 120	2.49 x 3.04	81.5	1”, SS	
MOSFET	Silicon	SO–8	98 x 120	2.49 x 3.04	129	min	
MOSFET	Silicon	SO–8	98 x 120	2.49 x 3.04	80.9	1”, SS	
MOSFET	Silicon	SO–8	98 x 120	2.49 x 3.04	44.5	1”, 10S	
Rectifier	Silicon/Schottky	SOD–123	35 x 35	0.89 x 0.89	205.7	1”, SS	
Rectifier	Silicon/Schottky	SOD–123	35 x 35	0.89 x 0.89	429.2	min	
MOSFET	Silicon	SOT–223	35 x 70	0.89 x 1.78	167.49	min	
MOSFET	Silicon	SOT–223	35 x 70	0.89 x 1.78	75.49	1”, SS	
MOSFET	Silicon	SOT–223	55 x 90	1.40 x 2.29	159.8	min	
MOSFET	Silicon	SOT–223	55 x 90	1.40 x 2.29	88.5	0.7”, SS	
MOSFET	Silicon	SOT–223	55 x 90	1.40 x 2.29	71.8	1”, SS	

NOTES:
1. Derating applied to all numbers
   $R_{\theta JX}$ < 20: #*1.25
   20 < $R_{\theta JX}$ < 100 #*(1+)0.25–0.15*((#–20)/80)))
   $R_{\theta JX}$ > 100 #*1.1
2. $R_{\theta JA}$ is on min pad unless noted
3. DXPAK $R_{\theta JA}$ is on min pad unless noted

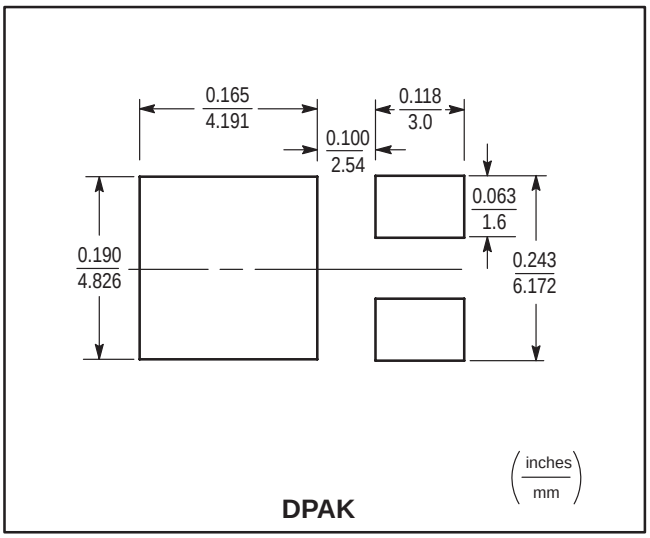
Thermal Comparison and Summary of Low Voltage Surface Mount Packages

Time in Seconds	Minimum Pad Size (°C/W)	Minimum Pad Size (watts)	0.5" Sq. Pad Size (°C/W)	0.5" Sq. Pad Size (watts)	1" Sq. Pad Size (°C/W)	1" Sq. Pad Size (watts)	Die Size (mils)	Die Size (mm)	Packages
5	24.5	5.10	—	—	15	8.33	100x100	2.54x2.54	 DPAK
10	38.5	3.25	—	—	21	5.95			
SS	134	0.93	—	—	67.5	1.85			
5	55	2.27	—	—	30	4.17	35x70	0.889x1.77	 SOT–223
10	75	1.67	—	—	35	3.57			
SS	167	0.75	—	—	75.94	1.65			
5	50.5	2.48	44	2.84	37.5	3.33	96x120	2.438x3.04	 SO–8
10	64	1.95	51.5	2.43	44	2.84			
SS	128.9	0.97	102	1.23	80.9	1.55			
5	97.5	1.28	52	2.40	46	2.72	70x85	1.77x2.159	 Micro8
10	122	1.02	56	2.23	51	2.45			
SS	199	0.63	107.6	1.16	94.7	1.32			
5	137	0.91	62	2.02	58.3	2.14	40x70	1.016x1.77	 TSOP–6
10	160	0.78	68.3	1.83	61.5	2.03			
SS	241	0.52	125.8	0.99	102.3	1.22			

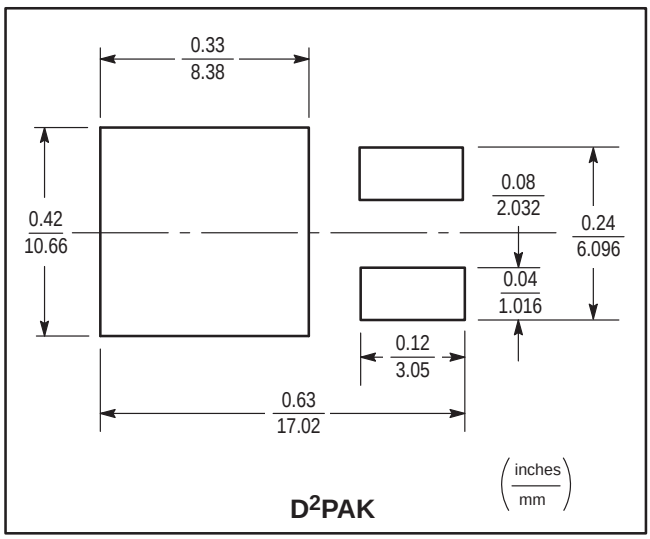
NOTES: These apply to all of the measurements
SS = Steady State
Thermal measurements are $R_{\theta JA}$ in °C/Watt
Measurements have been derated
All devices are single die

Appendix B Footprints for Soldering

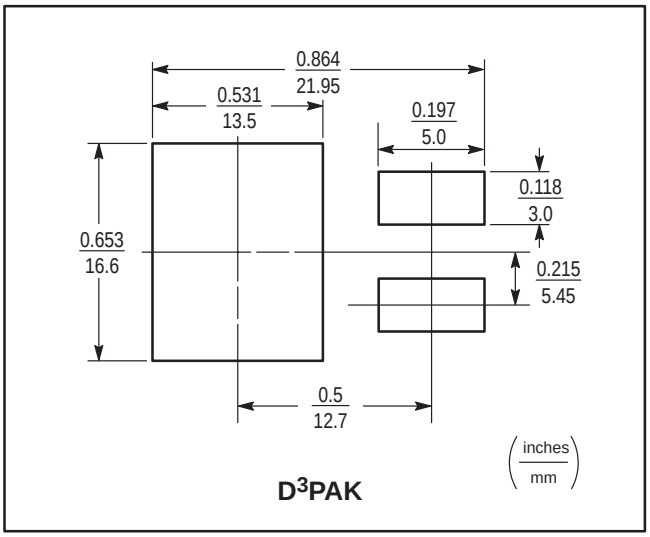
Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry the packages will self align when subjected to a solder reflow process.



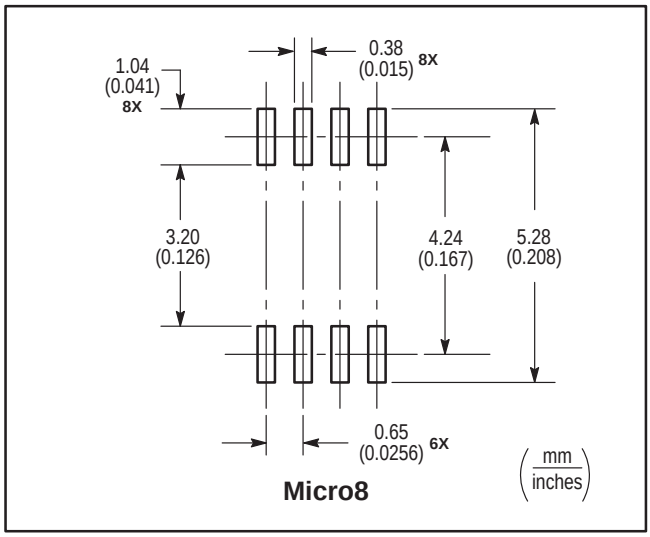
DPAK



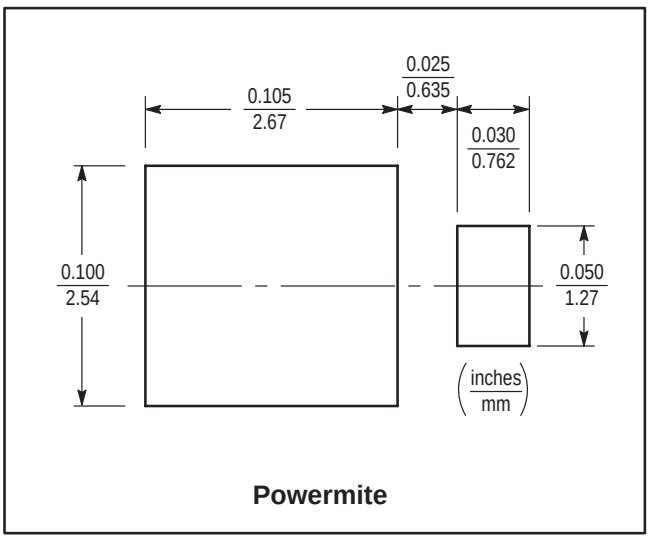
D²PAK



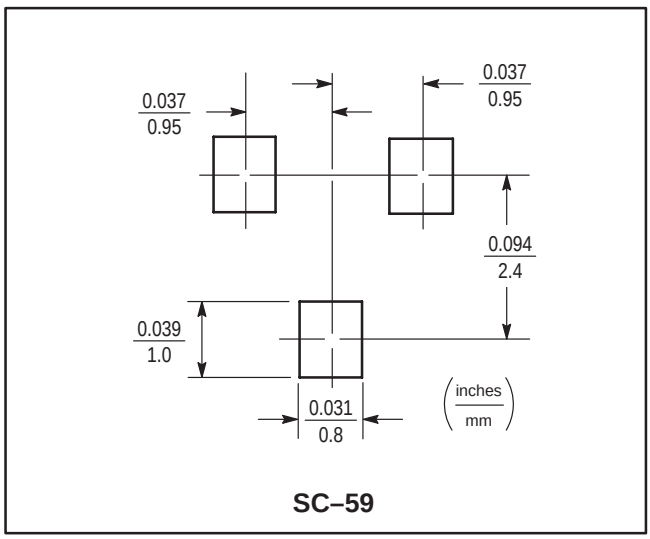
D³PAK



Micro8

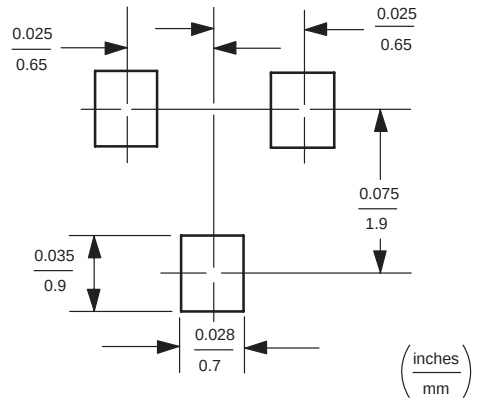


Powermite

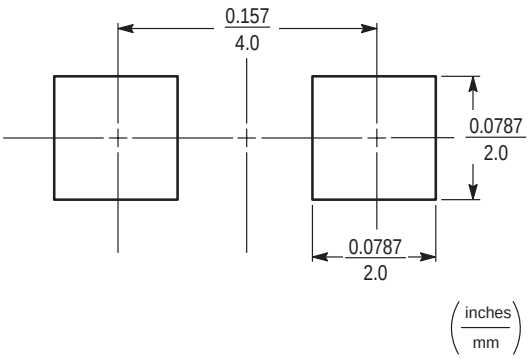


SC–59

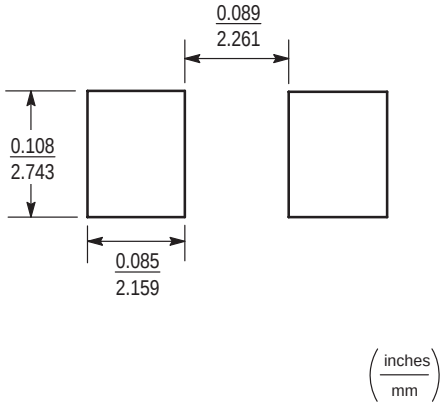
Appendix B Footprints for Soldering (continued)



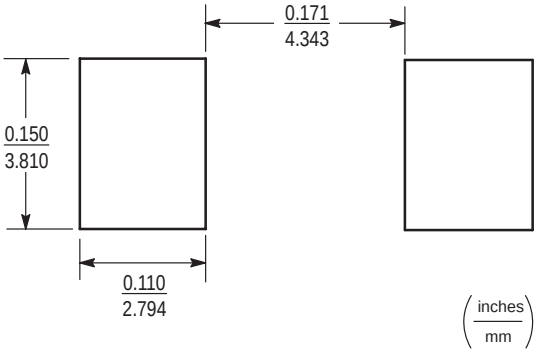
SC–70/SOT–323



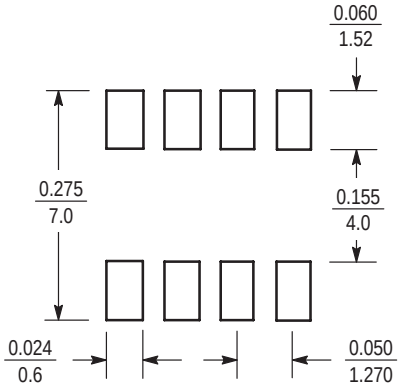
SMA



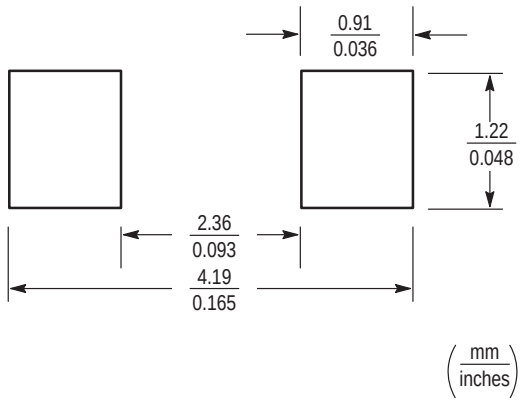
SMB



SMC

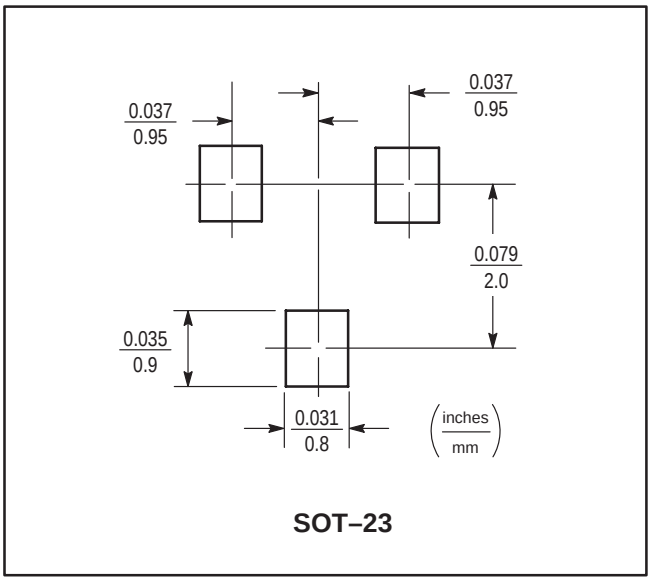


SO–8

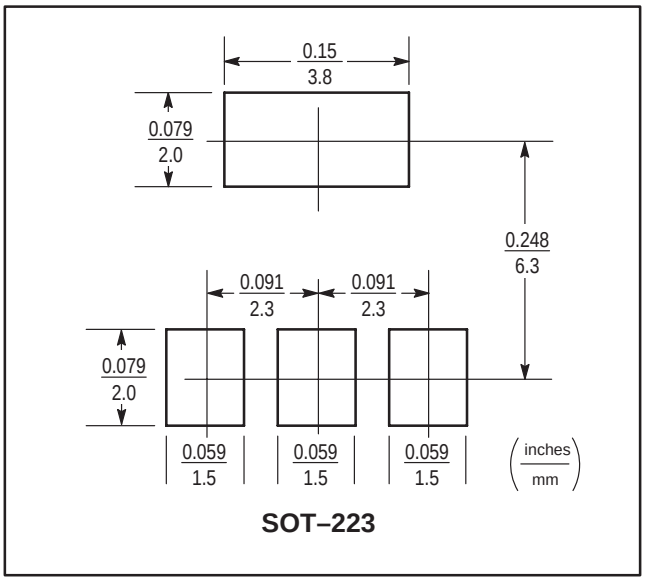


SOD–123

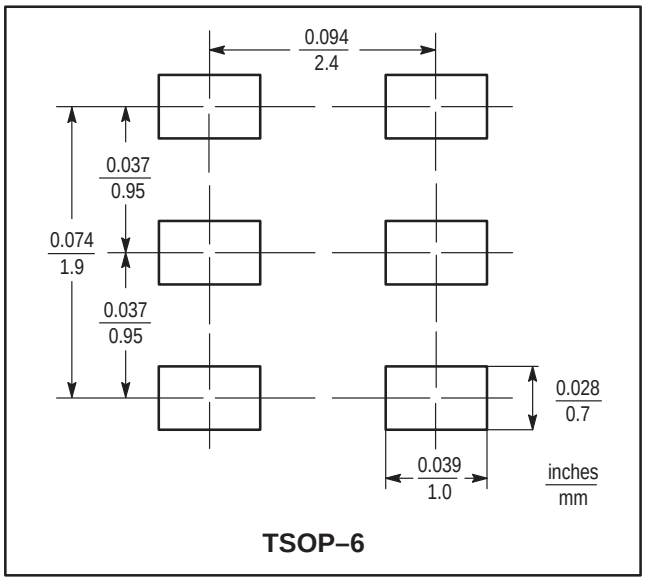
Appendix B Footprints for Soldering (continued)



SOT–23



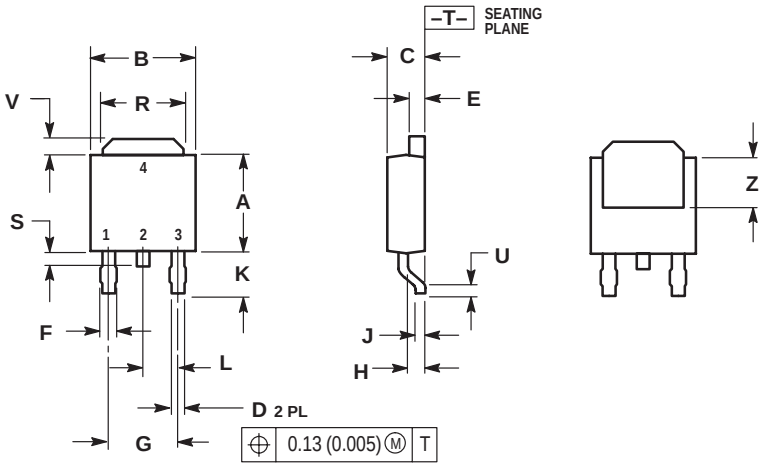
SOT–223



TSOP–6

Appendix C Package Outline Drawings

DPAK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	—	0.51	—
V	0.030	0.050	0.77	1.27
Z	0.138	—	3.51	—

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

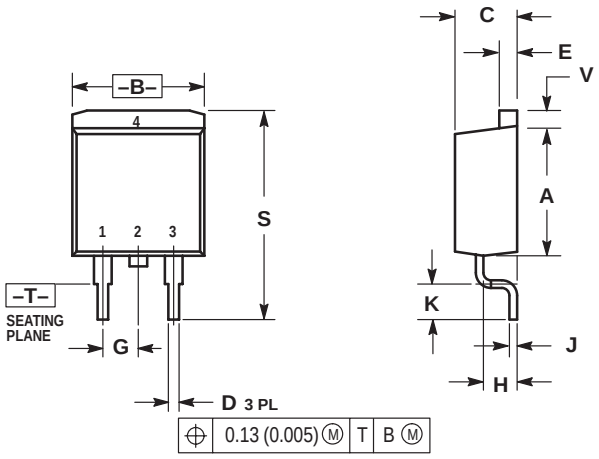
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

CASE 369A–13
ISSUE Z

D²PAK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

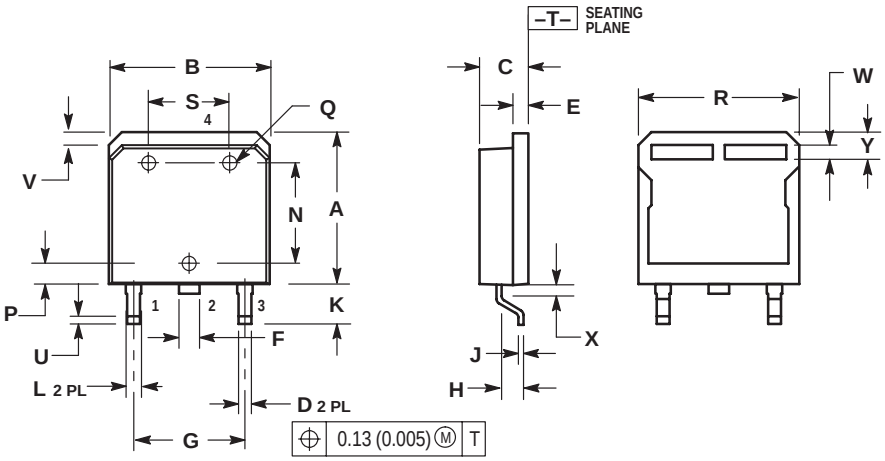
STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

CASE 418B–03
ISSUE C

Appendix C Package Outline Drawings (continued)

D^{3}PAK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

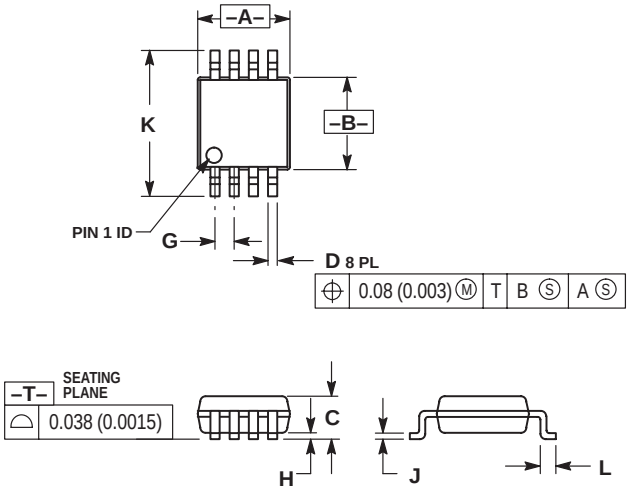
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.588	0.592	14.94	15.04
B	0.623	0.627	15.82	15.93
C	0.196	0.200	4.98	5.08
D	0.048	0.052	1.22	1.32
E	0.058	0.062	1.47	1.57
F	0.078	0.082	1.98	2.08
G	0.430 BSC		10.92 BSC	
H	0.105	0.110	2.67	2.79
J	0.018	0.022	0.46	0.56
K	0.150	0.160	3.81	4.06
L	0.058	0.062	1.47	1.57
N	0.353	0.357	8.97	9.07
P	0.078	0.082	1.98	2.08
Q	0.053	0.057	1.35	1.45
R	0.623	0.627	15.82	15.93
S	0.313	0.317	7.95	8.05
U	0.028	0.032	0.71	0.81
V	0.050	—	1.27	—
W	0.054	0.058	1.37	1.47
X	0.050	0.060	1.27	1.52
Y	0.104	0.108	2.64	2.74

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 433–01
ISSUE C

Micro8



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	—	1.10	—	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

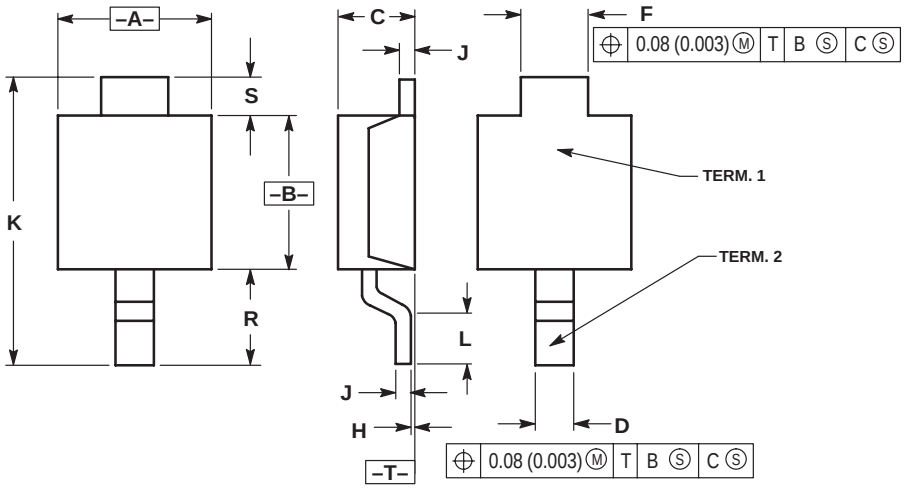
STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N–SOURCE
2. N–GATE
3. P–SOURCE
4. P–GATE
5. P–DRAIN
6. P–DRAIN
7. N–DRAIN
8. N–DRAIN

CASE 846A–02
ISSUE D

Appendix C Package Outline Drawings (continued)

Powermite

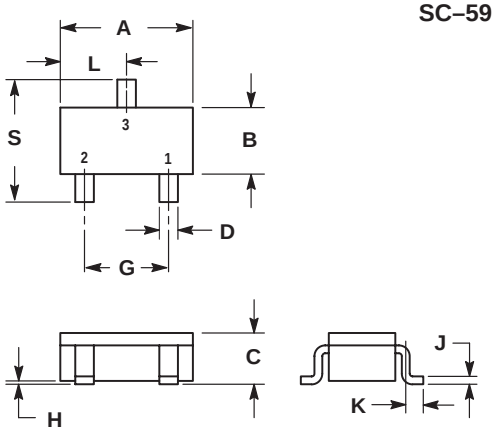


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.75	2.05	0.069	0.081
B	1.75	2.18	0.069	0.086
C	0.85	1.15	0.033	0.045
D	0.40	0.69	0.016	0.027
F	0.70	1.00	0.028	0.039
H	–0.05	+0.10	–0.002	+0.004
J	0.10	0.25	0.004	0.010
K	3.60	3.90	0.142	0.154
L	0.50	0.80	0.020	0.031
R	1.20	1.50	0.047	0.059
S	0.50 REF		0.019 REF	

CASE 457–04
ISSUE C

SC–59



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.70	3.10	0.1063	0.1220
B	1.30	1.70	0.0512	0.0669
C	1.00	1.30	0.0394	0.0511
D	0.35	0.50	0.0138	0.0196
G	1.70	2.10	0.0670	0.0826
H	0.013	0.100	0.0005	0.0040
J	0.09	0.18	0.0034	0.0070
K	0.20	0.60	0.0079	0.0236
L	1.25	1.65	0.0493	0.0649
S	2.50	3.00	0.0985	0.1181

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. N.C.
2. ANODE
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. N.C.
2. CATHODE
3. ANODE

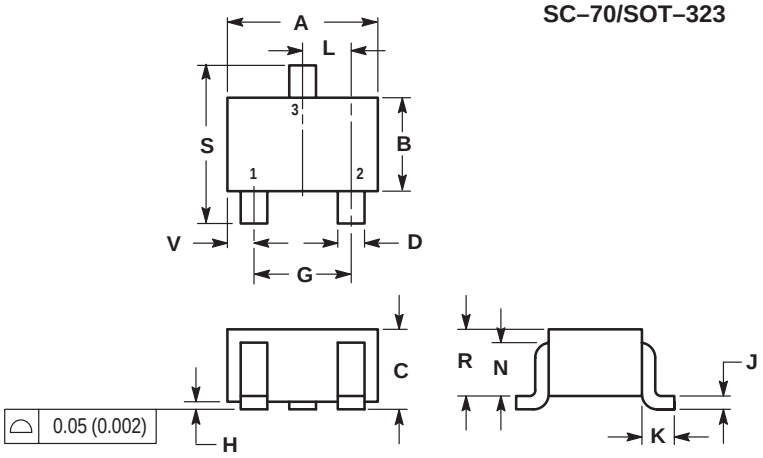
STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. ANODE/CATHODE

CASE 318D–04
ISSUE F

Appendix C Package Outline Drawings (continued)

SC–70/SOT–323



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.035	0.049	0.90	1.25
D	0.012	0.016	0.30	0.40
G	0.047	0.055	1.20	1.40
H	0.000	0.004	0.00	0.10
J	0.004	0.010	0.10	0.25
K	0.017 REF		0.425 REF	
L	0.026 BSC		0.650 BSC	
N	0.028 REF		0.700 REF	
R	0.031	0.039	0.80	1.00
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

STYLE 1:
CANCELLED

STYLE 2:
PIN 1. ANODE
2. N.C.
3. CATHODE

STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 6:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 7:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

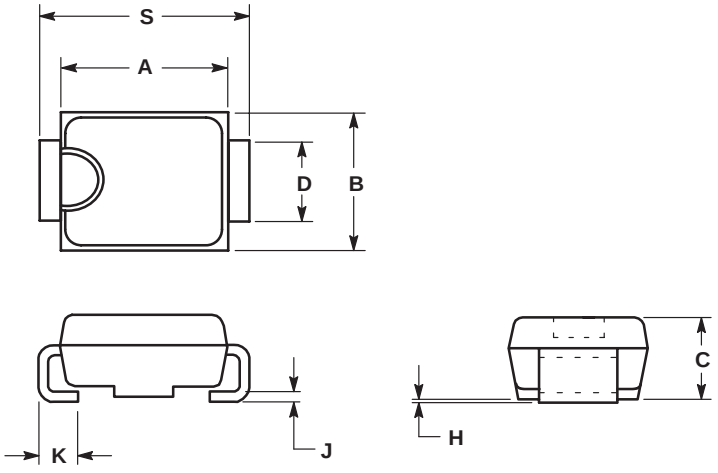
STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. CATHODE–ANODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. ANODE–CATHODE

CASE 419–02
ISSUE J

SMA



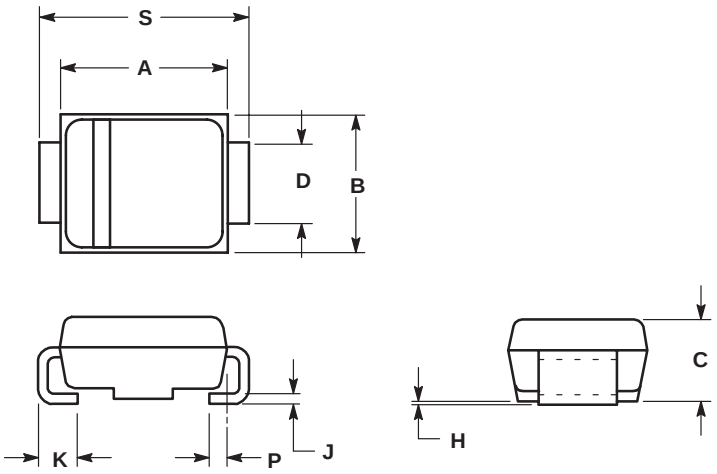
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.160	0.180	4.06	4.57
B	0.090	0.115	2.29	2.92
C	0.075	0.105	1.91	2.67
D	0.050	0.064	1.27	1.63
H	0.004	0.008	0.10	0.20
J	0.006	0.016	0.15	0.41
K	0.030	0.060	0.76	1.52
S	0.190	0.220	4.83	5.59

CASE 403B–01
ISSUE O

Appendix C Package Outline Drawings (continued)

SMB

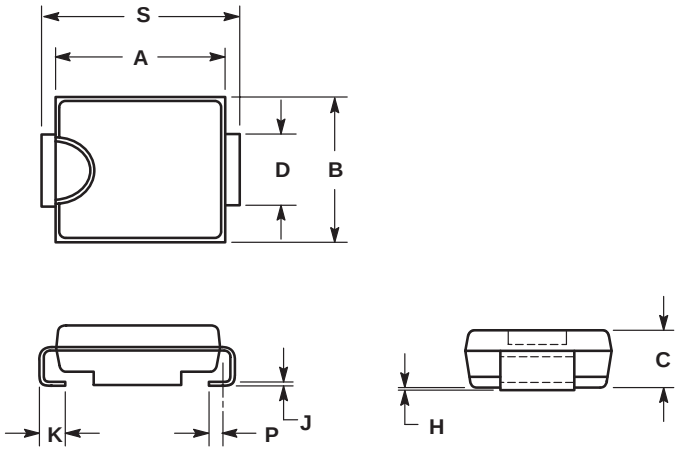


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. D DIMENSION SHALL BE MEASURED WITHIN DIMENSION P.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.160	0.180	4.06	4.57
B	0.130	0.150	3.30	3.81
C	0.075	0.095	1.90	2.41
D	0.077	0.083	1.96	2.11
H	0.0020	0.0060	0.051	0.152
J	0.006	0.012	0.15	0.30
K	0.030	0.050	0.76	1.27
P	0.020 REF		0.51 REF	
S	0.205	0.220	5.21	5.59

CASE 403A–03
ISSUE D

SMC



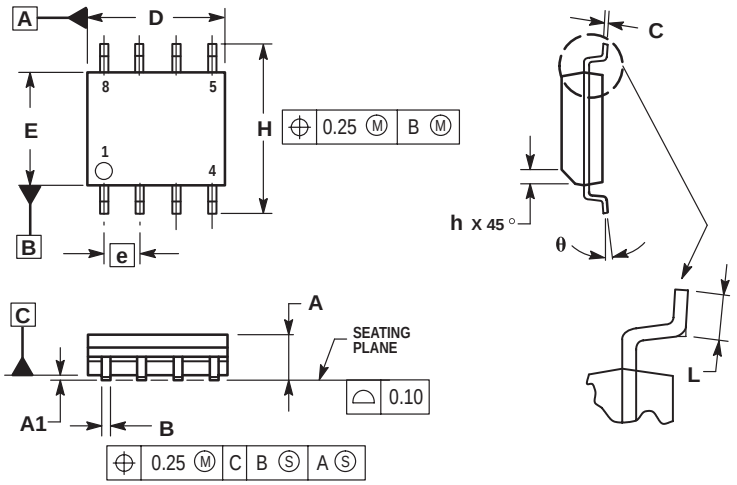
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. D DIMENSION SHALL BE MEASURED WITHIN DIMENSION P.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.260	0.280	6.60	7.11
B	0.220	0.240	5.59	6.10
C	0.075	0.095	1.90	2.41
D	0.115	0.121	2.92	3.07
H	0.0020	0.0060	0.051	0.152
J	0.006	0.012	0.15	0.30
K	0.030	0.050	0.76	1.27
P	0.020 REF		0.51 REF	
S	0.305	0.320	7.75	8.13

CASE 403–03
ISSUE B

Appendix C Package Outline Drawings (continued)

SO–8



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0 °	7 °

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N–SOURCE
2. N–GATE
3. P–SOURCE
4. P–GATE
5. P–DRAIN
6. P–DRAIN
7. N–DRAIN
8. N–DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

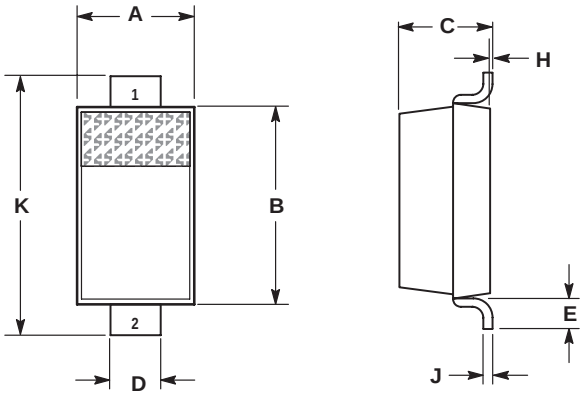
STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

CASE 751–06
ISSUE T

Appendix C Package Outline Drawings (continued)

SOD–123



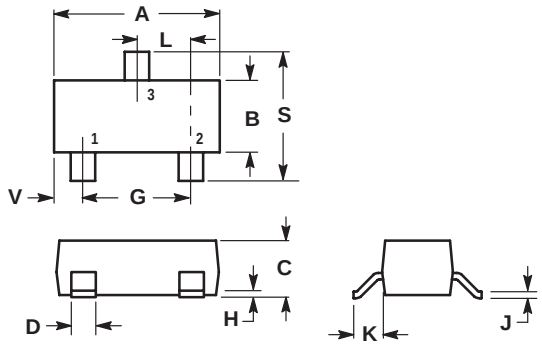
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.055	0.071	1.40	1.80
B	0.100	0.112	2.55	2.85
C	0.037	0.053	0.95	1.35
D	0.020	0.028	0.50	0.70
E	0.004	—	0.25	—
H	0.000	0.004	0.00	0.10
J	—	0.006	—	0.15
K	0.140	0.152	3.55	3.85

STYLE 1:
PIN 1. CATHODE
2. ANODE

CASE 425–04
ISSUE C

SOT–23



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE–ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE–ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

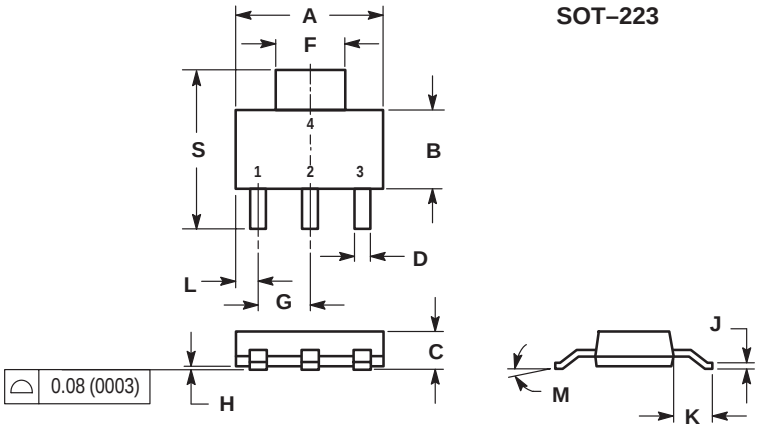
STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

CASE 318–08
ISSUE AF

Appendix C Package Outline Drawings (continued)

SOT–223



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 °	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

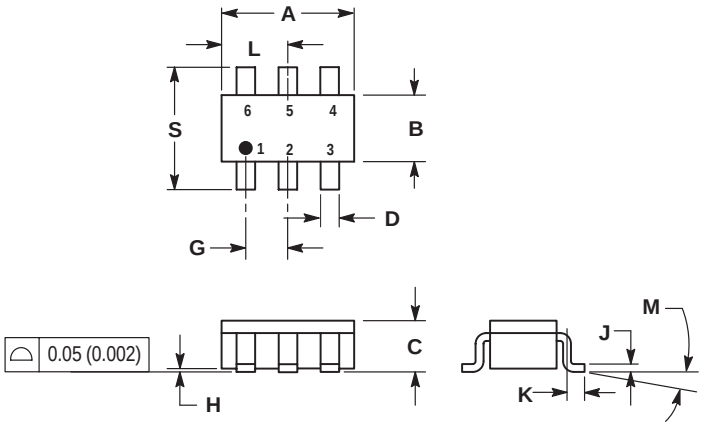
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

CASE 318E–04
ISSUE J

TSOP 6



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

CASE 318G–02
ISSUE D

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