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A 50W, 500kHz, Full-Bridge, Phase-Shift, ZVS Isolated DC to DC Converter Using the HIP4081A

Author: David J. Hamo

Introduction

Many articles and papers have been published recently promoting the performance and benefits of the Phase-Shift, Full-Bridge Topology and rightly so. This topology productively utilizes the same elements that have been plaguing power supply designers for decades, those infamous parasitic components. The topology enables designers to advantageously employ transformer leakage inductance, MOSFET output capacitance and the MOSFET body diode, enabling designers to easily move their designs upwards in frequency. The topology offers additional advantages like zero-voltage-switching at a constant switching frequency, which substantially reduces switching losses. This can be significant enough to eliminate heatsinking of power MOSFETS and/or enabling the use of less expensive power devices. Reduced EMI and RFI are additional benefits, since the voltage and current switching waveforms are much “cleaner” and waveform edges switch softly compared to conventional pulse width modulation (PWM) techniques. The ability to move upwards in frequency will ultimately reduce the overall size and lower the cost of the supply. One megahertz operation and beyond is possible with this topology. This is truly a major advancement in topological architecture. The requirements for this design are a full bridge configuration, an additional inductor to aid resonant operation and output structure consisting of a dual diode rectifier and an LC filter. Special thermal substrates may not be required. As a result, cost savings can be realized by utilizing inexpensive FR4 printed circuit board material in place of elaborate thermal designs. What’s more, EMI/RFI filtering requirements and heatsinking are less rigorous further reducing costs. Therefore, focusing on the overall system cost, it can be demonstrated that employing this topology does have merit.

Presently, there are limited phase-shift controllers on the market, and those that are available are still expensive. Having faced this problem, an investigation of designing a discrete solution was performed. What was discovered proved to be encouraging. With any low cost single ended controller and two low cost logic ICs, one can generate all the gating and delay functions necessary to derive the phase-shift control waveforms. What makes this all possible is the Intersil HIP4081A MOSFET driver. The HIP4081A is capable of independently driving four MOSFETs directly, eliminating the need for traditional drive transformers. The HIP4081A also allows additional drive and control capabilities unavailable with conventional gate drive transformers. This includes the ability to vary the turn-on delays of both upper and lower MOSFET switches. This is an essential feature for realizing zero voltage switching (ZVS). The net result is flexibility and capacity to derive the control logic drive signals necessary for phase-shift ZVS switching. The voltage rating of the HIP4081A is 80V, which is ideal for telecom DC to DC converters. With the added overvoltage protection circuit which turns on the lower MOSFETS and turns off the upper MOSFETS, further protection is supplied to the system. The block diagram of the full-bridge phase-shift power supply described in this application note is shown in Figure 1. The circuit discussed here has an output power capability of 50W, but operation can be scaled upwards to the 500W range with the appropriate power component changes.

HIP4081A Features

The HIP4081A is a member of the HIP408X family of high frequency H-Bridge driver ICs. The HIP4081A H-Bridge driver has the ability to operate from 8 to 80VDC for driving N-channel MOSFET H-Bridges. The HIP4081A is packaged in both 20 Lead DIP and 20 Lead SOIC, provide peak gate current drive of 2.5A and can switch up to 1MHz. A combination of bootstrap and charge-pumping techniques is used to power the circuitry which drives the upper halves of the H-Bridge. The bootstrap technique supplies high instantaneous current needed for turning on the power devices, while the charge pump provides enough current to “maintain” bias voltage on the upper driver sections and MOSFETs. Since voltages on the upper bias supply pin “float” along with the source terminals of the upper power switches, the design of this family provides voltage capability for the upper bias supply terminals of 95VDC. Two resistors tied to pins HDEL and LDEL can provide precise delay matching of upper and lower propagation delays. The programmable delay range for this device is 10ns to 100ns. This variable delay capability is imperative for zero voltage switching and will be described shortly.

Phase-Shift Control Overview

Due to the number of well written papers on the theory and concepts of phase-shift ZVS conversion, we will limit the discussion to the implementation of the technology. Several papers are listed in the reference section that address phase-shift ZVS conversion topics further.

The full bridge drive control logic required for this topology is not conceptually complex. Figure 2 shows the full bridge with

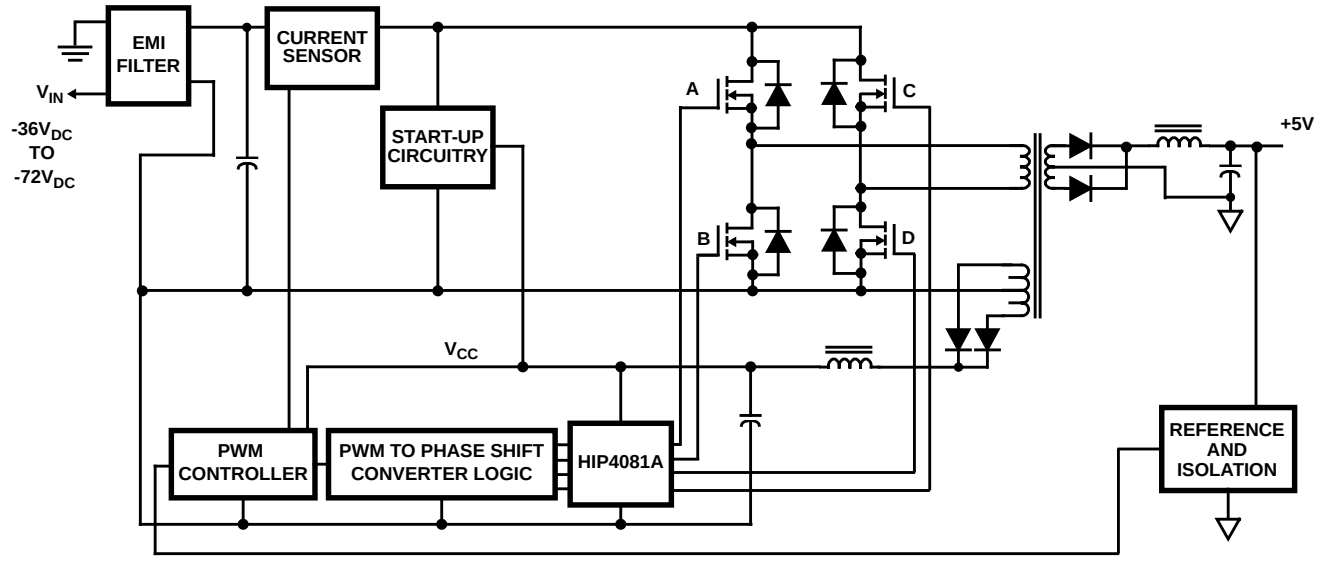

FIGURE 1. FULL-BRIDGE, PHASE-SHIFT POWER SUPPLY BLOCK DIAGRAM

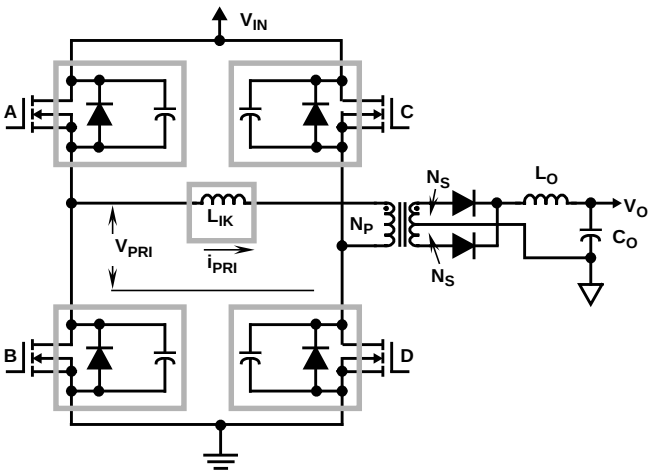

FIGURE 2.

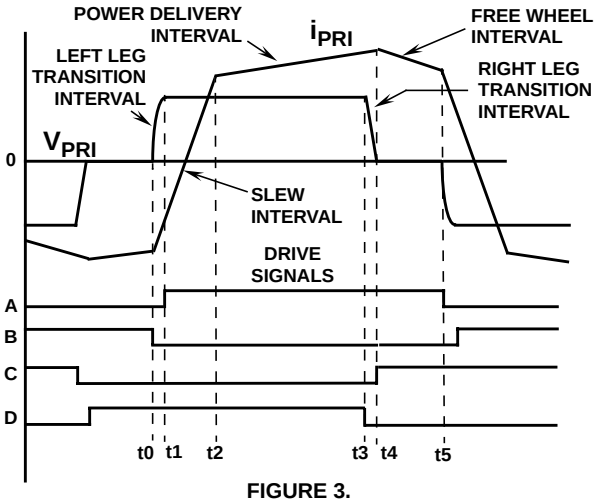

FIGURE 3.

associated parasitic components essential for ZVS operation. Figure 3 shows the waveforms associated with the circuit of Figure 2. During phase-shift ZVS operation there are five states or intervals of time, that take place per half cycle of operation. These states will be briefly discussed and only one half cycle of the bridge will be described due to the circuits symmetric operation. Refer to Figure 3 during the following descriptions and time interval identifications.

Slew Interval (t0-t2)

The slew interval is the time it takes for the primary current to reverse directions. This time is established by the level of input voltage across the primary, load current and the total inductance in the primary path, referred to as the resonant inductance. This inductance includes the leakage inductance of the transformer and any additional inductance in the primary path. Additional inductance may be required to store enough energy to displace the capacitive charge on C_{OSS} and to provide realistic transition delay times. The term resonant inductance will refer to the combination of transformer leakage inductance and any additional inductance in the primary path.

Power Delivery Interval (t2-t4)

The gate drive signals and timing diagram associated with the full bridge are shown in Figure 4. The power delivery interval of the phase shift topology is similar to the traditional full bridge converter, in that two diagonal switches are on (A&D or B&C). This applies the full input voltage across the primary and results in power transfer to the load. The amount of time these switches are on is directly proportional to the phase shift between the two sets of waveforms AB and CD. The phase between these sets of waveforms will change as required, to regulate the output voltage. A 100% phase shift will result in 100% duty cycle. Conversely, a 0% phase shift will result in 0% duty cycle.

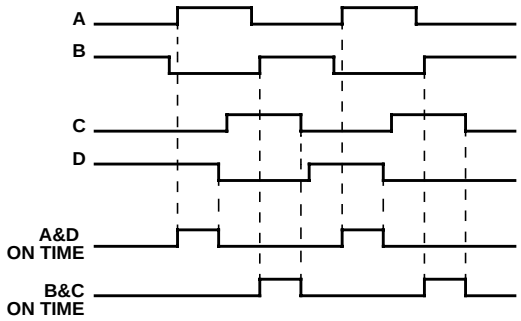

FIGURE 4

Freewheel Interval (t4-t5)

Notice the following from Figure 3. There is a time when A&C switches will conduct simultaneously and B&D switches will conduct simultaneously. This state is called the “freewheel” interval. This is how the phase-shift controller can perform control without changing the frequency, unlike other quasi-resonant topologies. As the load requirements change, the freewheel time changes accordingly. The freewheel time increases with light loads and decreases with heavy loads. In other words, the freewheel time is a way for the controller to idle until the next appropriate state comes along. During the freewheel time, reflected load current is circulated through the FET switches A&C or B&D and the voltage across the primary is zero. Figure 3 shows the droop in primary current during this time. This is caused by conduction losses in the circulation path and output inductor ripple current.

Transition Intervals (ZVS Delay)

Left Leg Transition Interval (t0- t1)

The method for ZVS involves the displacement of charge in the drain-to-source capacitances of the MOSFETs and occurs differently for the two legs of the bridge. The left leg (A&B) transition interval begins after the freewheel state to initiate the power delivery interval. This is the time required to displace the charge on the output capacitance of the A&B leg. For the left leg, the source of energy that displaces this charge is stored in the transformer’s leakage inductance plus any additional inductance in the primary path (the total being the resonant inductance). The displacement of this charge forces the voltage across MOSFET A to zero (MOSFET B ZVS occurs during the cycles second half), enabling zero voltage switching to take place. Here the MOSFETs output capacitances form a resonant circuit with the resonant inductance. The charge is displaced in a time equal to one-fourth the resonant period. As a result, the left leg transition time is given by:

$$t_{LL} = \frac{\pi}{2} \times \sqrt{L_R C_R} \qquad \text{(EQ. 1)}$$

t_{LL} = Transition time for the left leg interval

L_R = Transformer leakage inductance + additional inductance

C_R = Resonant capacitance

The resonant capacitance is given by:

$$C_R = \frac{4}{3} \times C_{OSS} + C_{XFMR} \qquad \text{(EQ. 2)}$$

C_{OSS} = MOSFET output capacitance

C_{XFMR} = Transformer capacitance

The MOSFET output capacitance C_{OSS} is multiplied by 4/3 to approximate the average capacitance value during a varying drain-to-source voltage. The derivation of this equation is listed in appendix A.

Right Leg Transition Interval(t3- t4)

The second ZVS delay is called the right leg (C&D) transition time which terminates the power delivery interval. This is the time required to displace the charge on the output capacitance of the C&D leg. The converters output inductor current is reflected to the primary and therefore is the source of energy which will displace this charge. The displacement of this charge forces the voltage across MOSFET C to zero (MOSFET D ZVS occurs during the cycles second half), enabling zero voltage switching to take place. In this case however, the mechanism for displacement of charge is not resonant, but linear since this transition is modelled by a current source of reflected output current driving the output capacitance. The time is given by:

$$t_{RL} = \frac{C_R \times V_{IN}}{I_P} \qquad \text{(EQ. 3)}$$

V_{IN} = Voltage applied to full bridge

I_P = Peak primary current

C_R = Resonant capacitance

t_{RL} = Transition time for the right leg interval

Both energy sources required to displace the charge on the drain-to-source capacitances of the MOSFETs are load dependant. This makes it difficult to maintain zero-voltage-switching at light loads. However, this fact does not pose a serious problem as described later in the section titled ZVS Design Considerations.

Phase-Shift Drive Derivation

Deriving the phase-shift drive control logic from a standard off-the-shelf PWM controller is straight forward. The controller chosen is the Unitrode UC3823A. This was chosen for its high speed operation and low start-up current. However, any low-cost, high-speed controller could be used. Figure 5 shows the logic circuit used to derive the phase-shift control logic. The timing diagram for this circuit is shown in Figure 6. Notice that the clock output from the UC3823A is shown only for reference purposes. The clock signal is not used in the circuit, however, many of the following equations will include the clock period t_{CLK} in their composition. The clock period t_{CLK} is 2µs.

The PWM output from the controller clocks the flip-flop which outputs waveforms at its Q and $\overline{Q}$ outputs, which become a&b. At the same time the PWM logic signal is exclusive ORed with the Q and $\overline{Q}$ outputs of the flip-flop. This generates the c&d waveforms as shown in the timing diagram. Normally “slivers” are developed on the c&d waveforms. They come about from the time delay caused by the PWM clock signal propagation time through the flip-flop. Using advanced CMOS logic the maximum sliver width will be approximately 15ns. While it is possible to generate sliverless waveforms with additional circuitry, this does not present a problem since small capacitors filter the slivers as

shown in Figure 5. The Q and $\overline{Q}$ signals are passed through an XOR gate which is configured as a non-inverting buffer and become a&b. This is to match the timing of the a&b drive outputs with the c&d drive outputs. These signals are then input into the HIP4081A which in turn drives the MOSFET H-Bridge. The A&B drive signals drive the Left-Leg of the bridge while the C&D drive signals drive the Right-Leg of the bridge.

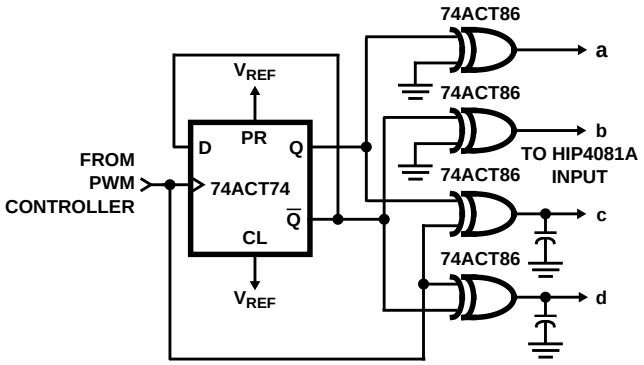

FIGURE 5.

The flip-flop and XOR gates receive their power from the controllers V_{REF} terminal of the UC3823A, which outputs +5V. The power requirements for the logic devices are well within the reference output current capabilities. However, the reference should be properly by-passed.

The ZVS timing delays are determined by Equation 1 and Equation 3. Once the requirements are known the HIP4081A turn on delay times can be set accordingly by the resistor values on the HDEL and LDEL pins. Normally, the left leg and right leg would like to be controlled independently. With the HIP4081A the upper and lower device delay times are controlled independently. This causes a requirement that both delay times be identical. Typically the left leg delay is slightly longer than the right leg delay. In this case the HDEL and LDEL are set to the longer of the two. This concept will be explained further in the section titled ZVS Design Considerations.

The Design Process

Now that the proper control signals for the phase-shift topology have been realized its time to begin working through the design of the power supply of Figures 7A and 7B.

To begin, the overall power supply requirements have been defined by:

Input Voltage = -36V to -72V

Output Voltage = +5V

Output Current = 10A

Switching Frequency = 500kHz

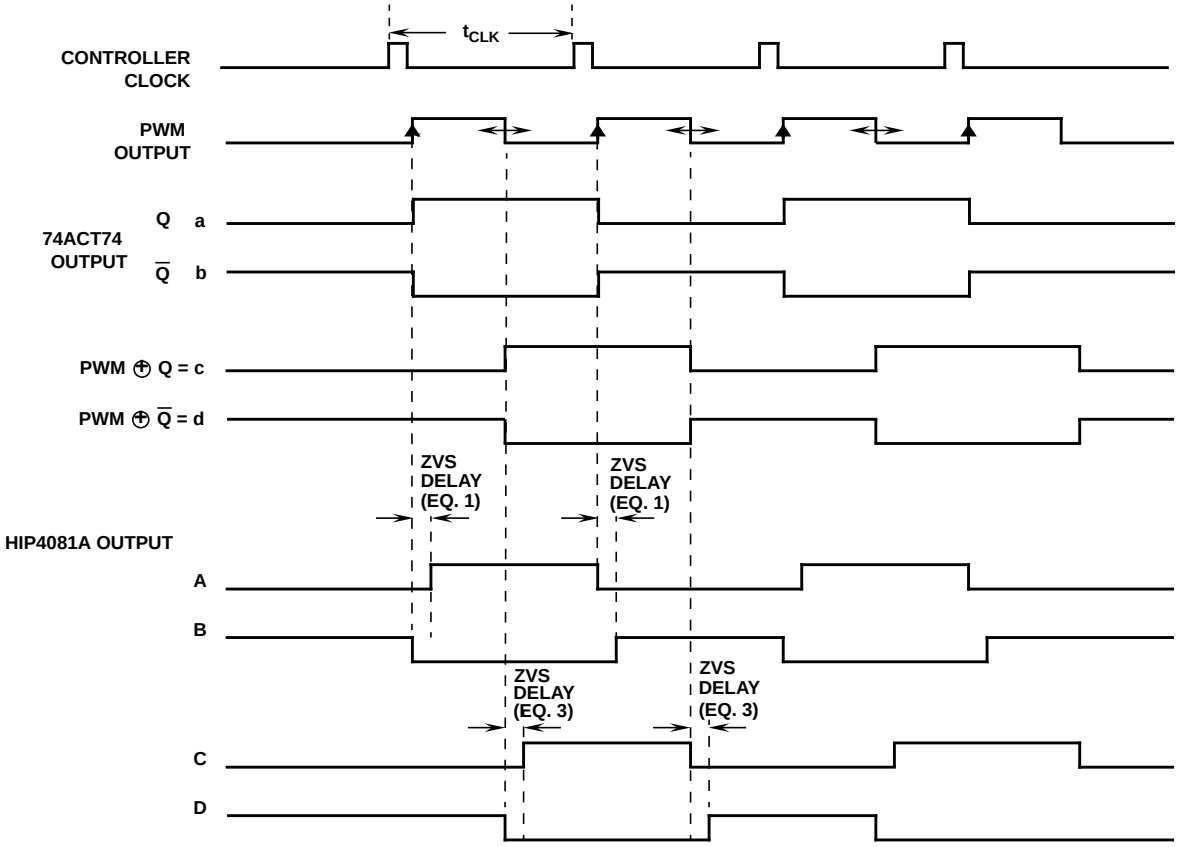

FIGURE 6. PHASE SHIFT TIMING DIAGRAM

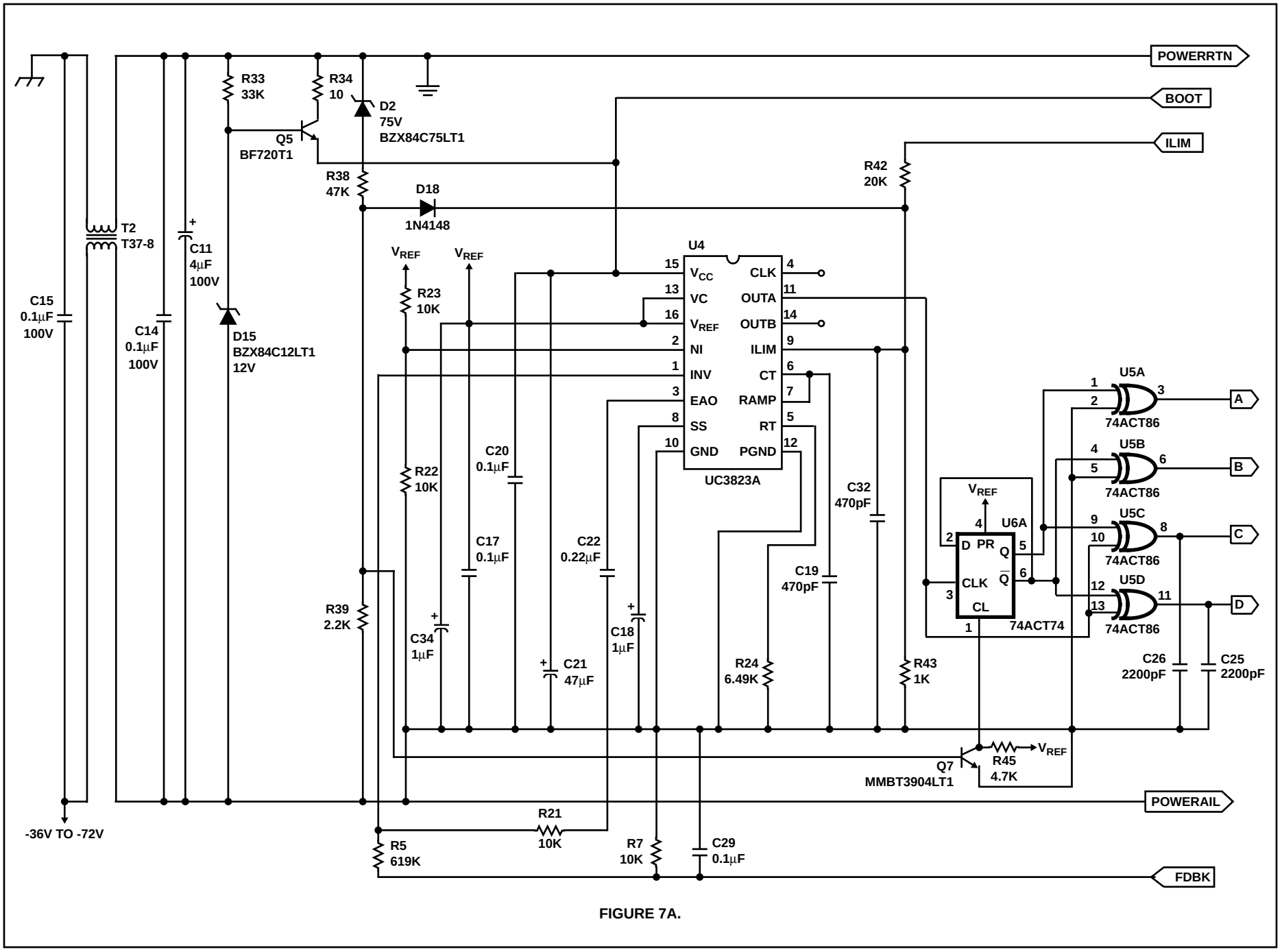
POWERRTN
BOOT
ILIM
R33
33K
R34
10
D2
75V
BZX84C75LT1
Q5
BF720T1
R38
47K
D18
1N4148
R42
20K
T2
T37-8
C11
4µF
100V
C15
0.1µF
100V
C14
0.1µF
100V
D15
BZX84C12LT1
12V
U4
VCC
VC
VREF
NI
INV
EAO
SS
GND
CLK
OUTA
OUTB
ILIM
CT
RAMP
RT
PGND
UC3823A
R23
10K
R22
10K
C20
0.1µF
C17
0.1µF
C22
0.22µF
C18
1µF
C34
1µF
C21
47µF
C32
470pF
C19
470pF
R39
2.2K
R24
6.49K
R43
1K
U6A
74ACT74
U5A
U5B
U5C
U5D
74ACT86
A
B
C
D
C26
2200pF
C25
2200pF
Q7
MMBT3904LT1
R45
4.7K
-36V TO -72V
POWERAIL
R21
10K
R5
619K
R7
10K
C29
0.1µF
FDBK

FIGURE 7A.

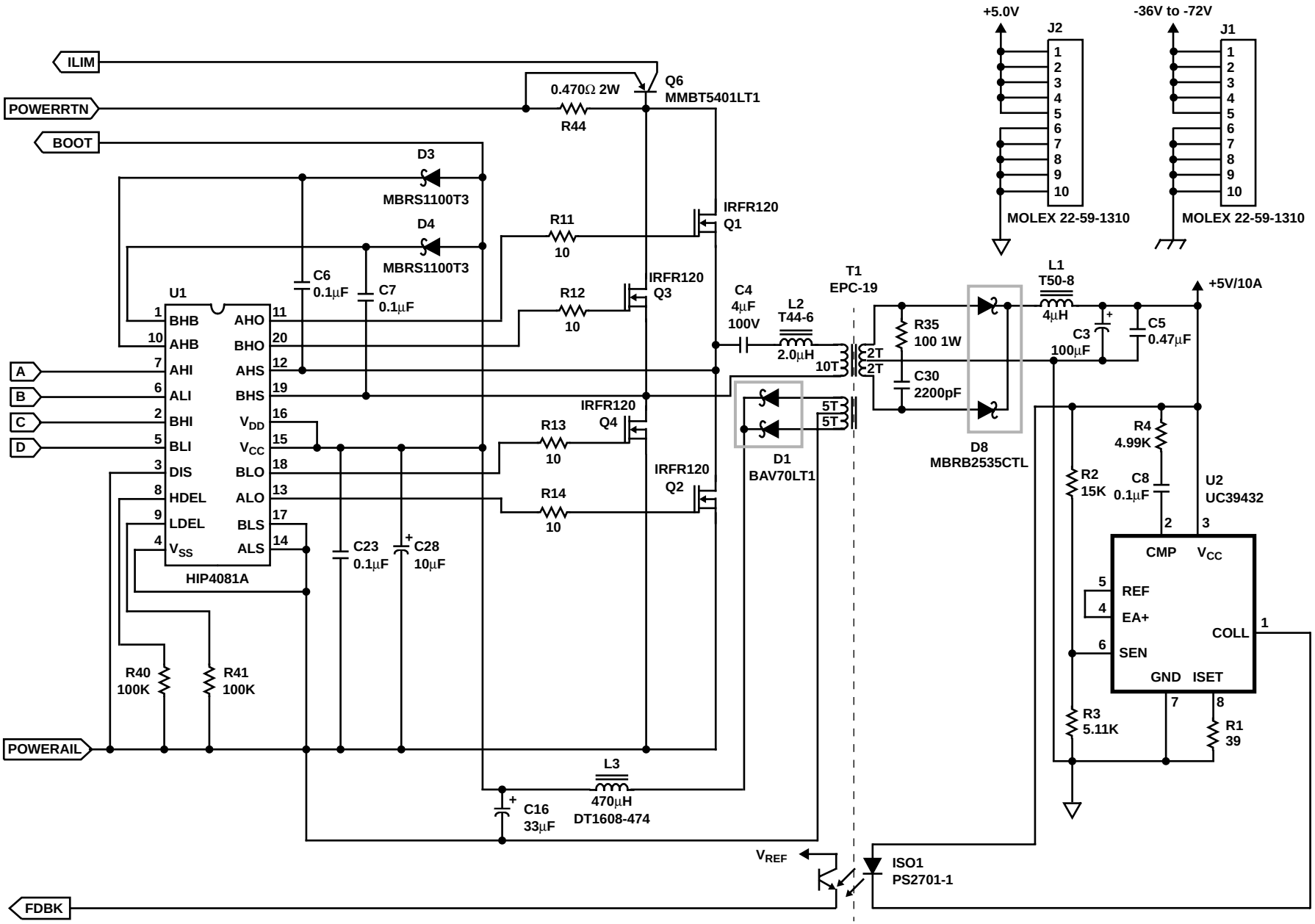
ILIM
POWERRTN
BOOT
A
B
C
D
FDBK
POWERAIL
U1
HIP4081A
BHB
AHB
AHI
ALI
BHI
BLI
DIS
HDEL
LDEL
VSS
AHO
BHO
AHS
BHS
VDD
VCC
BLO
ALO
BLS
ALS
0.470Ω 2W
R44
Q6
MMBT5401LT1
D3
MBRS1100T3
D4
MBRS1100T3
C6
0.1µF
C7
0.1µF
R11
10
R12
10
R13
10
R14
10
IRFR120
Q1
IRFR120
Q3
IRFR120
Q4
IRFR120
Q2
C23
0.1µF
C28
10µF
R40
100K
R41
100K
L3
470µH
DT1608-474
C16
33µF
C4
4µF
100V
L2
T44-6
2.0µH
T1
EPC-19
10T
2T
2T
5T
5T
D1
BAV70LT1
R35
100 1W
C30
2200pF
D8
MBRB2535CTL
L1
T50-6
4µH
C3
100µF
C5
0.47µF
+5V/10A
+5.0V
-36V to -72V
J2
J1
MOLEX 22-59-1310
MOLEX 22-59-1310
R4
4.99K
R2
15K
C8
0.1µF
U2
UC39432
CMP
VCC
REF
EA+
SEN
COLL
GND
ISET
R3
5.11K
R1
39
VREF
ISO1
PS2701-1

FIGURE 7B.

Power Semiconductor Selection

One of the overall goals of this supply is to maintain the lowest profile and size possible. This is important to module manufacturers, as well as board level OEMs. We selected a form factor close to the standard 3" x 3", along with a minimum profile. The voltage and current requirements along with size constraints has lead to the choice of four Intersil IRFR120s for the full-bridge switches. They have a r_{DSON} of 0.27Ω, a breakdown voltage of 100V and are available in the surface mount TO-261(D-PAK)™ package. The output rectifier diode chosen is the Motorola MBRB2535CTL available in a (D^2-PAK)™. This rectifier was chosen because of its very low forward voltage drop, slightly over 0.3V at 10A. This is a important consideration since most of the power loss is in the output rectifier.

Transformer Design

Maintaining the form factor requirements mentioned earlier has lead to the choice of an EPC-19 ferrite core from TDK. In this application the transformer size is limited by core loss. The transformer will be designed for a temperature rise of 50^oC. That coupled with a maximum ambient temperature of 50^oC, the transformer can reach a maximum temperature of 100^oC. PC40 material was chosen since it has a curie temperature in excess of 215^oC, and low core loss at the switching frequency. Design curves given with the core material (TDK catalog #BAE-030D) show temperature rise for a given core loss. The design curves indicate that the core temperature will rise 50^oC with the core dissipating 800mW. This value is for core loss only and excludes any copper losses. If the core losses and copper losses were equally distributed in the transformer the core loss will be 400mW. Therefore, we can determine the maximum core loss limitation for this design:

$$P_{CLOSS} = \frac{P_{CORE}}{V_e} \quad \text{(EQ. 4)}$$

$$P_{CLOSS} = \frac{400mW}{1.047cm^3} = 382\frac{mW}{cm^3}$$

Using the curves once again for the PC40 material, the core loss vs flux density curves indicate that the peak flux density for a core loss of 382 mW/cm^3 is approximately 1200 gauss. The switching frequency is 500kHz but with the full-bridge topology the core flux swings at half the switching frequency. Therefore the transformer switching frequency will be 250kHz while operating in the first and third quadrants of its hysteresis curve. The remaining transformer design procedure is now straight forward.

From Faraday's Law:

$$N_P = \frac{E \times \Delta t \times 10^8}{Ae \times \Delta B} \quad \text{(EQ. 5)}$$

Where E = voltage across the transformer windings (Volts)

N_P = number of primary turns

A_e = Iron area of the core (cm^2)

ΔB = Core flux density (Gauss)

Δt = time in which the flux is changed

For an EPC-19 transformer operating at 250kHz, a 25^oC rise will occur operating with a peak flux density of 1200G. If we let the maximum primary duty cycle reach 80% the maximum on time will be 0.8t, then the maximum flux density change within the time span of 0.8t/2 will be ΔB = 2400G. The voltage across the transformer has been reduced by 2V due to an anticipated voltage drop caused by the two MOSFET switches $r_{DS(ON)}$. The minimum primary turns from Equation 5 is:

$$N_P = \frac{36 - 2 \times \left(\frac{0.8 \times 4 \times 10^{-6}}{2}\right) \times 10^8}{0.227 \times 2400} \geq 10Turns$$

Now in the most ideal case:

$$V_O = V_{IN} \times \frac{N_S}{N_P} \times D$$

For the non-ideal case:

$$V_O = \left((V_{IN} - V_{MOSDROP}) \times \frac{N_S}{N_P} - V_{RECT} \right) \times D$$

Rearranging and solving for the secondary turns ratio:

$$N_S = \left(\frac{\frac{V_O}{D} + V_{RECT}}{V_{IN} - V_{MOSDROP}} \right) \times N_P \quad \text{(EQ. 6)}$$

$$N_S = \left(\frac{5}{\frac{0.8}{36 - 2}} + 0.3 \right) \times 10 = 2Turns$$

The transformer turns ratio has been designed to yield a given flux density excursion, thereby maintaining the limits of temperature range. Next, the wire size must be determined and the copper losses must not exceed 400mW to limit the rise in core temperature to 50^oC. For the primary windings a current density of 500 circular mils per RMS ampere was used. For the secondary a current density of approximately 200 circular mils per RMS ampere was used because of the higher current and the fact that there are only two windings per side required for the secondary. Using these current densities, wire size requirements become 20AWG for the primary and 19AWG for the secondary. For the secondary, eight strands of 28AWG magnet wire will be used, yielding an equivalent circular mil area of 19AWG. With wire selected, the copper loss including skin effects and increased wire resistance at 100^oC, approach 300mW. Therefore we can expect a maximum temperature rise of slightly less than 50^oC. The transformer was wound by interleaving the secondary halves between the primary. The first half of the secondary will be wound first and the primary will be wound next. The remaining secondary half will be wound and finally, the auxiliary will be wound.

ZVS Design Considerations

Now that the transformer has been designed it is a good time to determine the ZVS transition times. This will allow the turn on delays to be set properly for zero-voltage-switch-

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ing to take place. However, choosing the left leg transition time requires much thought because this time is a function of many variables. Therefore, before going any further some concepts need to be clarified and an equation will be derived that will allow this value to be chosen quickly and correctly.

In Figure 8, primary bridge voltage, primary current and secondary voltage waveforms are shown. Notice that the primary and secondary duty cycles are different. From these waveforms the following relationship can be determined:

$$\Delta D = D - D_e \quad \text{(EQ. 7)}$$

ΔD = Loss of duty cycle on the secondary side.

D = Primary voltage duty cycle.

D_e = Secondary voltage duty cycle or effective duty cycle.

The loss of duty cycle on the secondary side is a key concept. This loss is caused by the time it takes to change the direction of the primary current (t2-t1). Therefore it is imperative that the resonant inductance value not be excessive. Otherwise, this might require a larger turns ratio, since the primary duty cycle could reach its maximum value while the secondary duty cycle is incapable of sustaining the appropriate output voltage. This concept could be a stumbling block for the unsuspecting. This leads to the importance of deriving an equation for L_R in terms of this loss of duty cycle ΔD which enables L_R to be bounded properly. This in turn, will lead to the correct value chosen for the left leg transition t_{LL}.

Deriving an equation for ΔD:

Let t2-t1 equal the time it takes for the primary current to slew. Since we know the slope of the sluing primary current, the following equation can be determined from Figure 8.

$$t2 - t1 = \frac{\frac{N_S}{N_P} \times I_{LOAD}}{\frac{V_i}{L_R}}$$

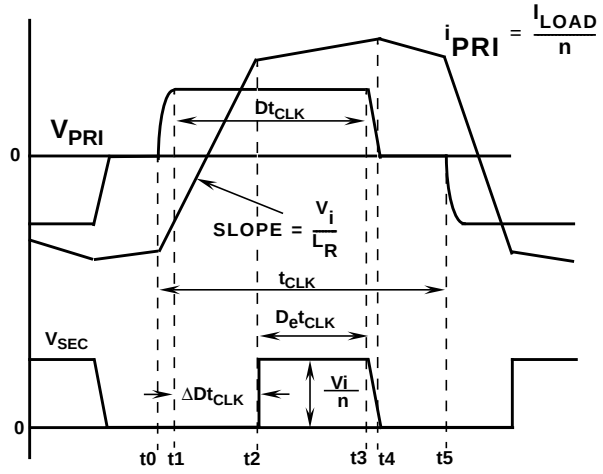

FIGURE 8.

Rearranging:

$$t2 - t1 = \frac{N_S \times L_R \times I_{LOAD}}{N_P \times V_i}$$

From Figure 8:

$$\Delta D \times t_{CLK} = t_2 - t_1$$

Performing the substitution and multiplying by two since there are two such transitions per period, the loss of duty cycle on the secondary is then equal to:

$$\Delta D = \frac{2 \times N_S \times L_R \times I_{LOAD}}{t_{CLK} \times N_P \times V_i}$$

Solving for L_R:

$$L_R = \frac{\Delta D \times t_{CLK} \times V_i \times N_P}{2 \times I_{LOAD} \times N_S} \quad \text{(EQ. 8)}$$

We now have an expression for the total resonant inductance in terms of loss of duty cycle so that its value can be easily determined. From the beginning of the design the maximum secondary duty cycle has been chosen to be 80%. Using this value and selecting a duty cycle loss of 15%, will yield a maximum primary duty cycle of 95%. The leakage inductance of the transformer is approximately 500nH and the total resonant inductance calculation becomes:

$$L_R = \frac{0.15 \times 2 \times 10^{-6} \times (36 - 2) \times 10}{2 \times 10 \times 2} = 2.55\mu H$$

$$L_{RINDUCTOR} = 2.05\mu H - 0.5\mu H = 2.05\mu H$$

Before determining the left leg transition time the resonant capacitance must be calculated. The IRFR120 MOSFET switches have a C_{OSS} capacitance equal to 130pF and the transformer primary capacitance is approximately equal to 10pF. Using Equation 2 the resonant capacitance is calculated:

$$C_R = \frac{4}{3} \times 130 \times 10^{-12} + 10^{-12} = 183pF$$

The left leg transition is then calculated using Equation1:

$$t_{LL} = \frac{\pi}{2} \times \sqrt{2.55 \times 10^{-6} \times 183 \times 10^{-12}}$$

$$t_{LL} = 34ns$$

In the previous calculation an alternative expression for t_{LL} could have been used:

$$t_{LL} = \frac{\pi}{2} \times \sqrt{\frac{\Delta D \times t_{CLK} \times V_i \times C_R \times N_P}{2 \times I_{LOAD} \times N_S}} \quad \text{(EQ. 9)}$$

So making the left leg transition 34ns will cause the maximum primary duty cycle to be approximately 95% at full load with the minimum input voltage applied. This allows 5% margin for variations in C_R and L_R, assuming nearly 100% duty cycle is possible. These numbers can be adjusted easily by the previous equations for your particular needs.

Now that the resonant inductor and left leg transition time have been selected, the right leg transition time needs to be determined. It turns out that the maximum right leg transition time occurs during the maximum input voltage and at a load boundary called the ZVS operational limit. The ZVS operational limit is the point at which the power supply no longer maintains zero-voltage-switching. This is a normal function of this topology. As mentioned earlier, the two energy sources (resonant inductance and output inductance) required to dis-

place the charge on the drain-to-source capacitances of the MOSFETs are load dependant. Therefore at some load value less than maximum, the energy stored in these sources will be less than adequate to displace this charge. This is the point at which the converter will no longer operate in the ZVS mode. This is best exemplified by Figure 9. Figures 9 A, B and C show how the left leg transition is formed. Figure 9A shows that the energy in L_R is larger than the energy required to displace the capacitance charge. Figure 9B shows the ZVS operational limit where the energy in L_R is equal to the energy required to displace the capacitance charge. Figure 9C shows the energy in L_R is not capable of fully displacing the capacitance charge. The same scenario is true for the right leg transitions but they will ramp at a linear rate and their energy source is the output inductance as stated earlier.

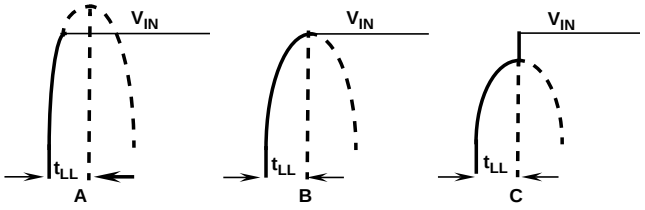

FIGURE 9.

It is more important to maintain ZVS at higher loads for two reasons. The first and more obvious is that the switching losses are greatly reduced. The second reason is because the free-wheel time is at a minimum during full load. Therefore the circulation of the reflected load current during the free-wheel time is shortened thereby reducing the I^2R losses in the free-wheel circulation path. During lighter loads the power dissipation in the MOSFET switches should not be significant if switching losses begin to manifest due to the smaller primary currents during lighter load values. For this reason, the design goal was to maintain ZVS operation down to half the maximum output power (25W). It should be noted that at higher converter power levels (>200W) it may be necessary to place saturable inductors in series with the anode leads of the output rectifier. This extends the range of zero-voltage-switching to very low power levels further improving efficiency. This concept is discussed in great detail in several of the listed references.

The equation which determines the minimum current required for ZVS operation is:

$$I_{PRI}(critical) = \sqrt{\frac{2 \times C_R \times V_{OSS}^{\frac{1}{2}} \times V_{IN(MAX)}^{\frac{3}{2}}}{L_R}} \quad \text{(EQ. 10)}$$

$$I_{PRI}(critical) = \sqrt{\frac{2 \times 183 \times 10^{-12} \times 25^{\frac{1}{2}} \times 72^{\frac{3}{2}}}{2.55 \times 10^{-6}}} = 0.662A$$

The minimum primary current to maintain ZVS switching is 0.662A. To see what this means in terms of output power the following calculation is performed:

$$I_O(Critical) = \frac{N_P}{N_S} \times 0.662 = 5 \times 0.662 = 3.31A$$

$$P_O(Critical) = 3.31A \times 5V = 16.6W$$

So the power at which the supply stops zero-voltage-switching is 16.6W, well below 1/2 Po(max), which is within the design goal requirements.

The right leg transition can now be determined using Equation 3:

$$t_{RL} = \frac{183 \times 10^{-12} \times 72}{0.662} = 20ns$$

The left-leg transition takes 34ns and the right-leg transition takes 20ns. These values can now be programmed as turn on delays via the HDEL and LDEL resistor values on the HIP4081A. As previously mentioned, since the HIP4081A controls the upper and lower delay times, both HDEL and LDEL should be set equal to the longest delay time. This time will be 34ns.

Resonant Component Selection

The core material selected for the resonant inductor was chosen for its high Q and low core loss characteristics. Micrometals powdered iron RF core T44-6 has a Q of 200 at the resonant frequency of interest, 7MHz ($F_{RES}=1/(4xt_{LL})$).

The output filter inductor was another Micrometals powdered iron RF core, T50-8 chosen for its low core loss at 500kHz. This material has the lowest core loss of any other material they offer. As a result, it is also the most expensive. Another core which may be used is the T50-52. The 52 material has slightly higher core loss and is less expensive.

Effects of Variations in MOSFET Parasitic Output Capacitance

The MOSFETs parasitic output capacitance, C_{OSS} can vary from part to part, and from manufacturer to manufacturer. However, this variability does not cause any severe aberration in the operation of the converter. The only noticeable effect can be a slight decrease in efficiency. This loss in efficiency is due to two factors.

The first and most significant is capacitive turn-on losses. This is caused by the energy required to displace the charge on the output capacitance when there is insufficient energy in the resonant inductor to perform this task. This is indicated by the first term in Equation 11. The other losses are simply turn-on and turn-off losses which normally occur if zero voltage switching is not in effect. These turn-on and turn-off switching losses are caused by the slight movement of the resonant peak with respect to the programmed ZVS delay time as C_{OSS} varies from its nominal value. This may cause drain-to-source voltage to occur simultaneously with drain current during a portion of the switching time, thereby decreasing efficiency. This is indicated by the second and third terms in Equation 11.

Figure 10 shows the curve of output capacitance as a function of drain-to-source voltage. C_{OSS} is measured at a drain-to-source voltage = 25V. This voltage point is designated as V_{OSS}. At this voltage point C_{OSS} is equal to 162pF as indicated by the curve.

Maximum variations of C_{OSS} for Intersil IRFR120 is ±20% of the measured value as shown by Figure 10. However, changes in C_{OSS} can be much more significant when select-

ing the same MOSFET from a different manufacturer. This is because each MOSFET manufacturer has different processes, resulting in changes from the typical value. This value can be significantly different from the typical value shown in the data sheets. Therefore, it is a good idea to work closely with your supplier to obtain the measured value for C_{OSS}. The measured value for C_{OSS} at V_{OSS} = 25V is 162pF as shown in Figure 10. Therefore, one can expect a worst case variation of ±20% from this value as indicated by Figure 10. It will be shown that even for large changes in C_{OSS}, the total power dissipation in the converter will not be impacted greatly. It should be pointed out that the initial design proceeded with C_{OSS} = 130pF as stated on the data sheet for the typical value. It was later determined that the measured value was 162pF. This difference had no noticeable effect on converter performance confirming that moderate variations in C_{OSS} have little or no effect on converter performance.

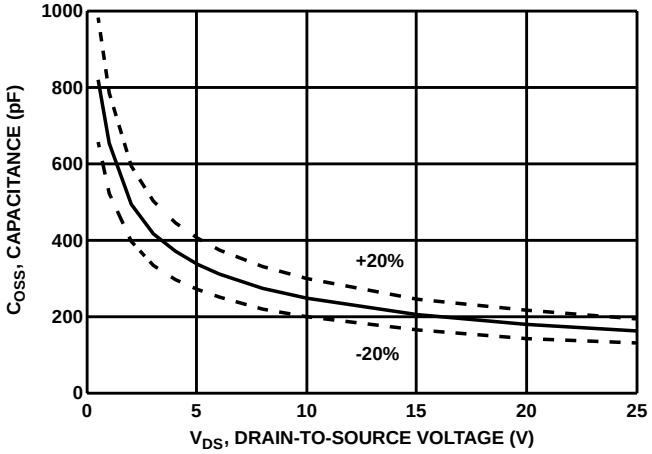

FIGURE 10. C_{OSS} CURVE FOR THE INTERSIL IRFR120

Figure 11 shows the effects of increased switching losses by varying C_{OSS} and the input voltage (essentially V_{DS}). Equation 11 was used to determine these curves and is derived in appendix A. From the curves of Figure11, it can be seen that even for large variations the impact in switching losses is not that great, especially if the converter is operating near full load. Again, one needs to understand their application to determine how much variation in C_{OSS} can be tolerated. Hopefully Figure11 will help give understanding to the impact of C_{OSS} variation on converter switching losses.

$$P_{SWLOSS} = \frac{\frac{4}{3} \times C_{OSS} \times V_{OSS}^{\frac{1}{2}} \times V_{IN}^{\frac{3}{2}} - \frac{1}{2} L_R \times I_{PRI}^2}{t_{CLK}} + \frac{I_{PRI} \times V_{SWLL} \times t_{SWLL}}{t_{CLK}} + \frac{I_{PRI} \times V_{SWRL} \times t_{SWRL}}{t_{CLK}} \quad \text{(EQ. 11)}$$

From Equation 11 it can be seen that the switching loss is ≤ zero if the resonant inductance has enough energy to displace the output capacitance and if the switching losses are zero due to ZVS operation. In the first term of the Equation, decreasing values of output capacitance are an advantage. Here the resulting energy in the resonant inductance exceeds the energy needed to displace the capacitance charge. Decreasing capacitance also means that the delay time set for the ZVS transition will be longer than necessary. This has no significant effect on converter efficiency. The efficiency will be slightly degraded only if the C_{OSS} value turns out larger than the target design. To counter this effect of possibly larger C_{OSS}, one could simply program the delays slightly longer than the calculated values. It should be pointed out that t_{SW} was chosen to be 10ns in Equation 11, to generate the curves of Figure 11.

In conclusion of this topic, once the measured value for C_{OSS} is known, one can expect a worst case change of ±20%. This change is insignificant to the converters performance as shown by Figure 11. Once a vendor is selected and transition delays are determined, the delays can be set and forgotten about.

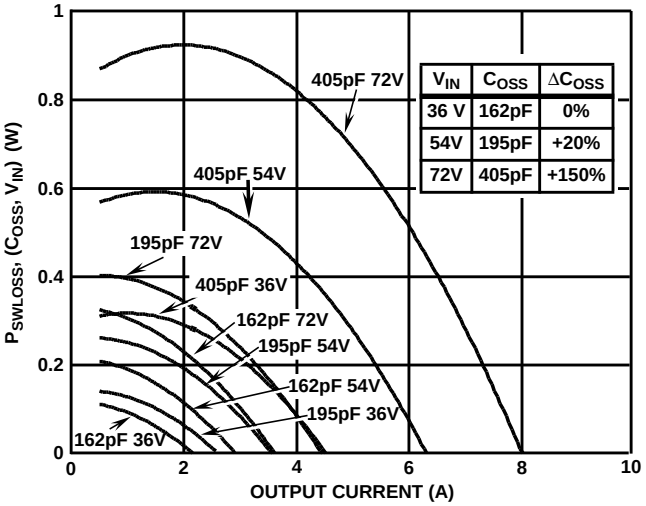

FIGURE 11. NON-ZVS OPERATION

Performance

Figures 12 and 13 show the primary voltage and current waveforms of the converter taken at a load current of 10A and an input voltage of 48V. As indicated below, the frequency of the primary side is 250kHz while the secondary side frequency will be twice the primary or 500kHz. The primary current scale is 0.5A per division yielding a $3A_{P-P}$ waveform. Notice how clean these waveforms are. This is one of the significant benefits of zero voltage switching. Additionally, the primary current and rectified secondary voltage is shown in Figure 14 to illustrate the erosion of the secondary duty cycle as mentioned earlier. The erosion is approximately 200ns, yielding a 10% reduction in the secondary side on time. The calculated value for a 48V input was 11% for a difference of 1%. This exemplifies the importance of using Equation 8 to calculate the erosion of the secondary. On the secondary side we have the same problem as with more classic topologies. A moderate snubber was added to the rectifier to reduce the ringing. The two graphs of Figures 15 and 16 show percent regulation and percent efficiency. Percent regulation was excellent. Over the full input voltage and load range, the maximum change in output voltage was 54mV. During moderate to high output current the efficiency was predominately in the low 80% range. The actual measurements correlated very closely with the loss analysis performed on this converter prior to its design. While this topology offers lossless switching, the conduction

losses do increase. What this topology offers for this configuration of input and output voltage is the ability to increase the switching frequency, while at the same time, providing much cleaner waveforms. The breakdown of the power loss data is given in Table 1. From these figures one can target specific areas to optimize the converter for greater efficiency. For instance, the current sense resistor can be replaced with a current transformer for improved efficiency.

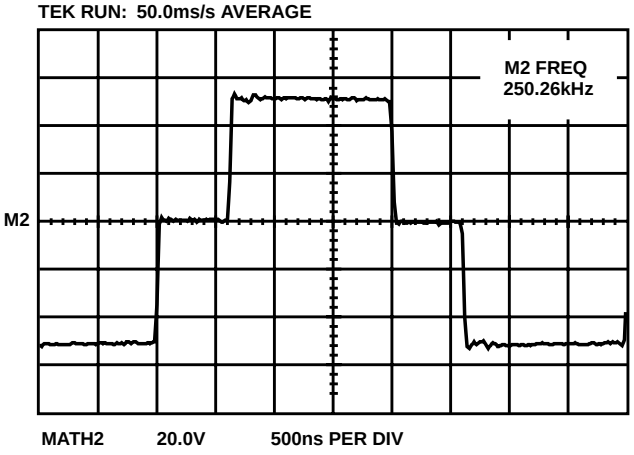

FIGURE 12.

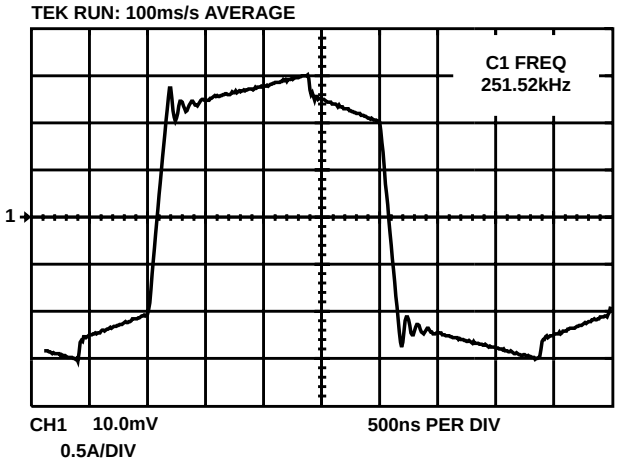

FIGURE 13.

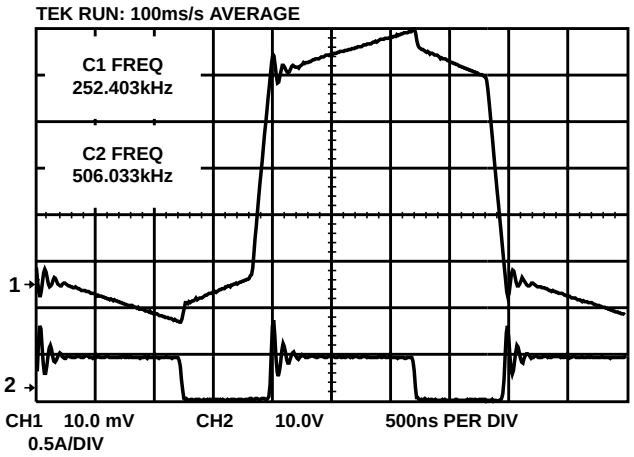

FIGURE 14.

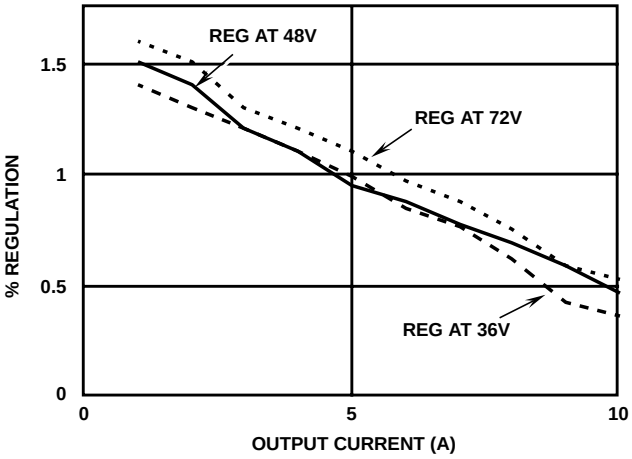

FIGURE 15.

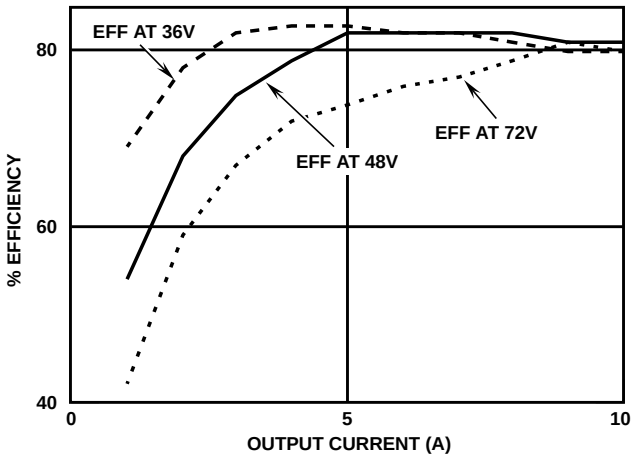

FIGURE 16.

TABLE 1. LOSS ANALYSIS AT V_{IN} = 48V, I_{OUT} = 10A

MOSFET Full-Bridge Conduction Losses	4W
Output Diode Losses	3W
Switching Losses	0W
Power Transformer Losses	0.8W
Output Inductor Losses	0.75W
Resonant Inductor Losses	0.57W
Current Sense Resistor Losses	1.2W
Snubber Losses	0.38W
Miscellaneous Losses	1.24W
Total Power Loss	11.94W
Efficiency	81%

Operating the converter with a load greater than 5A will require a heatsink attached to the output rectifier. In addition, the full bridge may require a larger copper area or small heatsink for heat removal.

The plots shown in Figure 17 illustrate the progression of zero voltage switching. The first and second plots show that the delay time is skewed from the nominal value. This is because the HIP4081A delay was made excessively large to illustrate the resonant half sinusoid. Ideally you want to set the delay to 1/4 the period of the resonant frequency. This delay time is determined by Equation 1. The final plot shows the delay set to the optimum point for proper zero voltage switching. Notice the absence of ringing on V_{DS} compared to when non-zvs operation is taking place!

The plots of Figures 18 and 19 illustrate zero voltage switching of switch A and switch B. In the first plot of Figure 18, the voltage across A is zero during turn-on of switch A. Here you can see the HIP4081A driving the high side FET. Notice the 12V step on this waveform. This 12V step voltage is being supplied by the HIP4081A bootstrap capacitor which turns on switch A. The second plot shows the gate drive of switch B, along with the same phase node, V_{DS} of switch B. Here, the voltage across switch B is zero during the turn-on of switch B. In the remaining plots of Figure 19, the mechanism is the same, but here the MOSFETS are being turned off. In all of these waveforms you can see that the delay time is nearly 34ns as calculated in the application note.

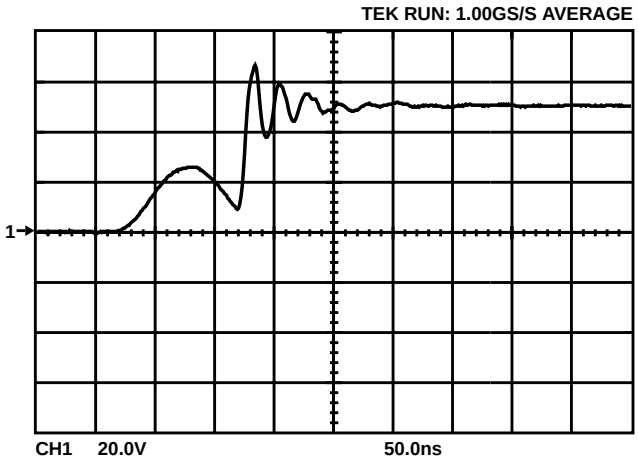

FIGURE 17A. HIP4081A DELAY SET FOR LARGE SKEW

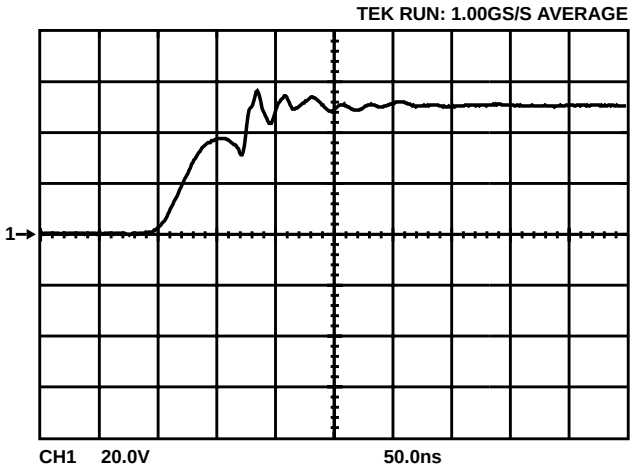

FIGURE 17B. HIP4081A DELAY SET FOR MODERATE SKEW

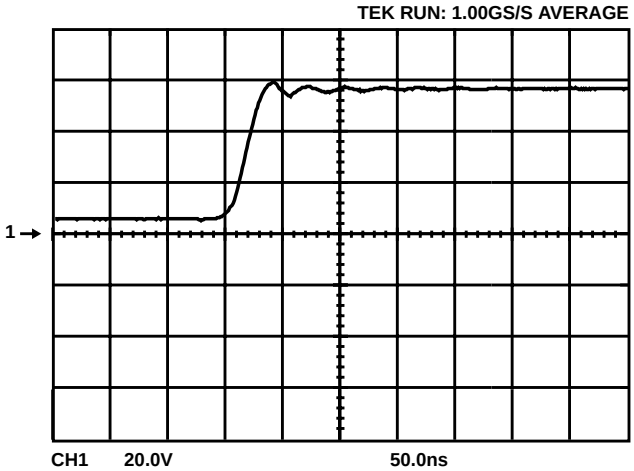

FIGURE 17C. HIP4081A DELAY SET FOR PROPER ZVS OPERATION

FIGURE 17. NON-ZVS TO ZVS PROGRESSION, V_{DS} OF SWITCH B, V_{IN} = 48V, I_{OUT} = 3A

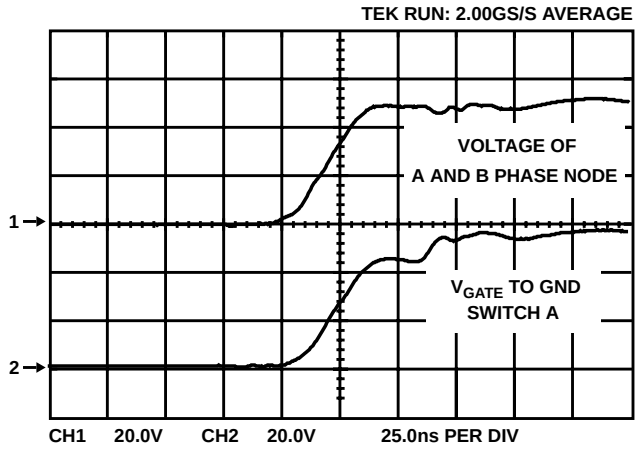

FIGURE 18A. VOLTAGE ACROSS SWITCH A = 0 DURING TURN-ON OF SWITCH A

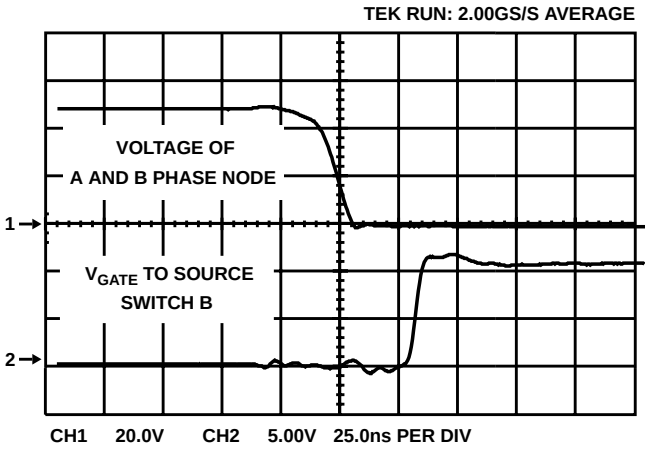

FIGURE 18B. VOLTAGE ACROSS SWITCH B = ZERO DURING TURN-ON OF SWITCH B

FIGURE 18. ZERO VOLTAGE SWITCHING OF SWITCH A AND B, ZVS TURN-ON

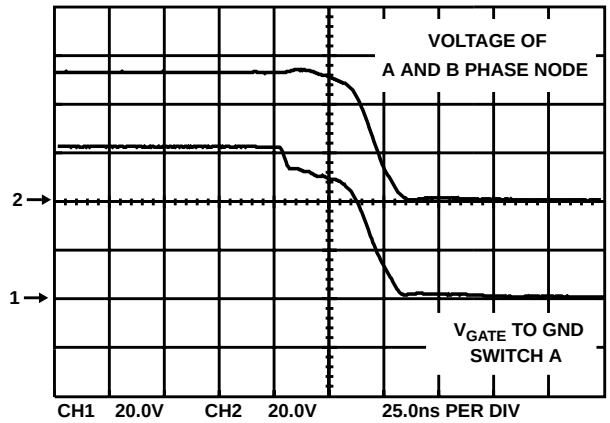

FIGURE 19A. VOLTAGE ACROSS SWITCH A = ZERO DURING TURN-OFF OF SWITCH A

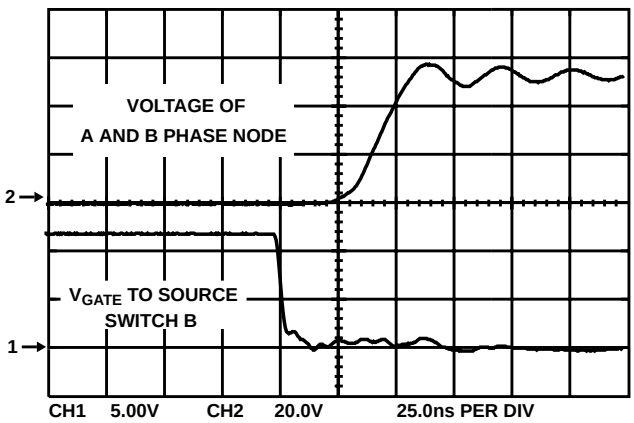

FIGURE 19B. VOLTAGE ACROSS SWITCH B = ZERO DURING TURN-OFF OF SWITCH B

FIGURE 19. ZERO VOLTAGE SWITCHING OF SWITCH A AND B, ZVS TURN-OFF

Conclusion

This topology was exciting and surprisingly simple to implement. It has been shown that the HIP4081A can be used successfully to realize the phase shift ZVS full-bridge topology. Not only does the HIP4081A drive the H-bridge but it also is capable of delivering the needed ZVS transition delay times required by this topology. In addition, a simple logic block was used to convert a single ended PWM output into the required phase shift logic drive signals.

A design process was developed to enable designers to accomplish their own designs. This was achieved by deriving essential equations and exposing key concepts. Following these procedures should allow designers to obtain success when incorporating this topology. What's more, much of the mystery of this topology has been removed, especially in the area of parasitic functionality within the design. It was shown that the output capacitance variation does not have a great impact on overall performance. It was shown that the effects of this variation can be determined easily with graphical methods.

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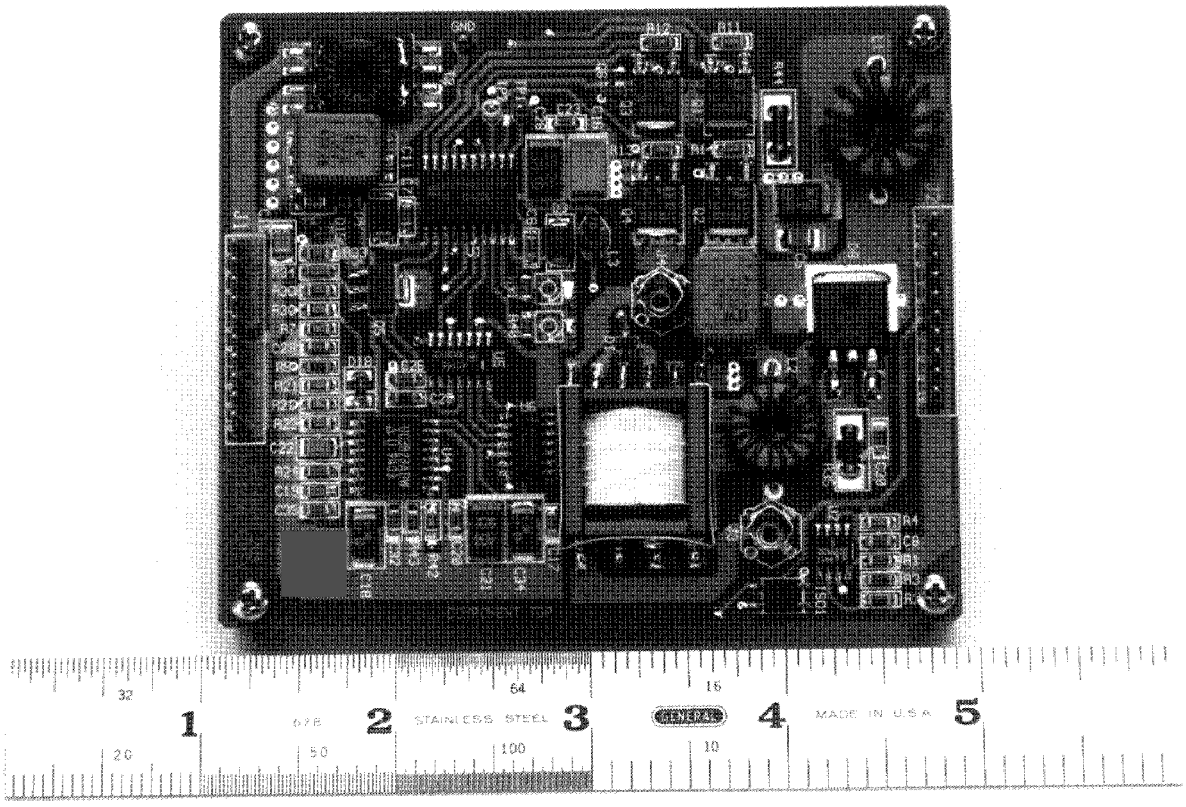
HIP4081A Converter



Material List

1	1	C3	100µF	10V
2	2	C11, C4	4µF	100V
3	1	C5	0.47µF	10V
4	7	C6, C7, C8, C17, C20, C23, C29	0.1µF	50V
5	2	C15, C14	0.1µF	100V
6	1	C16	33µF	20V
7	2	C18, C34	1µF	20V
8	2	C19, C32	470pF	50V
9	1	C21	47µF	20V
10	1	C22	0.22µF	50V
11	3	C25, C26, C30	2200pF	50V
12	1	C28	10µF	20V
13	1	D1	BAV70LT1	
14	1	D2	BZX84C75LT1	
15	2	D3, D4	MBRS1100T3	
16	1	D8	MBRB2535CTL	
17	1	D15	BZX84C12LT1	
18	1	D18	1N4148	
19	1	IS01	NEC PS2701-1	
20	1	J1	MOLEX 22-59-1310	
21	1	J2	MOLEX 22-59-1310	
22	1	L1	4µH	MICROMETALS T50-8
23	1	L2	2.0µH	MICROMETALS T50-6
24	1	L3	470µH	COILCRAFT DT1608
25	4	Q1, Q2, Q3, Q4	IRFR120	INTERSIL
26	1	Q5	BP720T1	
27	1	Q6	MMBT5401LT1	
28		Q7	MMBT3904LT1	
29	1	R1	39	
30	1	R2	15K	1%
31	1	R3	5.11K	1%
32	1	R4	4.99K	1%
33	1	R5	619K	1%
34	2	R21, R7	10K	
35	5	R11, R12, R13, R14, R34	10	
36	2	R23, R22	10K	1%
37	1	R24	6.49K	1%
38	1	R33	33K	
39	1	R35	100	1W
40	1	R38	47K	
41	1	R39	2.2K	
42	2	R40, R41	100K	
43	1	R42	20K	
44	1	R43	1K	
45	1	R44	0.470	2W
46	1	R45	4.7K	
47	1	T1	EPC-19	
48	1	T2	MICROMETALS T37-8	
49	1	U1	HIP4081A	INTERSIL
50	1	U2	UC39432	
51	1	U4	UC3823A	
52	1	U5	74ACT86	
53	1	U6	74ACT74	

Appendix A

Derivation of Equation 1

The equation for resonant frequency:

$$Fr = \frac{1}{2\pi\sqrt{LC}}$$

The left leg transition takes place within a period of 1/4 the resonant period.

$$t_{LL} = \frac{1}{4}(2\pi\sqrt{LC}) = \frac{\pi}{2}\sqrt{LC}$$

Derivation of Equation 2

The output capacity C_{OSS} is a depletion-dependant capacity whose value depends upon the impressed drain-to-source voltage. Therefore the drain-to-source capacitance value over varying drain-to-source voltages can be approximated as:

$$C_{DS}(V_{DS}, n) = C_{OSS}\left(\frac{V_{OSS}}{V_{DS}}\right)^n$$

Where n is between 1/2 and 1/3 for most MOSFETs, C_{OSS} is the measured output capacitance at a drain to source voltage V_{OSS}. Most manufacturers measure this value at V_{OSS} = 25V.

Derive Energy and substitute for current:

$$E = \int (v \times i)\, dt$$

$$i = \frac{dQ}{dt}$$

$$E = \int v\, dQ$$

Capacitance is a function of drain-to-source voltage:

$$C(V_{DS}) = \frac{dQ}{dV_{DS}}$$

$$E(V_{DS}, n) = \int V_{DS} C(V_{DS}, n)\, dV_{DS}$$

$$E(V_{DS}, n) = C_{OSS} V_{OSS}^n \int V_{DS}^{1-n} dV_{DS}$$

Integrating:

$$E(V_{DS}, n) = \frac{C_{OSS} \times V_{OSS}^n \times V_{DS}^{2-n}}{2-n}$$

Evaluate at n = 1/2 for the INTERSIL IRFR120:

$$E = \left(\frac{2}{3} C_{OSS}\right)\left(V_{OSS}^{\frac{1}{2}}\right)\left(V_{DS}^{\frac{3}{2}}\right)$$

Notice that the output capacitance is multiplied by the factor of 2/3. For the phase-shift ZVS topology there are two output capacitances (C_{OSS}) in parallel during each resonant transition. Therefore the effective energy and resonant capacitance is multiplied by 2 becoming:

$$E = \left(\frac{4}{3} C_{OSS}\right)\left(V_{OSS}^{\frac{1}{2}}\right)\left(V_{DS}^{\frac{3}{2}}\right)$$

$$C_R = \frac{4}{3} C_{OSS}$$

Derivation of Equation 10

When the energy in the resonant inductor is equal to the energy in the resonant capacitance the critical point of ZVS operation is reached. When energy in the resonant inductor is below the stored MOSFET capacitance energy there is Non-ZVS operation. When it is above there is ZVS operation. Therefore:

$$C_R \times V_{OSS}^{\frac{1}{2}} \times V_{DS}^{\frac{3}{2}} = \frac{1}{2} \times L_R \times I_{PRI}^2$$

V_{DS} is essentially V_{IN},
where V_{IN} is the maximum input voltage.

$$I_{PRI}(\text{Critical}) = \sqrt{\frac{2 \times C_R \times V_{OSS}^{\frac{1}{2}} \times V_{IN(MAX)}^{\frac{3}{2}}}{L_R}}$$

Derivation of Equation 11

The energy of the resonant capacitance C_R can be displaced by the energy in the resonant inductance L_R. When this happens the capacitive turn on loss is equal to zero:

$$C_R \times V_{OSS}^{\frac{1}{2}} \times V_{DS}^{\frac{3}{2}} - \frac{1}{2} \times L_R \times I_{PRI}^2 = 0$$

Since V_{DS} is essentially V_{IN}, the power required to displace the resonant capacitance is:

$$P_{SWLOSS} = \left(C_R \times V_{OSS}^{\frac{1}{2}} \times V_{IN}^{\frac{3}{2}} - \frac{1}{2} \times L_R \times I_{PRI}^2 \right) \times F_{XFMR}$$

$$F_{XFMR} = \frac{1}{2t_{CLK}}$$

Substituting and multiplying by two since there are two such transitions per period:

$$P_{SWLOSS} = \left[\frac{C_R \times V_{OSS}^{\frac{1}{2}} \times V_{IN}^{\frac{3}{2}} - \frac{1}{2} \times L_R \times I_{PRI}^2}{2t_{CLK}} \right] \times 2$$

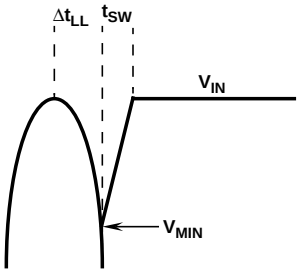
$$= \frac{C_R \times V_{OSS}^{\frac{1}{2}} \times V_{IN}^{\frac{3}{2}} - \frac{1}{2} \times L_R \times I_{PRI}^2}{t_{CLK}}$$

From the ZVS Transition times:

$$\Delta t_{LL}(C_{OSS}) = \left(\frac{\pi}{2} \times \sqrt{C_R(C_{OSS}) \times L_R} \right) - t_{LL}$$

$$\Delta t_{RL}(C_{OSS}) = \left(\frac{C_R(C_{OSS}) \times 72}{I_{PRICRIT}(C_{OSS})} \right) - t_{RL}$$

Determine switched V_{DS} for t_{LL} Skew:



Where t_{SW} is the MOSFET switching time during the non-zvs portion of the waveform. This can be caused by a delay too long as shown or by a delay too short.

$$\Delta t_{LL} = \frac{1}{2\pi F_{RES}} \times \arcsin\left(\frac{V_{MIN}}{V_{IN}} \right)$$

$$\sin(\omega_{RES} \times \Delta t_{LL}) = \frac{V_{MIN}}{V_{IN}}$$

$$V_{SWLL}(C_{OSS}, V_{IN}) = V_{IN} \times \sin(\omega_{RES} \times \Delta t_{LL}(C_{OSS}))$$

Determine switched V_{DS} for t_{RL} Skew:

From Equation 3:

$$V_{SWRL}(C_{OSS}) = \frac{\Delta t_{RL}(C_{OSS}) \times I_{PRICRIT}}{C_R}$$

Combining:

$$P_{SWLOSS}\left(C_{0SS}, V_{IN}\right) = \frac{C_R \times V_{OSS}^{\frac{1}{2}} \times V_{IN}^{\frac{3}{2}} - \frac{1}{2} \times L_R \times I_{PRI}^2}{t_{CLK}}$$

$$+ \frac{I_{PRI} \times V_{SWLL}\left(C_{OSS}, V_{IN}\right) \times t_{SWLL}}{t_{CLK}}$$

$$+ \frac{I_{PRI} \times V_{SWRL}\left(C_{OSS}\right) \times t_{SWRL}}{t_{CLK}}$$