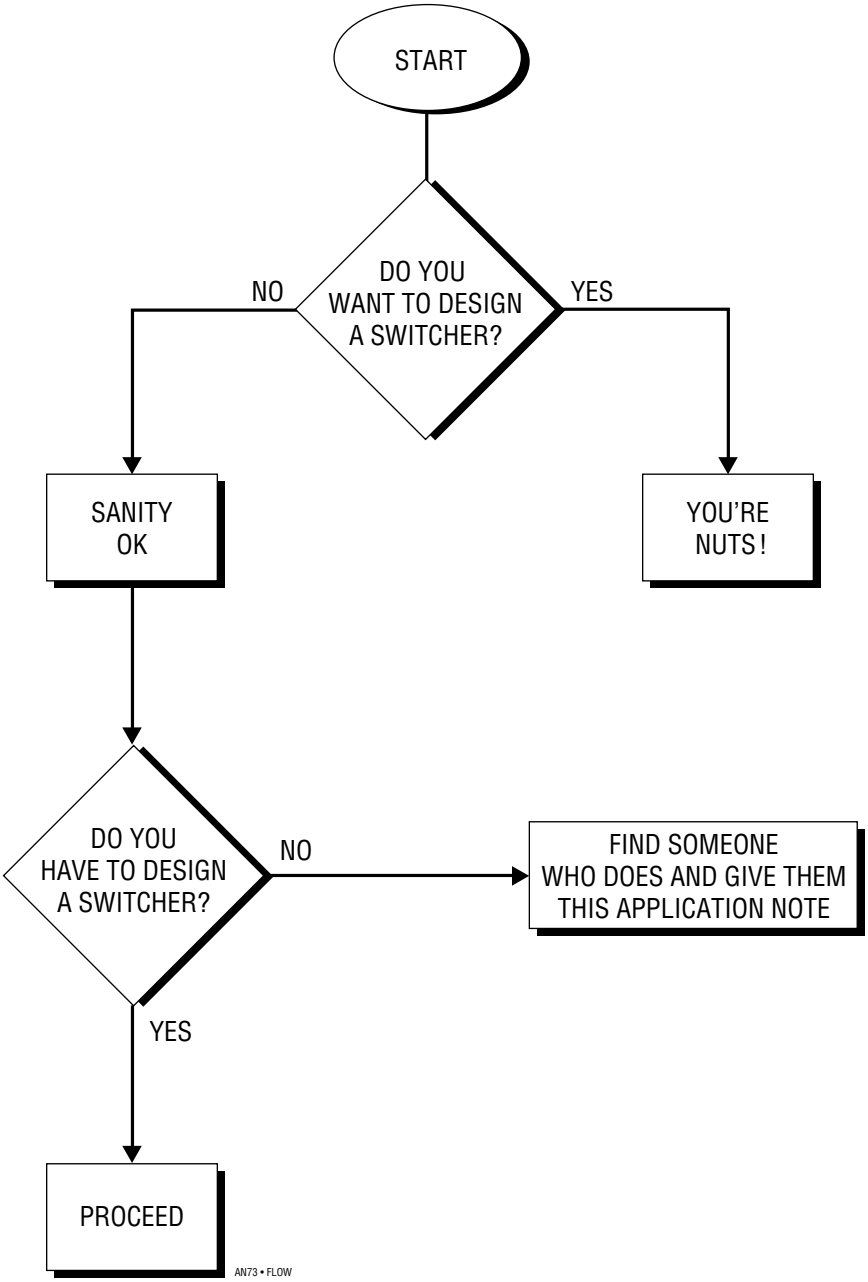
LT1339 Design Manual

Designing the Power Converter

Dale Eagar



PREFACE

Switching Power Converter: an Early Example

Although the origin of switching power converters is lost in antiquity, some early machines have been identified that work on this principle. Among the first was the hydraulic impulse pump, in use centuries before the use of electricity (see Figure 1). This device allows some of the energy in the stream of water flowing from point A to point B to be diverted to pump a smaller amount of water from point B to point C. Here is how this "water hammer" works (refer to Figures 1 and 2). First, the control valve SW1 opens at time t_1 and flow commences through the downpipe L1. As the velocity of water flow in the downpipe increases, so does the energy stored in the moving mass. ($E = 1/2MV^2$, where M = mass of the moving water, V = the velocity of the moving water, and E = energy, usually expressed in Joules). When the valve SW1 has been open long enough for the water flow rate to reach a valve that is a significant percentage of the theoretical maximum flow rate, we shut the valve SW1. This is t_2 in Figure 2. By shutting the control valve SW1 at time t_2, we attempt to arrest the flow through the downpipe. One thing about energy—it doesn't like being abandoned, so the pressure rises until something gives. Lucky for our downpipe, we have a check valve that can open and divert the otherwise-trapped energy into C1, the output damper. Enough H_2O moves through the check valve D1 and into C1 at a pressure head above the load head H2 to remove all kinetic energy associated with the down flow in the downpipe. Hence, for every hogshead of water that flows into the downpipe, a partial hogshead of water is delivered to the barrel at point C.

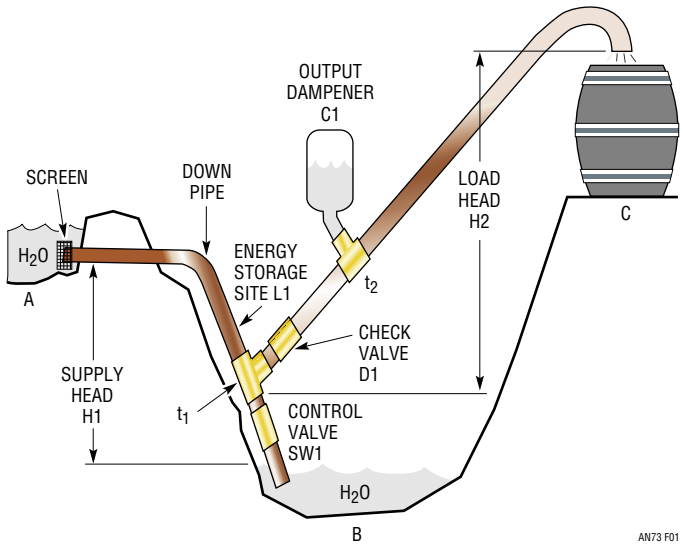


Figure 1. Hydraulic Impulse Pump (Water Hammer)

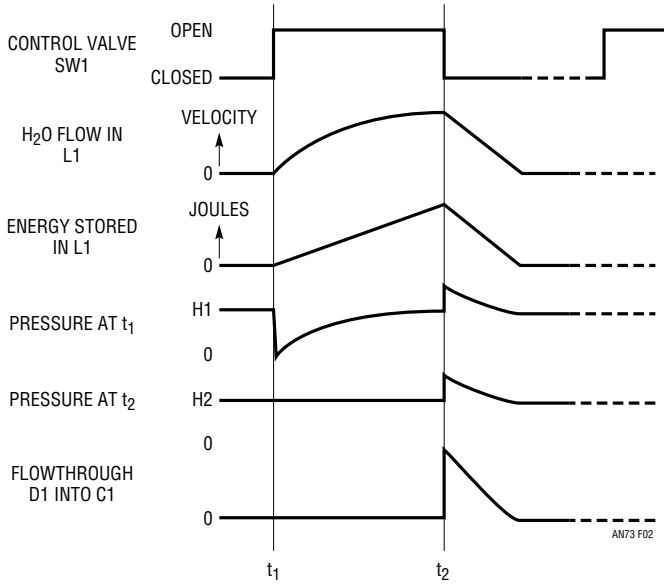


Figure 2. Water Hammer Waveforms

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INTRODUCTION

The advent of the switching regulator has greatly reduced the size, weight and volume of power conversion circuitry, while improving both the speed of response and efficiency. With the output voltage requirements going ever lower and currents ever higher, close scrutiny is applied to the loss mechanisms of the power converter. The loss mechanisms are divided into three classes: resistance loss, fixed voltage loss and switching loss. Resistance losses are caused by the circuit resistances (input capacitor ESR, power switch on-resistance, DC and AC resistance of the inductor, resistance of any current-sense elements, resistance in the output diode and ESR in the output capacitors), each multiplied by the squares of their respective currents. Fixed voltage losses associated with diode forward drops can be calculated by multiplying diode forward voltage by diode current. Switching losses are caused by both the finite turn-on and turn-off times of the MOSFETs and the stray capacitance on the source of the top MOSFET. As the trend toward higher output current progresses, the first thing to do is minimize all losses caused by resistance (because the power is proportional to I^2R). It is easy to minimize resistance because we have available very low ESR capacitors, low on-resistance MOSFETs and low series-resistance inductors. We have controllers that place a very small voltage across the current sense resistors. We do such a good job of dropping the resistive loss mechanisms that the output diode forward-voltage drop becomes the greatest loss mechanism. This is how the mandate for synchronous rectification comes about. Synchronous rectification is achieved by replacing the output diode with a low on-resistance switch. With synchronous rectification, efficiencies are higher, and, more importantly, power dissipated in the switching power supply is lower, often eliminating the need for heat sinks and/or fans.

High Power Synchronous DC/DC Controller

FEATURES

- **High Voltage: Operation Up to 60V**
- **High Current: Dual N-Channel Synchronous Drive Handles Up to 10,000pF Gate Capacitance**
- Programmable Average Load Current Limiting
- 5V Reference Output with 10mA External Loading Capability
- Programmable Fixed Frequency Synchronizable Current Mode Operation Up to 150kHz
- Undervoltage Lockout with Hysteresis
- Programmable Start Inhibit for Power Supply Sequencing and Protection
- Adaptive Nonoverlapping Gate Drive Prevents Shoot-Through

APPLICATIONS

- 48V Telecom Power Supplies
- Personal Computers and Peripherals
- Distributed Power Converters
- Industrial Control Systems
- Lead-Acid Battery Backup Systems
- Automotive and Heavy Equipment

DESCRIPTION

The LT®1339 is a high power synchronous current mode switching regulator controller. The IC drives dual N-channel MOSFETs to create a single IC solution for high power DC/DC converters in applications up to 60V.

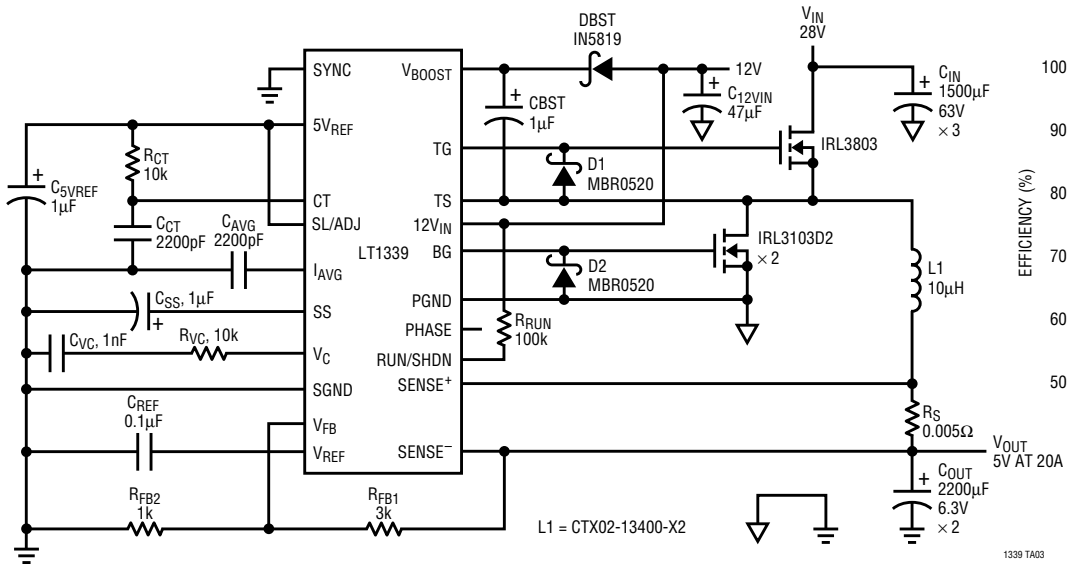
The LT1339 incorporates programmable average current limiting, allowing accurate limiting of DC load current independent of inductor ripple current. The IC also incorporates user-adjustable slope compensation for minimization of magnetics at duty cycles up to 90%.

The LT1339 timing oscillator operating frequency is programmable and can be synchronized up to 150kHz. Minimum off-time operation provides main switch protection. The IC also incorporates a soft start feature that is gated by both shutdown and undervoltage lockout conditions.

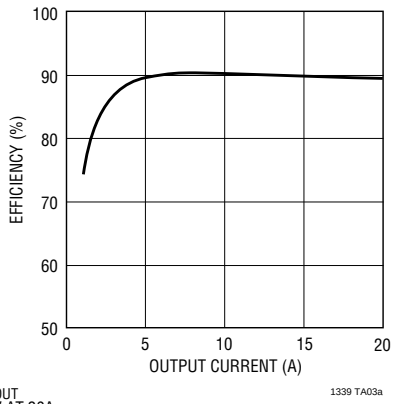
An output phase reversal pin allows flexibility in configuration of converter types, including inverting and negative topologies.

TYPICAL APPLICATION

28V to 5V 20A Buck Converter



28V to 5V Efficiency



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages
- Power Supply Voltage ($12V_{IN}$) ..... –0.3V to 20V
- Topside Supply Voltage (V_{BOOST})
  - V_{TS} – 0.3V to V_{TS} + 20V (V_{MAX} = 75V)
- Topside Reference Pin Voltage (TS) ..... –0.3V to 60V

Input Voltages
- Sense Amplifier Input Common Mode ... –0.3V to 60V
- RUN/SHDN Pin Voltage ..... –0.3V to $12V_{IN}$
- All Other Inputs ..... –0.3V to 7V

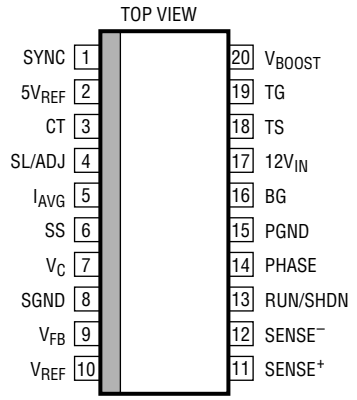
Maximum Currents
- 5V Reference Output Current 65mA

Maximum Temperatures
- Operating Ambient Temperature Range
  - LT1339C ..... 0°C to 70°C
  - LT1339I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
20-LEAD PDIP

SW PACKAGE
20-LEAD PLASTIC SO WIDE

T_{JMAX} = 125°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 85°C/W (SW)

ORDER PART NUMBER
LT1339CN
LT1339CSW
LT1339IN
LT1339ISW

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

$12V_{IN}$ = V_{BOOST} = 12V, V_C = 2V, TS = 0V, V_{FB} = V_{REF} = 1.25V, C_{TG} = C_{BG} = 3000pF, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply and Protection							
I_{12VIN}	DC Active Supply Current (Note 2)		●		14	20	mA
	DC Standby Supply Current	$V_{RUN/SHDN}$ < 0.5V	●		150	250	µA
I_{BOOST}	DC Active Supply Current (Note 2)				2.2		mA
	DC Standby Supply Current	$V_{RUN/SHDN}$ < 0.5V			0		µA
$V_{RUN/SHDN}$	Shutdown Rising Threshold		●	1.15	1.25	1.35	V
V_{SSHYST}	Shutdown Threshold Hysteresis				25		mV
I_{SS}	Soft Start Charge Current		●	4	8	14	µA
V_{UVLO}	Undervoltage Lockout Threshold - Falling		●	8.20	9.00	9.75	V
	Undervoltage Lockout Threshold - Rising		●		9.35	9.95	V
	Undervoltage Lockout Hysteresis		●	200	350		mV
5V Reference							
V_{REF5}	5V Reference Voltage	Line, Load and Temperature	●	4.75	5.00	5.25	V
	5V Reference Line Regulation	10V ≤ $12V_{IN}$ ≤ 15V	●		3	5	mV/V
I_{REF5}	5V Reference Load Range - DC		●			10	mA
	Pulse		●			20	mA
	5V Reference Load Regulation	0 ≤ I_{REF5} ≤ 20mA	●		–1.25	–2	V/A
I_{SC}	5V Reference Short-Circuit Current				45		mA

ELECTRICAL CHARACTERISTICS

$12V_{IN} = V_{BOOST} = 12V$, $V_C = 2V$, TS = 0V, $V_{FB} = V_{REF} = 1.25V$, $C_{TG} = C_{BG} = 3000pF$, $T_A = 25°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Error Amplifier							
V_{FB}	Error Amplifier Reference Voltage	Measured at Feedback Pin	 ●	1.242 1.235	1.250 1.250	1.258 1.265	V V
I_{FB}	Feedback Input Current	$V_{FB} = V_{REF}$	●	0.1	0.5	1.0	µA
g_m	Error Amplifier Transconductance		●	1200	2000	3200	µmho
A_V	Error Amplifier Voltage Gain		●	1500	3000		V/V
I_{VC}	Error Amplifier Source Current Error Amplifier Sink Current	 $V_{FB} - V_{REF} = 500mV$	● ●	200 280	275 400		µA µA
V_{VC}	Absolute V_C Clamp Voltage	Measured at V_C Pin			3.5		V
V_{SENSE}	Peak Current Limit Threshold Average Current Limit Threshold (Note 4)	Measured at Sense Inputs Measured at Sense Inputs	● ●	170 110	190 120	 130	mV mV
V_{IAVG}	Average Current Limit Threshold	Measured at I_{AVG} Pin			2.5		V
Current Sense Amplifier							
A_V	Amplifier DC Gain	Measured at I_{AVG} Pin			15		V/V
V_{OS}	Amplifier Input Offset Voltage	$2V < V_{CMSENSE} < 60V$, $SENSE^+ - SENSE^- = 5mV$	●	0.1			mV
I_B	Input Bias Current	Sink ($V_{CMSENSE} > 5V$) Source ($V_{CMSENSE} = 0V$)	● ●		45 700	75 1200	µA µA
Oscillator							
f_O	Operating Frequency, Free Run Frequency Programming Error (Note 3)	 $f_O \leq 150kHz$	● ●	 –5		150 5	kHz %
I_{CT}	Timing Capacitor Discharge Current	LT1339C LT1339I	● ●	2.20 2.10	2.50 2.50	2.75 2.75	mA mA
V_{SYNC}	SYNC Input Threshold	Rising Edge	●	0.8		2.0	V
f_{SYNC}	SYNC Frequency Range	$f_{SYNC} \leq 150kHz$	●	f_O		$1.4f_O$	
Output Drivers							
$V_{TG,BG}$	Undervoltage Output Clamp Standby Mode Output Clamp	$12V_{IN} \leq 8V$ $V_{RUN} < 0.5V$	● ●		0.4	0.7 0.1	V V
V_{TG}	Top Gate On Voltage Top Gate Off Voltage		● ●	11.0	11.9 0.4	12.0 0.7	V V
t_{TGR}	Top Gate Rise Time		●		130	200	ns
t_{TGF}	Top Gate Fall Time		●		60	140	ns
V_{BG}	Bottom Gate On Voltage Bottom Gate Off Voltage		● ●	11.0	11.9 0.4	12.0 0.7	V V
t_{BGR}	Bottom Gate Rise Time		●		70	200	ns
t_{BGF}	Bottom Gate Fall Time		●		60	140	ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

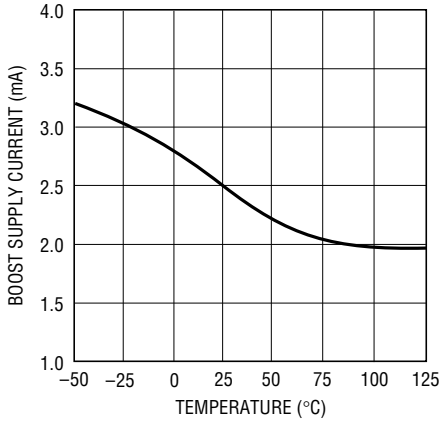
Note 2: Supply current specification does not include external FET gate charge currents. Actual supply currents will be higher and vary with operating frequency, operating voltages and the type of external FETs used. See Application Information section.

Note 3: Test condition: $R_{CT} = 16.9k$, $C_{CT} = 1000pF$.

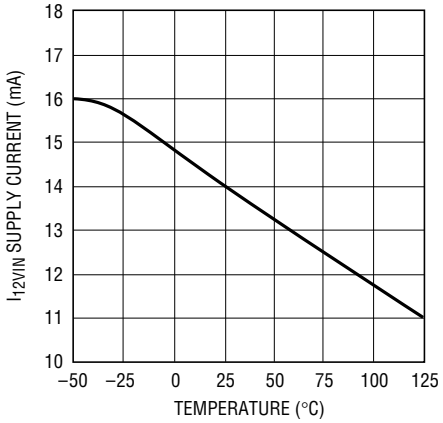
Note 4: Test Condition: $V_{CMSENSE} = 10V$.

TYPICAL PERFORMANCE CHARACTERISTICS

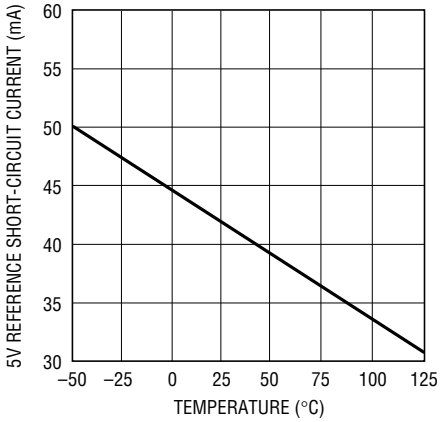
Boost Supply Current vs Temperature



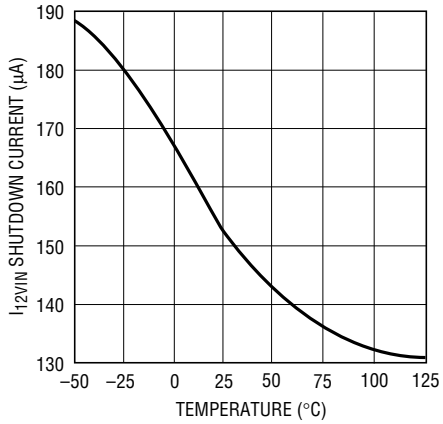
$12V_{IN}$ Supply Current vs Temperature



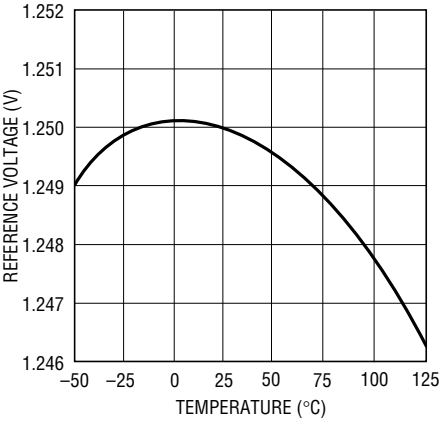
5V Reference Short-Circuit Current vs Temperature



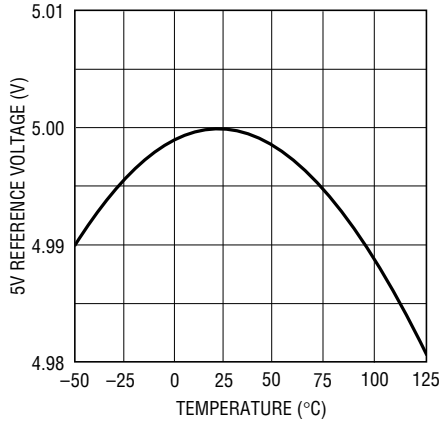
I_{12VIN} Shutdown Current vs Temperature



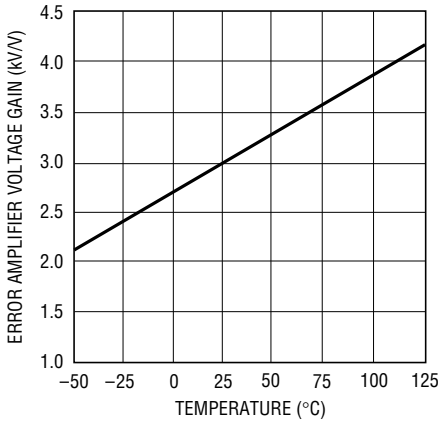
Reference Voltage vs Temperature



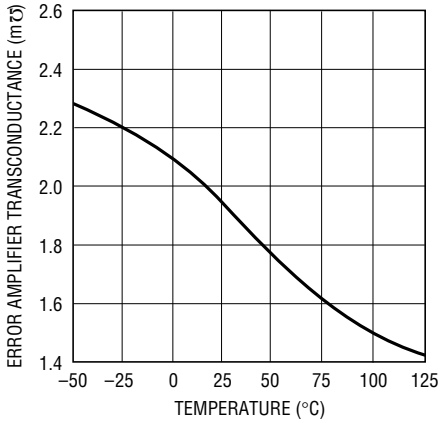
5V Reference Voltage vs Temperature



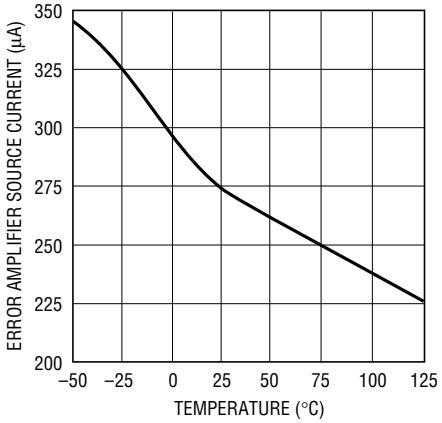
Error Amplifier Voltage Gain vs Temperature



Error Amplifier Transconductance vs Temperature

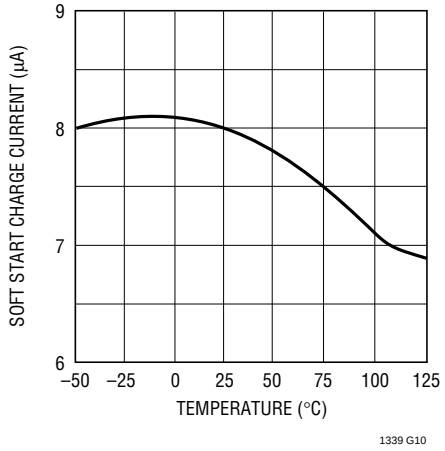


Error Amplifier Maximum Source Current vs Temperature

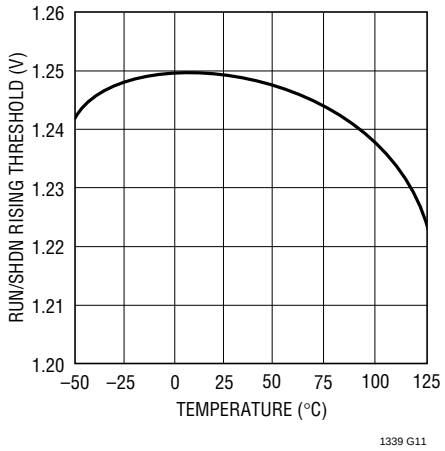


TYPICAL PERFORMANCE CHARACTERISTICS

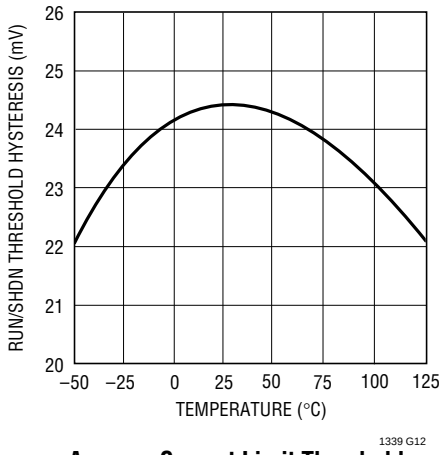
Soft Start Charge Current vs Temperature



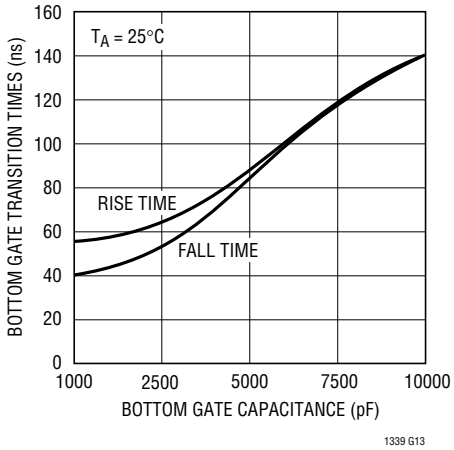
RUN/SHDN Rising Threshold vs Temperature



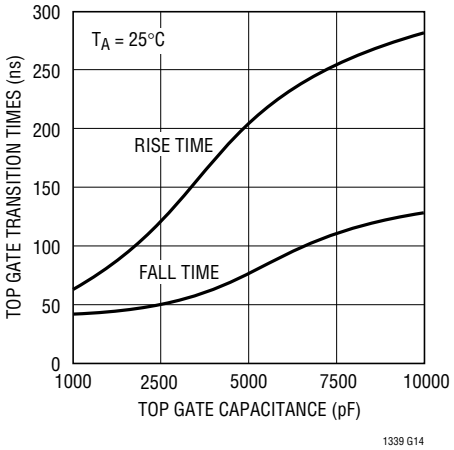
RUN/SHDN Threshold Hysteresis vs Temperature



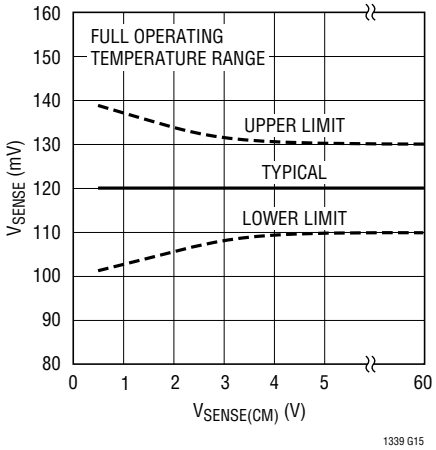
Bottom Gate Transition Times vs Bottom Gate Capacitance



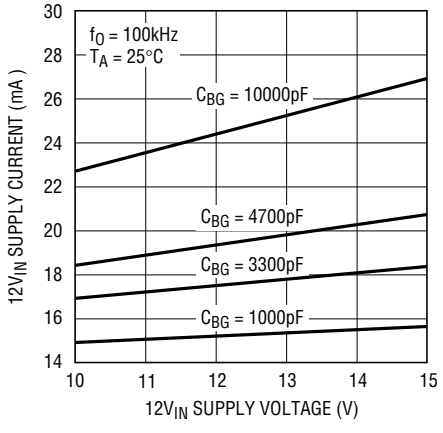
Top Gate Transition Times vs Top Gate Capacitance



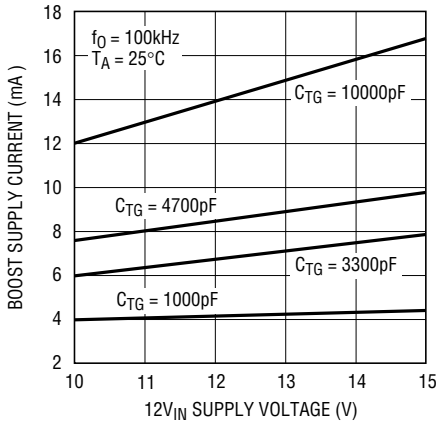
Average Current Limit Threshold Sense Voltage Tolerance vs Common Mode Voltage



$12V_{IN}$ Supply Current vs Supply Voltage

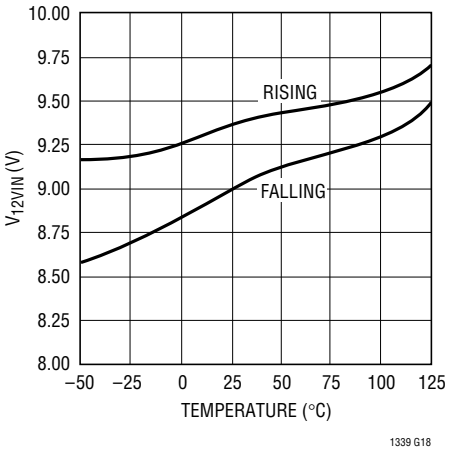


Boost Supply Current vs $12V_{IN}$ Supply Voltage

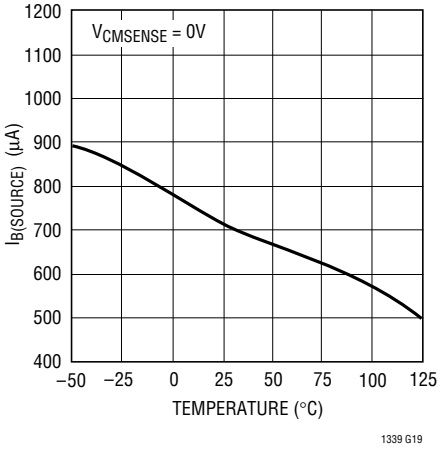


TYPICAL PERFORMANCE CHARACTERISTICS

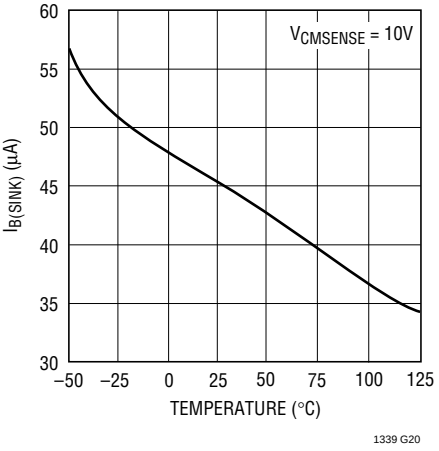
UVLO Thresholds vs Temperature



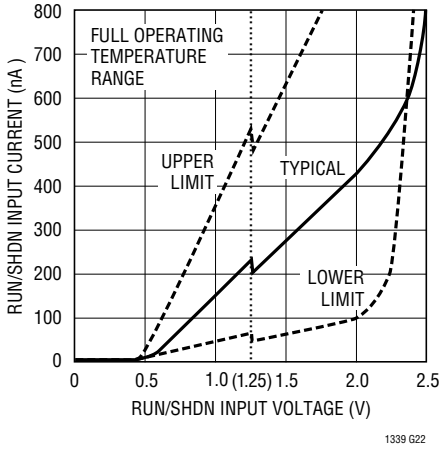
Sense Amplifier Input Bias Current (Source) vs Temperature



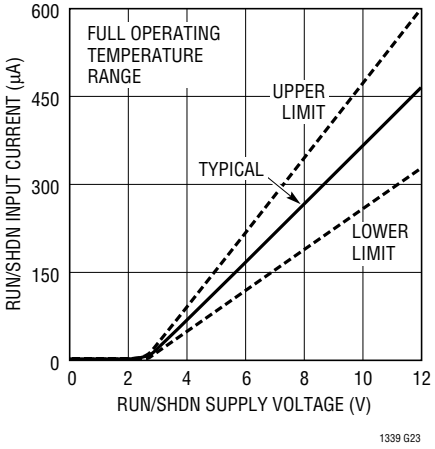
Sense Amplifier Input Bias Current (Sink) vs Temperature



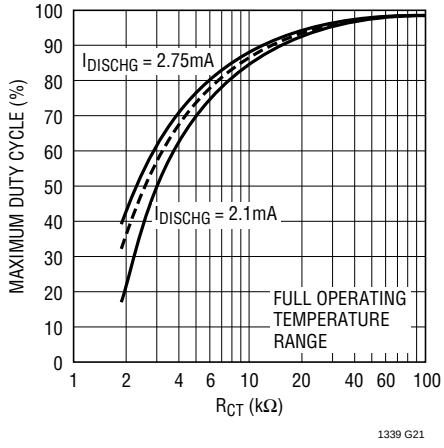
RUN/SHDN Input Current vs Pin Voltage



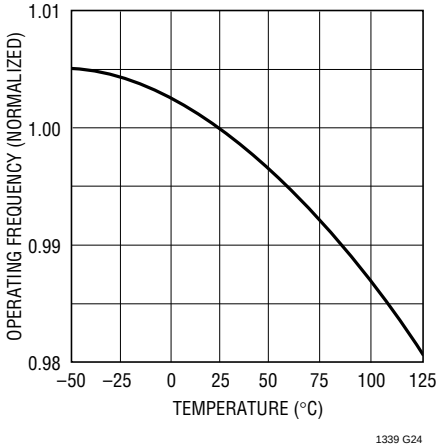
RUN/SHDN Input Current vs Pin Voltage



Maximum Duty Cycle vs R_{CT}



Operating Frequency (Normalized) vs Temperature



PIN FUNCTIONS

SYNC (Pin 1): Oscillator Synchronization Pin with TTL-Level Compatible Input. Input drives internal rising edge triggered one-shot; sync signal on/off times should be ≥1µs (10% to 90% DC at 100kHz). Does not contain internal pull-up. Connect to SGND if not used.

$5V_{REF}$ (Pin 2): 5V Output Reference. Allows connection of external loads up to 10mA DC. (Reference is not available in shutdown.) Typically bypassed with 1µF capacitor to SGND.

CT (Pin 3): Oscillator Timing Pin. Connect a capacitor (C_{CT}) to ground and a pull-up resistor (R_{CT}) to the $5V_{REF}$ supply. Typical values are CT = 1000pF and $10k \leq R_{CT} \leq 30k$.

SL/ADJ (Pin 4): Slope Compensation Adjustment. Allows increased slope compensation for certain high duty cycle applications. Resistive loading of the pin increases effective slope compensation. A resistor divider from the $5V_{REF}$ pin can tailor the onset of additional slope compensation to specific regions in each switch cycle. Pin can be floated or connected to $5V_{REF}$ if no additional slope compensation is required. (See Applications Information section for slope compensation details.)

I_{AVG} (Pin 5): Average Current Limit Integration. Frequency response characteristic is set using the 50kΩ output impedance and external capacitor to ground. Averaging roll-off typically set at 1 to 2 orders of magnitude under switching frequency. (Typical capacitor value ~1000pF for f_O = 100kHz.) Shorting this pin to SGND will disable the average current limit function.

SS (Pin 6): Soft Start. Generates ramping threshold for regulator current limit during start-up and after UVLO event by sourcing about 8µA into an external capacitor.

V_C (Pin 7): Error Amplifier Output. RC load creates dominant compensation in power supply regulation feedback loop to provide optimum transient response. (See Applications Information section for compensation details.)

SGND (Pin 8): Small-Signal Ground. Connect to negative terminal of C_{OUT}.

V_{FB} (Pin 9): Error Amplifier Inverting Input. Used as voltage feedback input node for regulator loop. Pin sources about 0.5µA DC bias current to protect from an open feedback path condition.

V_{REF} (Pin 10): Bandgap Generated Voltage Reference Decoupling. Connect a capacitor to signal ground. (Typical capacitor value ~0.1µF.)

$SENSE^+$ (Pin 11): Current Sense Amplifier Inverting Input. Connect to most positive (DC) terminal of current sense resistor.

$SENSE^-$ (Pin 12): Current Sense Amplifier Noninverting Input. Connect to most negative (DC) terminal of current sense resistor.

RUN/SHDN (Pin 13): Precision Referenced Shutdown. Can be used as logic level input for shutdown control or as an analog monitor for input supply undervoltage protection, etc. IC is enabled when RUN/SHDN pin rising edge exceeds 1.25V. About 25mV of hysteresis helps assure stable mode switching. All internal functions are disabled in shutdown mode. If this function is not desired, connect RUN/SHDN to $12V_{IN}$ (typically through a 100k resistor). See Applications Information section.

PHASE (Pin 14): Output Driver Phase Control. If Pin 14 is not connected (floating), the topside driver operates the main switch, with the bottom side driver operating the synchronous switch. Shorting Pin 14 to ground reverses the roles of the output drivers. PHASE is typically shorted to ground for inverting and boost configurations. Positive buck configuration requires the PHASE pin to float. See Applications Information section.

PGND (Pin 15): Power Ground. References the bottom side output switch and internal driver control circuits. Connect with low impedance trace to V_{IN} decoupling capacitor negative (ground) terminal.

BG (Pin 16): Bottom Side Output Driver. Connects to gate of bottom side external power FET.

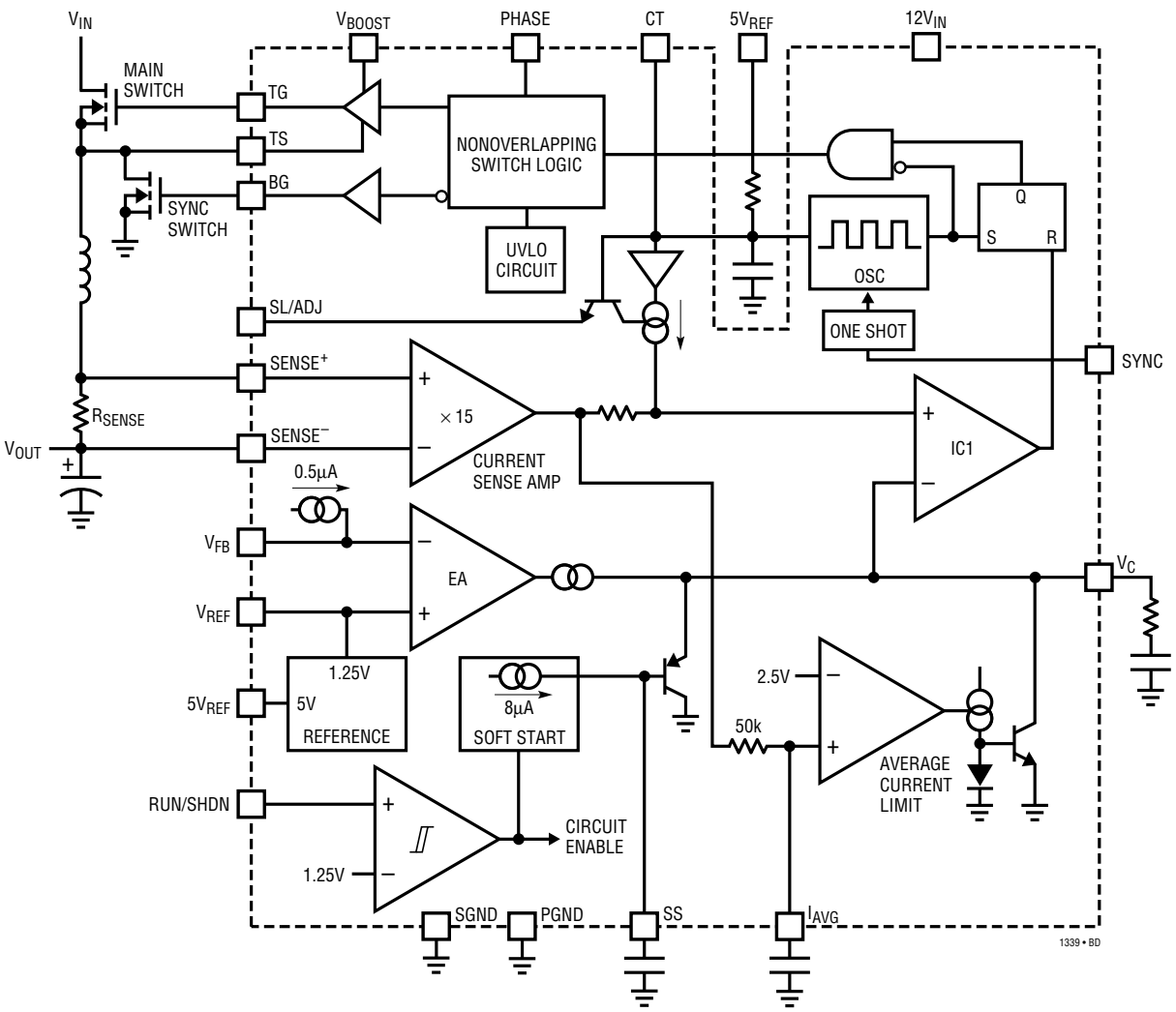
$12V_{IN}$ (Pin 17): 12V Power Supply Input. Bypass with at least 1µF to PGND.

TS (Pin 18): Boost Output Driver Reference. Typically connects to source of topside external power FET and inductive switch node.

TG (Pin 19): Topside (Boost) Output Driver. Connects to gate of topside external power FET.

V_{BOOST} (Pin 20): Topside Power Supply. Bootstrapped via 1µF capacitor tied to switch node (Pin 18) and Schottky diode connected to the $12V_{IN}$ supply.

FUNCTIONAL BLOCK DIAGRAM



OPERATION (Refer to Functional Block Diagram)

Basic Control Loop

The LT1339 uses a constant frequency, current mode synchronous architecture. The timing of the IC is provided through an internal oscillator circuit, which can be synchronized to an external clock, programmable to operate at frequencies up to 150kHz. The oscillator creates a modified sawtooth wave at its timing node (CT) with a slow charge, rapid discharge characteristic.

During typical positive buck operation, the main switch MOSFET is enabled at the start of each oscillator cycle. The main switch stays enabled until the current through the switched inductor, sensed via the voltage across a series sense resistor (R_{SENSE}), is sufficient to trip the current comparator (IC1) and, in turn, reset the RS latch. When the RS latch resets, the main switch is disabled, and the synchronous switch MOSFET is enabled. Shoot-through prevention logic prohibits enabling of the synchronous switch until the main switch is fully disabled. If the current comparator threshold is not obtained throughout the entire oscillator charge period, the RS latch is bypassed and the main switch is disabled during the oscillator discharge time. This “minimum off time” assures adequate charging of the bootstrap supply, protects the main switch, and is typically about 1µs.

OPERATION (Refer to Functional Block Diagram)

The current comparator trip threshold is set on the V_C pin, which is the output of a transconductance amplifier, or error amplifier (EA). The error amplifier integrates the difference between a feedback voltage (on the V_{FB} pin) and an internal bandgap generated reference voltage of 1.25V, forming a signal that represents required load current. If the supplied current is insufficient for a given load, the output will droop, thus reducing the feedback voltage. The error amplifier forces current out of the V_C pin, increasing the current comparator threshold. Thus, the circuit will servo until the provided current is equal to the required load and the average output voltage is at the value programmed by the feedback resistors.

Average Current Limit

The output of the sense amplifier is monitored by a single pole integrator comprised of an external capacitor on the I_{AVG} pin and an internal impedance of approximately 50kΩ. If this averaged value signal exceeds a level corresponding to 120mV across the external sense resistor, the current comparator threshold is clamped and cannot continue to rise in response to the error amplifier. Thus, if average load current requirements exceed $120mV/R_{SENSE}$, the supply will current limit and the output voltage will fall out of regulation. The average current limit circuit monitors the sense amplifier output without slope compensation or ripple current contributions, therefore the average load current limit threshold is unaffected by duty cycle.

Undervoltage Lockout

The LT1339 employs an undervoltage lockout circuit (UVLO) that monitors the 12V supply rail. This circuit disables the output drive capability of the LT1339 if the 12V supply drops below about 9V. Unstable mode switching is prevented through 350mV of UVLO threshold hysteresis.

Adaptive Nonoverlapping Output Stage

The FET driver output stage implements adaptive nonoverlapping control. This circuitry maintains dead time independent of the type, size or operating conditions of the switch elements. The control circuit monitors the output gate drive signals, insuring that the switch gate (being disabled) is fully discharged before enabling the other switch driver.

Shutdown

The LT1339 can be put into low current shutdown mode by pulling the RUN/SHDN pin low, disabling all circuit functions. The shutdown threshold is a bandgap referred voltage of 1.25V typical. Use of a precision threshold on the shutdown circuit enables use of this pin for undervoltage protection of the V_{IN} supply and/or power supply sequencing.

Soft Start

The LT1339 incorporates a soft start function that operates by slowly increasing the internal current limit. This limit is controlled by clamping the V_C node to a low voltage that climbs with time as an external capacitor on the SS pin is charged with about 8μA. This forces a graceful climb of output current capability, and thus a graceful increase in output voltage until steady-state regulation is achieved. The soft start timing capacitor is clamped to ground during shutdown and during undervoltage lockout, yielding a graceful output recovery from either condition.

5V Internal Reference

Power for the oscillator timing elements and most other internal LT1339 circuits is derived from an internal 5V reference, accessible at the $5V_{REF}$ pin. This supply pin can be loaded with up to 10mA DC (20mA pulsed) for convenient biasing of local elements such as control logic, etc.

Slope Compensation

For duty cycles greater than 50%, slope compensation is required to prevent current mode duty cycle instability in the regulator control loop. The LT1339 employs internal slope compensation that is adequate for most applications. However, if additional slope compensation is desired, it is available through the SL/ADJ pin. Excessive slope compensation will cause reduction in maximum load current capability and therefore is not desirable.

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R_{SENSE} Selection for Output Current

R_{SENSE} generates a voltage that is proportional to the inductor current for use by the LT1339 current sense amplifier. The value of R_{SENSE} is based on the required load current. The average current limit function has a typical threshold of 120mV/R_{SENSE}, or:

$$R_{SENSE} = 120mV/I_{LIMIT}$$

Operation with V_{SENSE} common mode voltage below 4.5V may slightly degrade current limit accuracy. See Average Current Limit Threshold Tolerance vs Common Mode Voltage curve in the Typical Performance Characteristics section for more information.

Output Voltage Programming

Output voltage is programmed through a resistor feedback network to V_{FB} (Pin 9) on the LT1339. This pin is the inverting input of the error amplifier, which is internally referenced to 1.25V. The divider is ratioed to provide 1.25V at the V_{FB} pin when the output is at its desired value.

The output voltage is thus set following the relation:

$$V_{OUT} = 1.25(1 + R2/R1)$$

when an external resistor divider is connected to the output as shown in Figure 1.

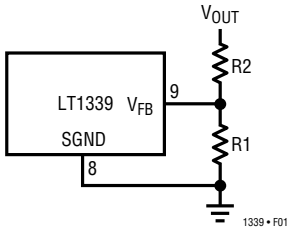

Figure 1. Programming LT1339 Output Voltage

If high value feedback resistors are used, the input bias current of the V_{FB} pin (1μA maximum) could cause a slight increase in output voltage. A Thevenin resistance at the V_{FB} pin of <5k is recommended.

Oscillator Components R_{CT} and C_{CT}

The LT1339 oscillator creates a modified sawtooth wave at its timing node (CT) with a slow charge, rapid discharge characteristic. The rapid discharge time corresponds to the minimum off-time of the PWM controller. This limits maximum duty cycle (DC_{MAX}) to:

$$DC_{MAX} = 1 - (t_{DISCH})(f_O)$$

This relation corresponds to the minimum value of the timing resistor (R_{CT}), which can be determined according to the following relation (R_{CT} vs DC_{MAX} graph appears in the Typical Performance Characteristics section):

$$R_{CT(MIN)} \approx [(0.8)(10^{-3})(1 - DC_{MAX})]^{-1}$$

Values for R_{CT} > 15k yield maximum duty cycles above 90%. Given a timing resistor value, the value of the timing capacitor (C_{CT}) can then be determined for desired operating frequency (f_O) using the relation:

$$C_{CT} \approx \frac{\left(1/f_O\right) - \left(100\right)\left(10^{-9}\right)}{\left(R_{CT}/1.85\right) + \frac{1.75}{\left(2.5\right)\left(10^{-3}\right) - \left(3.375/R_{CT}\right)}}$$

A plot of Operating Frequency vs R_{CT} and C_{CT} is shown in Figure 2. Typical 100kHz operational values are C_{CT} = 1000pF and R_{CT} = 16.9k.

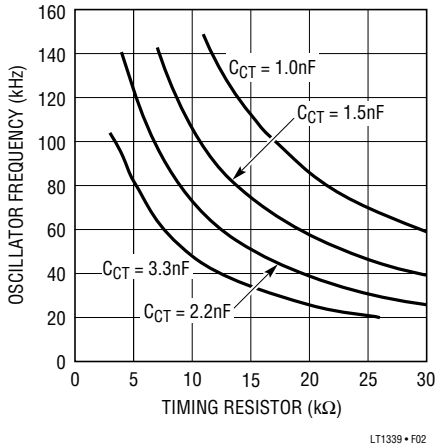

Figure 2. Oscillator Frequency vs R_{CT}, C_{CT}

Average Current Limit

The average current limit function is implemented using an external capacitor (C_{AVG}) connected from I_{AVG} to SGND that forms a single pole integrator with the 50kΩ output

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impedance of the I_{AVG} pin. The integrator corner frequency is typically set 1 to 2 orders of magnitude below the oscillator frequency and follows the relation:

$$f_{-3dB} = (3.2)(10^{-6})/C_{AVG}$$

The average current limit function can be disabled by shorting the I_{AVG} pin directly to SGND.

Soft Start Programming

The current control pin (V_C) limits sensed inductor current to zero at voltages less than a transistor V_{BE}, to full average current limit at $V_C = V_{BE} + 1.8V$. This generates a 1.8V full regulation range for average load current. An internal voltage clamp forces the V_C pin to a $V_{BE} – 100mV$ above the SS pin voltage. This 100mV "dead zone" assures 0% duty cycle operation at the start of the soft start cycle, or when the soft start pin is pulled to ground. Given the typical soft start current of 8μA and a soft start timing capacitor C_{SS}, the start-up delay time to full available average current will be:

$$t_{SS} = (1.5)(10^5)(C_{SS})$$

Boost Supply

The V_{BOOST} supply is bootstrapped via an external capacitor. This supply provides gate drive to the topside switch FET. The bootstrap capacitor is charged from $12V_{IN}$ through a diode when the switch node is pulled low.

The diode reverse breakdown voltage must be greater than $V_{IN} + 12V_{IN}$. The bootstrap capacitor should be at least 100 times greater than the total input capacitance of the topside FET. A capacitor in the range of 0.1μF to 1μF is generally adequate for most applications.

Shutdown Function—Input Undervoltage Detect and Threshold Hysteresis

The LT1339 RUN/SHDN pin uses a bandgap generated reference threshold of about 1.25V. This precision threshold allows use of the RUN/SHDN pin for both logic-level shutdown applications and analog monitoring applications such as power supply sequencing.

Because an LT1339 controlled converter is a power transfer device, a voltage that is lower than expected on the input supply could require currents that exceed the sourcing capabilities of that supply, causing the system to lock up in an undervoltage state. Input supply start-up protection can be achieved by enabling the RUN/SHDN pin using a resistor divider from the input supply to ground. Setting the divider output to 1.25V when that supply is almost fully enabled prevents the LT1339 regulator from drawing large currents until the input supply is able to provide the required power.

If additional hysteresis is desired for the enable function, an external feedback resistor can be used from the LT1339 regulator output. If connection to the regulator output is not desired, the $5V_{REF}$ internal supply pin can be used. Figure 3 shows a resistor connection on a 48V to 5V converter that yields a 40V V_{IN} start-up threshold for regulator enable and also provides about 10% input referred hysteresis.

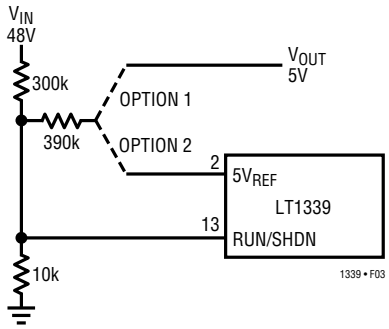

Figure 3. Input Supply Sequencing Programming

The shutdown function can be disabled by connecting the RUN/SHDN pin to the $12V_{IN}$ rail. This pin is internally clamped to 2.5V through a 20k series input resistance and will therefore draw about 0.5mA when tied directly to 12V. This additional current can be minimized by making the connection through an external resistor (100k is typically used).

Inductor Selection

The inductor for an LT1339 converter is selected based on output power, operating frequency and efficiency requirements. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (ΔI). For a buck converter, the minimum inductor value for a desired maximum operating ripple current can be determined using the following relation:

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$$L_{MIN} = \frac{(V_{OUT})(V_{IN} - V_{OUT})}{(\Delta I)(f_O)(V_{IN})}$$

where f_O = operating frequency. Given an inductor value (L), the peak inductor current is the sum of the average inductor current (I_{AVG})and half the inductor ripple current (ΔI), or:

$$I_{PK} = I_{AVG} + \frac{(V_{OUT})(V_{IN} - V_{OUT})}{(2)(L)(f_O)(V_{IN})}$$

The inductor core type is determined by peak current and efficiency requirements. The inductor core must withstand peak current without saturating, and series winding resistance and core losses should be kept as small as is practical to maximize conversion efficiency.

The LT1339 peak current limit threshold is 40% greater than the average current limit threshold. Slope compensation effects reduce this margin as duty cycle increases. This margin must be maintained to prevent peak current limit from corrupting the programmed value for average current limit. Programming the peak ripple current to less than 15% of the desired average current limit value will assure porper operation of the average current limit feature through 90% duty cycle (see Slope Compensation section).

Oscillator Synchronization

The LT1339 oscillator generates a modified sawtooth waveform at the C_T pin between low and high thresholds of about 0.8V (vl) and 2.5V (vh) respectively. The oscillator can be synchronized by driving a TTL level pulse into the SYNC pin. This inputs to a one-shot circuit that reduces the oscillator high threshold to 2V for about 200ns. The SYNC input signal should have minimum high/low times of ≥1µs.

Slope Compensation

Current mode switching regulators that operate with a duty cycle greater than 50% and have continuous inductor current can exhibit duty cycle instability. While a regulator will not be damaged and may even continue to function

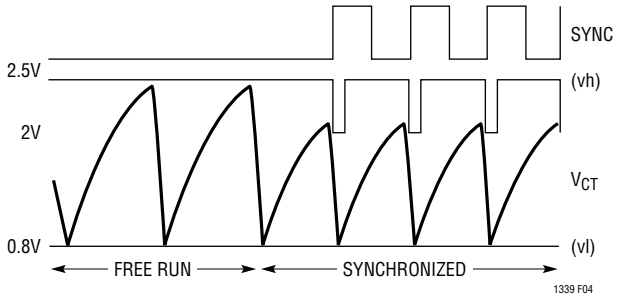

Figure 4. Free Run and Synchronized Oscillator Waveforms (at C_T Pin)

acceptably during this type of subharmonic oscillation, an irritating high-pitched squeal is usually produced.

The criterion for current mode duty cycle instability is met when the increasing slope of the inductor ripple current is less than the decreasing slope, which is the case at duty cycles greater than 50%. This condition is illustrated in Figure 5a. The inductor ripple current starts at I_1, at the beginning of each oscillator switch cycle. Current increases at a rate S1 until the current reaches the control trip level I_2. The controller servo loop then disables the main switch (and enables the synchronous switch) and inductor current begins to decrease at a rate S2. If the current switch point (I_2) is perturbed slightly and increased by ΔI, the cycle time ends such that the minimum current point is increased by a factor of (1 + S2/S1) to start the next cycle. On each successive cycle, this error is multiplied by a factor of S2/S1. Therefore, if S2/S1 is ≥ 1, the system is unstable.

Subharmonic oscillations can be eliminated by augmenting the increasing ripple current slope (S1) in the control loop. This is accomplished by adding an artificial ramp on the inductor current waveform internal to the IC (with a slope S_X) as shown in Figure 5b. If the sum of the slopes S1 + S_X is greater than S2, the condition for subharmonic oscillation no longer exists.

For a buck converter, the required additional current waveform slope, or "Slope Compensation," follows the relation:

$$S_X \geq \left(\frac{V_{IN}}{L}\right)(2DC - 1)$$

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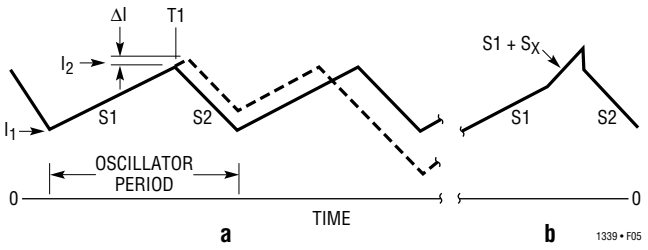

Figure 5. Inductor Current at DC > 50% and Slope Compensation Adjusted Signal

For duty cycles less than 50% (DC < 0.5), S_X is negative and is not required. For duty cycles greater than 50%, S_X takes on values dependent on S1 and duty cycle. This leads to a minimum inductance requirement for a given V_{IN} and duty cycle of:

$$L_{MIN} = \left(\frac{V_{IN}}{S_X}\right)(2DC - 1)$$

The LT1339 contains an internal S_X slope compensation ramp that has an equivalent current referred value of:

$$0.084\left(\frac{f_O}{R_{SENSE}}\right) \quad \text{Amp/s}$$

where f_O is oscillator frequency. This yields a minimum inductance requirement of:

$$L_{MIN} \geq \frac{(V_{IN})(R_{SENSE})(2DC - 1)}{(0.084)(f_O)}$$

A down side of slope compensation is that, since the IC servo loop senses an increase in perceived inductor current, the internal current limit functions are affected such that the maximum current capability of a regulator is reduced by the same amount as the effective current referred slope compensation. The LT1339, however, uses a current limit scheme that is independent of slope compensation effects (average current limit). This provides operation at any duty cycle with no reduction in current sourcing capability, provided ripple current peak amplitude is less than 15% of the current limit value. For example, if the supply is set up to current limit at 10A, as long as the peak inductor current is less than 11.5A, duty cycles up to 90% can be achieved without compromising the average current limit value.

If an inductor smaller than the minimum required for internal slope compensation (calculated above as L_{MIN}) is desired, additional slope compensation is required. The LT1339 provides this capability through the SL/ADJ pin. This feature is implemented by referencing this pin via a resistor divider from the $5V_{REF}$ pin to ground. The additional slope compensation will be affected at the point in the oscillator waveform (at pin CT) corresponding to the voltage set by the resistor divider. Additional slope compensation can be calculated using the relation:

$$S_{XADD} = \frac{(2500)(f_O)}{(R_{EQ})(R_{SENSE})} \quad \text{Amp/s}$$

where R_{EQ} is the effective resistance of the resistor divider. Actual compensation will be somewhat greater due to internal curvature correction circuitry that imposes an exponential increase in the slope compensation waveform, further increasing the effective compensation slope up to 20% for a given setting.

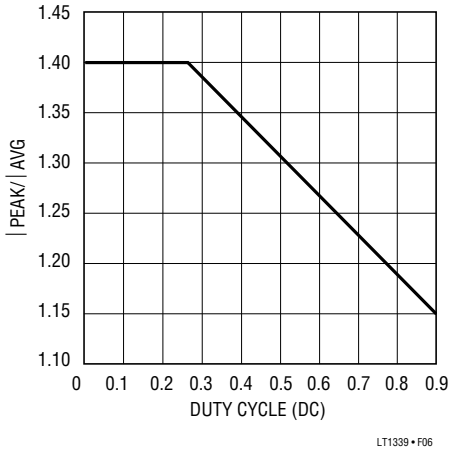

Figure 6. Maximum Ripple Current (Normalized) vs Duty Cycle for Average Current Limit

Design Example:

V_{IN} = 20V
V_{OUT} = 15V (DC = 0.75)
R_{SENSE} = 0.01Ω
f_O = 100kHz
L = 5μH

The minimum inductor usable with no additional slope compensation is:

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$$L_{MIN} \geq \frac{(20V)(0.01\Omega)(1.5-1)}{(0.084)(100000)} = 11.9\mu H$$

Since L = 5µH is less than L_{MIN}, additional slope compensation is necessary. The total slope compensation required is:

$$S_X \geq \left(\frac{20V}{5\mu H}\right)(1.5-1) = (2)(10^6) \quad \text{Amp/s}$$

Subtracting the internally generated slope compensation and solving for the required effective resistance at SL/ADJ yields:

$$R_{EQ} \leq \frac{(2500)(f_O)}{(2)(10^6)(R_{SENSE}) - (0.084)(f_O)} = 21.5k$$

Setting the resistor divider reference voltage at 2V assures that the additional compensation waveform will be enabled at 75% duty cycle. As shown in Figure 7a, using

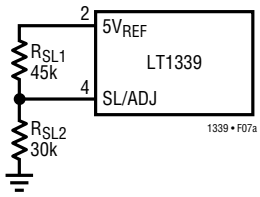

Figure 7a. External Slope Compensation Resistors

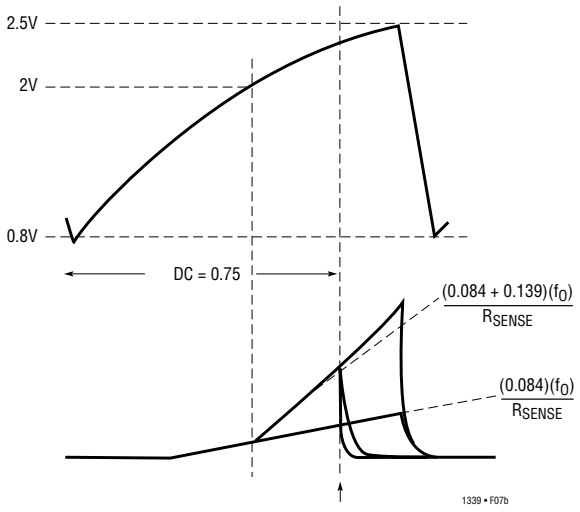

Figure 7b. Slope Compensation Waveforms

R_{SL1} = 45k and R_{SL2} = 30k sets the desired reference voltage and has a R_{EQ} of 18k, which meets both design requirements. Figure 7b shows the slope compensation effective waveforms both with and without the SL/ADJ external resistors.

Power MOSFET and Catch Diode Selection

External N-channel MOSFET switches are used with the LT1339. The positive gate-source drive voltage of the LT1339 for both switches is roughly equivalent to the $12V_{IN}$ supply voltage, so standard threshold MOSFETs can be used.

Selection criteria for the power MOSFETs include the "ON" resistance ($R_{DS(ON)}$), reverse transfer capacitance (C_{RSS}), maximum drain-source voltage (V_{DSS}) and maximum output current.

The power FETs selected must have a maximum operating V_{DSS} exceeding the maximum V_{IN}. V_{GS} voltage maximum must exceed the $12V_{IN}$ supply voltage.

Once voltage requirements have been determined, $R_{DS(ON)}$ can be selected based on allowable power dissipation and required output current.

In an LT1339 buck converter, the average inductor current is equal to the DC load current. The average currents through the main and synchronous switches are:

$$I_{MAIN} = (I_{LOAD})(DC)$$

$$I_{SYNC} = (I_{LOAD})(1 - DC)$$

The $R_{DS(ON)}$ required for a given conduction loss can be calculated using the relation:

$$P_{LOSS} = (I_{SWITCH})^2(R_{DS(ON)})$$

In high voltage applications (V_{IN} > 20V), the topside switch is required to slew very large voltages. As V_{IN} increases, transition losses increase through a square relation, until it becomes the dominant power loss term in the main switch. This transition loss takes the form:

$$P_{TR} \approx (k)(V_{IN})^2(I_{MAX})(C_{RSS})(f_O)$$

where k is a constant inversely related to the gate drive current, approximated by k = 2 in LT1339 applications.

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The maximum power loss terms for the switches are thus:

$$P_{MAIN} = (DC)(I_{MAX})^2(1 + \delta)(R_{DS(ON)}) + 2(V_{IN})^2(I_{MAX})(C_{RSS})(f_O)$$

$$P_{SYNC} = (1 - DC)(I_{MAX})^2(1 + \delta)(R_{DS(ON)})$$

The $(1 + \delta)$ term in the above relations is the temperature dependency of $R_{DS(ON)}$, typically given in the form of a normalized $R_{DS(ON)}$ vs Temperature curve in a MOSFET data sheet.

In some applications, parasitic FET capacitances couple the negative going switch node transient onto the bottom gate drive pin of the LT1339, causing a negative voltage in excess of the Absolute Maximum Rating to be imposed on that pin. Connection of a catch Schottky (rated to about 1A is typically sufficient) from this pin to ground will eliminate this effect.

C_{IN} and C_{OUT} Supply Decoupling Capacitor Selection

The large currents typical of LT1339 applications require special consideration for the converter input and output supply decoupling capacitors. Under normal steady state operation, the source current of the main switch MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. Most of this current is provided by the input bypass capacitor. To prevent large input voltage transients and avoid bypass capacitor heating, a low ESR input capacitor sized for the maximum RMS current must be used. This maximum capacitor RMS current follows the relation:

$$I_{RMS} \approx \frac{(I_{MAX})(V_{OUT}(V_{IN} - V_{OUT}))^{1/2}}{V_{IN}}$$

which peaks at a 50% duty cycle, when $I_{RMS} = I_{MAX}/2$. Capacitor ripple current ratings are often based on only 2000 hours (three months) lifetime; it is advisable to derate either the ESR or temperature rating of the capacitor for increased MTBF of the regulator.

The output capacitor in a buck converter generally has much less ripple current than the input capacitor. Peak-to-peak ripple current is equal to that in the inductor (ΔI_L), typically a fraction of the load current. C_{OUT} is selected to reduce output voltage ripple to a desirable value given an expected output ripple current. Output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L\{ESR + [(4)(f_O) \bullet C_{OUT}]^{-1}\}$$

where f_O = operating frequency.

Efficiency Considerations and Heat Dissipation

High output power applications have inherent concerns regarding power dissipation in converter components. Although high efficiencies are achieved using the LT1339, the power dissipated in the converter climbs to relatively high values when the load draws large amounts of power. Even at 90% efficiency, an application that provides 500W to the load has conversion loss of 55W.

I^2R dissipation through the switches, sense resistor and inductor series resistance create substantial losses under high currents. Generally, the dominant I^2R loss is evident in the FET switches. Loss in each switch is proportional to the conduction time of that switch. For example, in a 48V to 5V converter the synchronous FET conducts load current for almost 90% of the cycle time and thus, requires greater consideration for dissipating I^2R power.

Gate charge/discharge current creates additional current drain on the 12V supply. If powered from a high voltage input through a linear regulator, the losses in that regulator device can become significant. A supply solution bootstrapped from the output would draw current from a lower voltage source and reduce this loss component.

Transition losses are significant in the topside switch FET when high V_{IN} voltages are used. Transition losses can be estimated as:

$$P_{TLOSS} \approx 2(V_{IN})^2(I_{MAX})(C_{RSS})(f_O)$$

Since the conduction time in the main switch of a 48V to 5V converter is small, the I^2R loss in the main switch FET is also small. However, since the FET gate must switch up past the 48V input voltage, transition loss can become a significant factor. In such a case, it is often prudent to take the increased I^2R loss of a smaller FET in order to reduce C_{RSS} and thus, the associated transition losses.

Gate Drive Buffers

The LT1339 is designed to drive relatively large capacitive loads. However, in certain applications, efficiency improvements can be realized by adding an external buffer stage to drive the gates of the FET switches. When the

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switch gates load the driver outputs such that rise/fall times exceed about 100ns, buffers can sometimes result in efficiency gains. Buffers also reduce the effect of back injection into the bottom side driver output due to coupling of switch node transitions through the switch FET C_{MILLER}.

Paying the Physicists

In high power synchronous buck configurations, certain physical characteristics of the external MOSFET switches can impact conversion efficiency. As the input voltage approaches about 30V, the bottom MOSFETs will begin to exhibit "phantom turn-on." This phenomenon is caused by coupling of the instantaneous voltage step on the bottom side switch drain through C_{MILLER} to the device gate, yielding internal localized gate-source voltages above the turn-on threshold of the FET. This generates a shoot-through blip that ultimately eats away at efficiency numbers. In Figure 8 a negative prebias circuit is added to the bottom side gate. The addition of this ~3V of negative offset to the bottom gate drive provides additional off-state voltage range to prevent phantom turn-on.

This type of prebias circuit is used in the 48V to 5V, 50A converter pictured in the Typical Applications section.

As currents increase beyond the 10A to 15A range, the bottom side FET body diode experiences hard turn-on during switch dead time due to local current loop inductance preventing the timely transfer of charge to the Schottky catch diode. The charge current required to commutate this body diode creates a high dV/dt Schottky avalanche when the diode charge is finally exhausted (due to an effective inductor current discontinuity at the moment the body diode no longer requires charge). This generates an increased turn-on power burst in the topside switch, causing additional conversion efficiency loss. This effect of this parasitic inductance can be reduced by using *FETKEY*™ MOSFETs, which have parallel catch Schottky diodes internal to their packages. *FETKEY* MOSFETs are

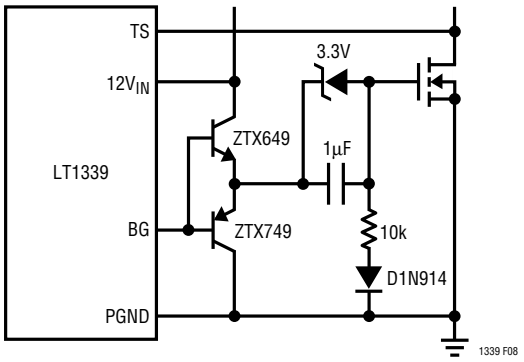


Figure 8. Bottom Side Driver Negative Prebias Circuit

not available for high voltages, so as input voltage continues to increase, they can no longer be used. Because this necessitates the use of discrete FETs and Schottkys, interdigitation of a number of smaller devices is required to minimize parasitic inductances. This technique is also used in the 48V to 5V, 50A converter shown in the Typical Applications section.

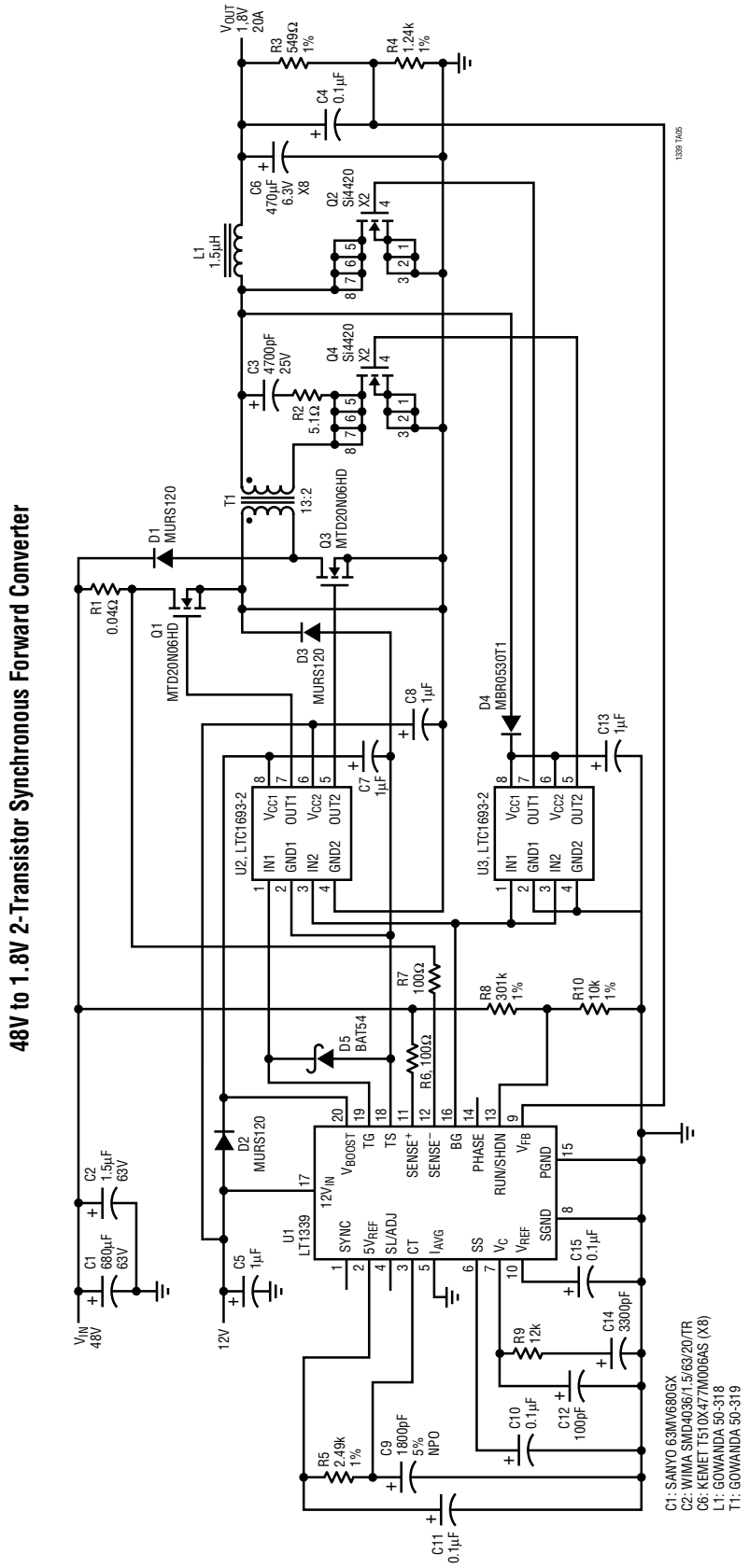
Optimizing Transient Response—Compensation Component Values

The dominant compensation point for an LT1339 converter is the V_C pin (Pin 7), or error amplifier output. This pin is connected to a series RC network, R_{VC} and C_{VC}. The infinite permutations of input/output filtering, capacitor ESR, input voltage, load current, etc. make for an empirical method of optimizing loop response for a specific set of conditions.

Loop response can be observed by injecting a step change in load current. This can be achieved by using a switchable load. With the load switching, the transient response of the output voltage can be observed with an oscilloscope. Iterating through RC combinations will yield optimized response. Refer to LTC Application Note 19 in *1990 Linear Applications Handbook, Volume 1* for more information.

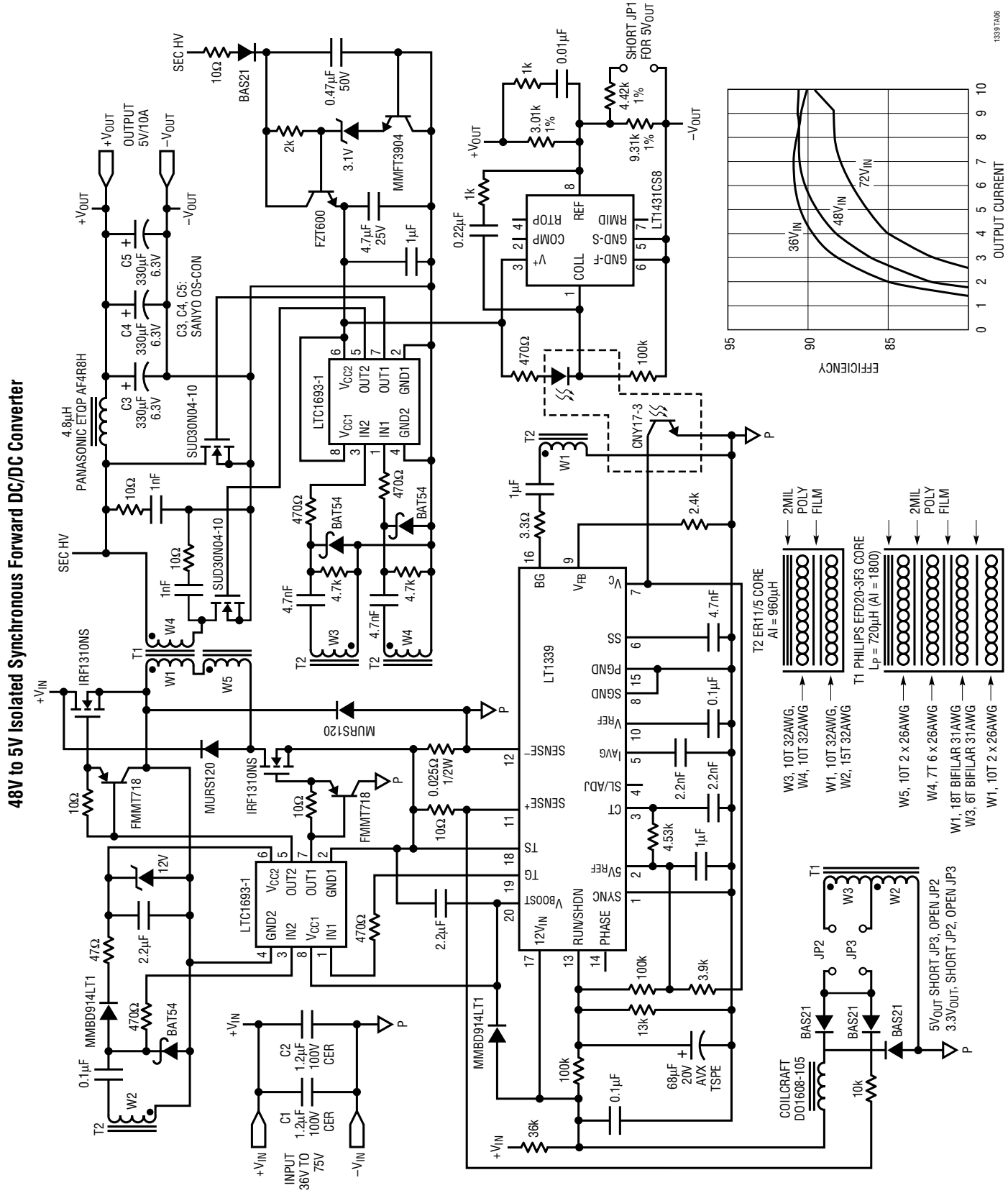
FETKEY is a trademark of International Rectifier Corporation.

TYPICAL APPLICATIONS



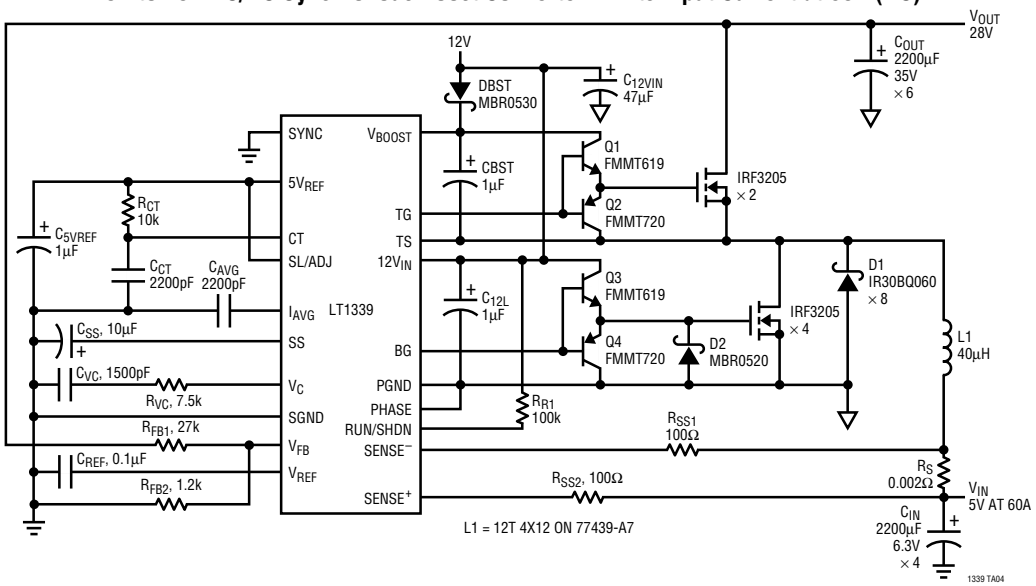
TYPICAL APPLICATIONS

48V to 5V Isolated Synchronous Forward DC/DC Converter



TYPICAL APPLICATIONS

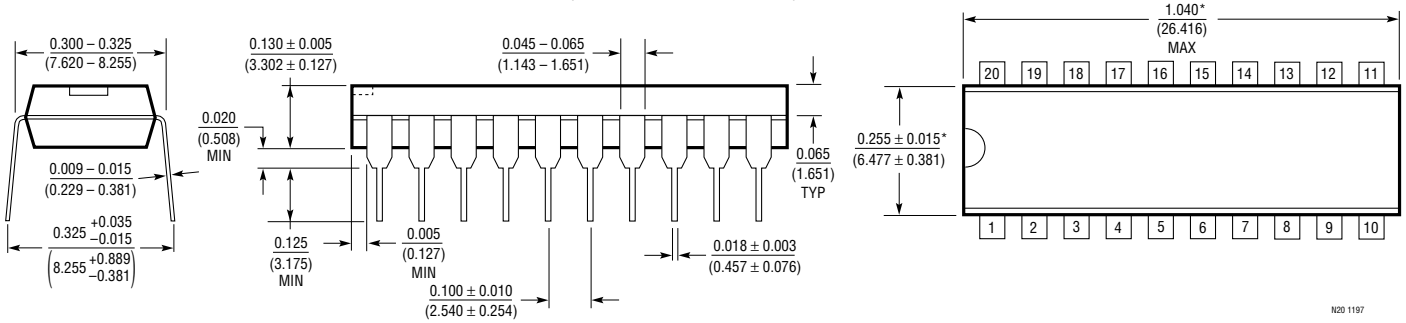
5V to 28V DC/DC Synchronous Boost Converter Limits Input Current at 60A (DC)



PACKAGE DESCRIPTION

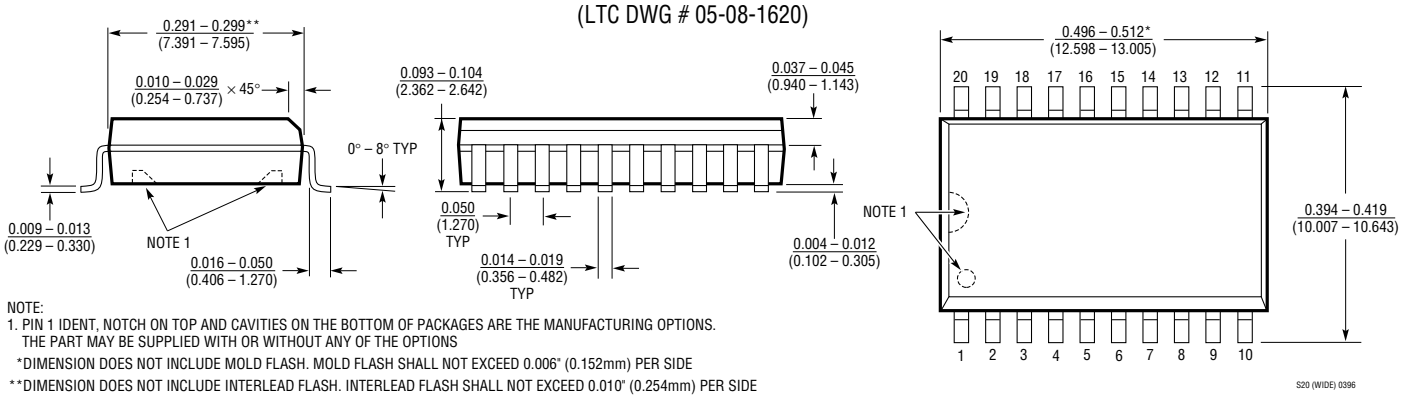
Dimensions in inches (millimeters) unless otherwise noted.

N Package
20-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

SW Package
20-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)



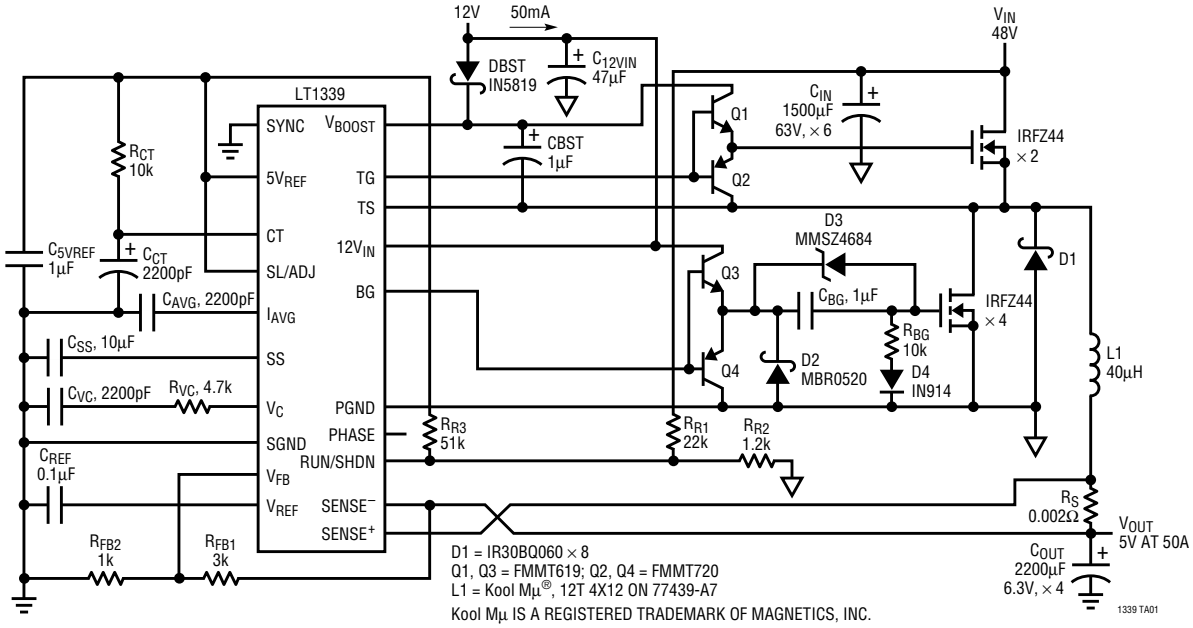
NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

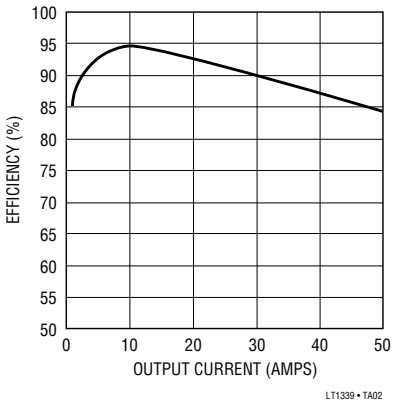
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

48V to 5V 50A DC/DC Converter with Input Supply Start-Up Protection



48V to 5V Efficiency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1158	Half-Bridge N-Channel MOSFET Driver	Current Limit Protection, 100% of Duty Cycle
LT1160	Half-Bridge N-Channel MOSFET Driver	Up to 60V Input Supply, No Shoot-Through
LT1162	Dual Half-Bridge N-Channel MOSFET Driver	V_{IN} to 60V, Good for Full-Bridge Applications
LT1336	Half-Bridge N-Channel MOSFET Driver	Smooth Operation at High Duty Cycle (95% to 100%)
LTC®1530	High Power Step-Down Switching Regulator Controller	Excellent for 5V to 3.xV Up to 50A
LTC1435A	High Efficiency, Low Noise Current Mode Step-Down DC/DC Converter	Drives Synchronous N-Channel MOSFETs
LTC1438	Dual High Efficiency, Low Noise Synchronous Step-Down Controller	Tight 1% Reference
LT1680	High Power DC/DC Current Mode Step-Up Controller	High Side Current Sense, Up to 60V Input

EXPANDED PIN DESCRIPTIONS

SYNC (PIN 1) OSCILLATOR SYNCHRONIZATION PIN

This pin allows the user to synchronize the LT1339 to an external clock.

The synchronized frequency must be faster than the free-running frequency of the LT1339. This logic-level input can be driven from TTL or 3.3V or 5V CMOS. Its threshold is set at $2.2V_{BE}$, about 1.5V, and it exhibits no hysteresis. Its duty factor can be almost anything, but you must ensure that the pulse is at least 500ns wide, whether asserted high or low. The internal synchronization event is triggered on the rising edge of the SYNC pulse; this event triggers an internal 200ns one-shot. While the output of the internal one-shot is asserted, the high level trip point of the CT pin is reduced from 2.5V to 2V (see Figure 3).

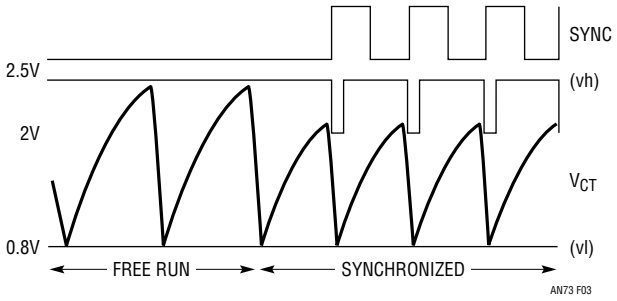


Figure 3. Free Run and Synchronized Oscillator Waveforms (at Pin CT)

If, during the 200ns at the output of the internal one-shot, the ramp voltage on the CT pin is above 2V, an early reset is initiated. Normal reset is initiated at 2.5V. The functions performed by the reset event are:

1. The CT pin (Pin 3) is discharged by the LT1339 to 0.8V
2. The beginning of a new on cycle ensues (the top gate goes high in buck mode or the bottom gate goes high in boost mode, depending on the logic level of the PHASE pin).

The SYNC pin is used to pull the oscillator frequency up from the free-running frequency set by R_{CT} and C_{CT}, so the free-running frequency should be set low enough (20% lower than the desired running frequency) to ensure synchronization. If unused, this pin should be tied either to SGND or to $5V_{REF}$, the latter having a penalty of an additional 1mA of quiescent operating current. Leaving this pin floating is bad form. If this pin is to be driven from 12V or 15V logic, a resistor divider is recommended, as shown in Figure 4.

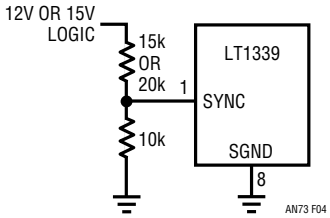


Figure 4. Synchronizing from Higher Voltage Logic Families

Pulling the SYNC pin above $5V_{REF}$ by a diode drop forward biases an internal diode which begins to source current into $5V_{REF}$, which has no provision to sink current. This is not recommended.

SYNCHRONIZING MULTIPLE LT1339s

There are two basic schemes to synchronize multiple power converters: master/slave synchronization and multiphase synchronization.

Master/Slave Synchronization

In master/slave synchronization, one LT1339 (the master) is set to free-run at the frequency desired for the whole system and the other LT1339(s) are slaved from the master. Figure 5 details the master/slave connection. The free-running frequencies of the slaves are set 20% lower than the free-running frequency of the master. In such a system, if the master LT1339 stops switching (shuts down) the slaves free-run at their natural frequency until the master resumes switching.

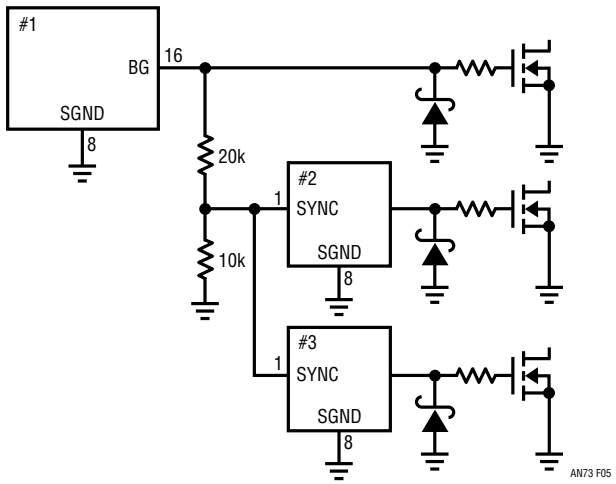


Figure 5. Master/Slave Synchronization

Multiphase Synchronization

Multiphase synchronization is very useful in systems where high ripple current mandates massive input capacitors in a buck or forward regulator, or massive output capacitors in a boost regulator. Refer to Figure 6. The master oscillator (U1) is set to run at *n* times the desired running frequency, where *n* is the number of phases desired. Select the subcircuit of U2 that matches the number of phases you desire (or make more phases by looking up the 4017 data sheet and choosing additional [up to ten] phases). Simply connect the sync outputs of Figure 6 to the SYNC pins of the respective LT1339s. Set up the LT1339s to free-run 20% slower than the synchronizing frequency, f_{OSC}/n.

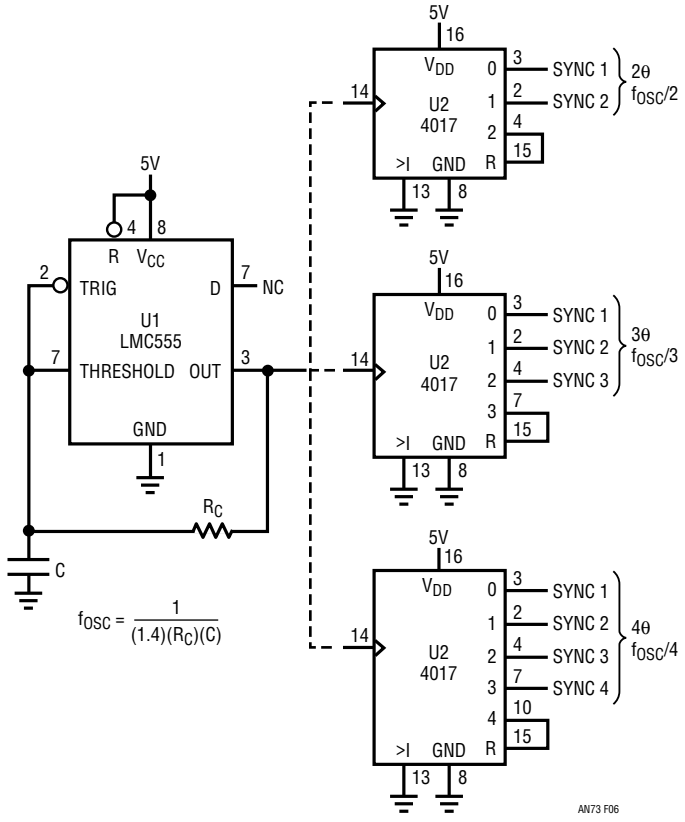


Figure 6. Mulitphase Synchronization

Wide-Range Synchronization

The LT1339 oscillator can be synchronized over a wider frequency range by acting directly on the CT pin. This can be done by pulling the CT pin above 2.5V; this sets an internal flip-flop, which, while set, keeps the LT1339 in the deadtime phase of operation. The deadtime phase is maintained until the CT pin is brought down to 0.8V. During the dead-time phase, the LT1339 enters and remains in the following state:

1. The main transistor (top FET of buck, bottom FET of boost) is off.
2. The synchronous transistor (bottom FET of buck, top FET of boost) is on.
3. A 2.5mA current source is discharging the CT pin.

The LT1339 will stay in this state as long as the CT pin is held above 0.8V.

When the CT pin is released, the internal discharge current (2.5mA) will pull it down to 0.8V, the internal flip-flop is reset and the next on cycle begins:

1. The synchronous transistor is turned off
2. The main transistor is turned on.
3. The 2.5mA discharge current is switched off.

Refer to Figure 7. This synchronization scheme has the advantage of allowing synchronization over the full operating range of the LT1339, but has the disadvantage of disabling the slope compensation. Due to the internal structures of the LT1339, the CT pin should not be pulled above 3.5V; doing so may seriously confuse the internal logic.

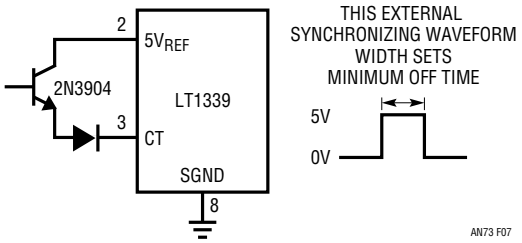


Figure 7. Wide-Range Synchronization Using the CT Pin

$5V_{REF}$ (PIN 2) OUTPUT REFERENCE

This is *your* reference, the reference to power your external logic, amplifiers and the supply to tailor the inputs of the LT1339 to your needs—it is 5V ±250mV over line, load and temperature. You can draw up to 10mA

from this pin. Sourcing current into this pin is not recommended because it has no pull-down capability other than the normal operating current of the logic of the LT1339. It is used as the reference for the oscillator section through R_T. To set up hysteresis for the RUN pin, connect an appropriate resistor from the RUN pin to the $5V_{REF}$ pin. Finally, the $5V_{REF}$ pin is used with the SL/ADJ pin to set the maximum duty factor or additional slope compensation when needed. Internally, the $5V_{REF}$ pin is used to power practically all internal functions, with only the RUN/SHDN comparator and both gate drive circuits powered from other sources. This pin should be decoupled to ground (SGND) with a 1µF capacitor having an ESR less than 10Ω. The decoupling capacitor can be anything from 0.1µF to many thousands of microfarads.

CT (PIN 3) OSCILLATOR TIMING PIN

The free-running (nonsynchronized) frequency of the LT1339 is set up by the R_{CT} and C_{CT} combination connected to this pin (see Figure 8). The value of the resistor R_{CT} sets up the minimum off-time of the LT1339. Refer to Figure 9 for duty factor verses R_{CT} in kΩ. If you would like

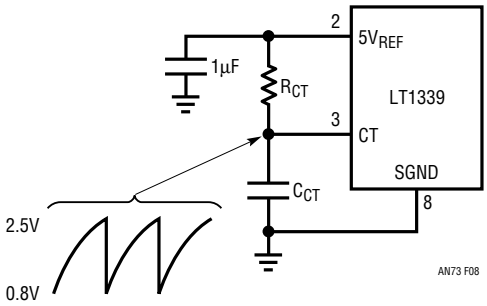


Figure 8. Oscillator Pin Connection + Waveform

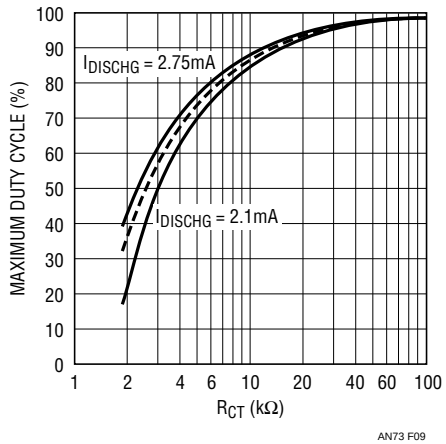


Figure 9. Duty Factor vs R_{CT}

to limit maximum duty factor to a number less than 90%, a better way to do so is described in the SL/ADJ (Pin 4) pin description.

Figure 10 shows the Oscillator Frequency vs R_{CT} and C_{CT}.

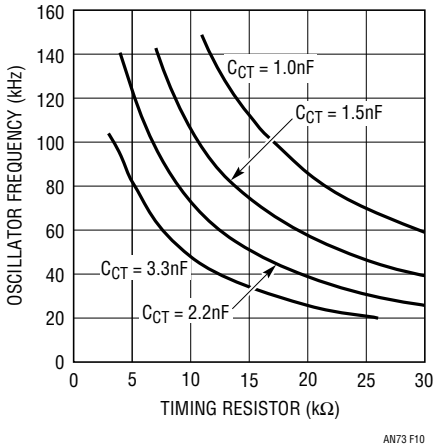


Figure 10. Oscillator Frequency vs R_{CT}, C_{CT}

SL/ADJ (PIN 4) SLOPE COMPENSATION ADJUSTMENT PIN

This pin is used to limit maximum duty factor and/or introduce additional slope compensation to the LT1339.

Limiting Maximum Duty Factor

Figure 11 details how to use the SL/ADJ pin to limit maximum duty factor. Limiting the maximum duty factor effectively limits the voltage input-to-output ratio where the converter can transform power. If you think of the converter as a DC variac, limiting the duty factor limits how far the variac can be turned. What function limiting duty factor performs depends upon the topology used:

1. In a synchronous buck converter, decreasing the maximum duty factor increases the dropout voltage. This could be used to set the minimum input voltage at which a given output voltage can be reached. It also limits the load-step response time when at the lowest input voltage.
2. In a synchronous boost converter, decreasing the maximum duty factor decreases the maximum available output voltage at a given input voltage. This could be used as an overvoltage protection default. Limiting duty factor can also affect the load step response time when operating at the minimum input voltage.

3. In a forward converter, decreasing the maximum duty factor is highly desirable because it prevents transformer core saturation, resulting in a robust design.
4. In all topologies, limiting the maximum duty factor can be used to prevent operation at duty factors at which the circuit would experience current mode instability, but this function is better performed by setting the UV lockout voltage appropriately.

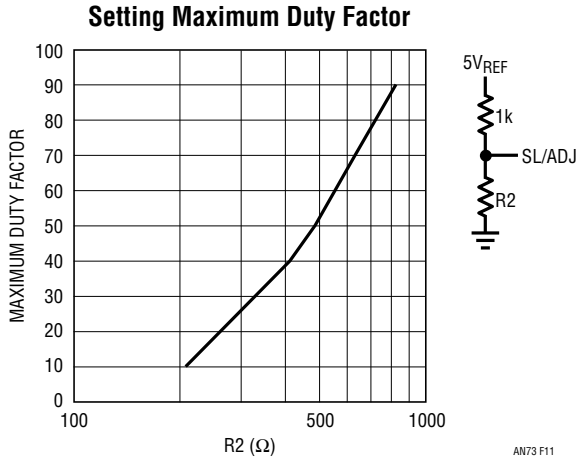


Figure 11. Using the Slope Comp Pin to Limit Duty Factor

Adding More Slope Compensation

At duty factors greater than 50%, an instability enters the current mode switcher world: current mode instability. This is seen as a two-cycle sequence: first, a cycle with a long on-time and short off-time, then a cycle with a short on-time and a long off-time. Current mode instability *always* happens at exactly half of the switching frequency and is completely independent of other forms of subharmonic oscillation. Current mode instability is independent of the control loop and can be observed when a voltage source is substituted for the control loop. Current mode instability occurs whenever the rising main inductor current ramp is slower than the falling main inductor current ramp. To make a design that can run at duty factors approaching unity, slope compensation is a must. The LT1339 has built-in slope compensation that is adequate for most buck converter designs, but if you have a boost converter running at very high duty factors, you may need more slope compensation.

If your system exhibits current mode instability, you will need to add slope compensation or increase the inductance of the main inductor. For the procedure to calculate the correct value for the main inductor, refer to the section entitled "Boost," or "Buck", according to which topology you have, and look up the "Inductor Selection" subsection. To add slope compensation to your existing design, use this procedure:

1. By varying V_{IN}, measure the minimum duty factor at which current mode instability occurs. If the duty factor is 50% or less, you are not looking at current mode instability; check loop stability.
2. Construct the subcircuit shown in Figure 12 and connect it to your switcher.

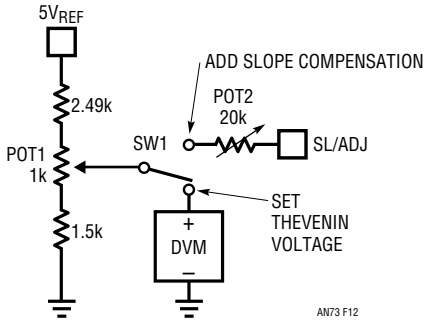


Figure 12. Slope Compensation Adjustment Setup Circuit

3. Power up and switch SW1 to the "set Thevenin voltage" position.
4. Select a Thevenin voltage from Table 1 that corresponds to a duty factor that is 10% less than you found in step 1.

Table 1. Thevinin Voltages for Slope Compensation

DF	$V_{THEVININ}$
90%	2.37
80%	2.23
70%	2.09
60%	1.922
50%	1.744

5. Adjust POT1 for that Thevenin voltage, as read on the DVM.
6. Adjust POT2 for maximum resistance and set SW1 for "Add slope compensation."

7. Decrease the resistance of POT2 to correct the current mode instability at the minimum input voltage and maximum load current allowed.
8. Calculate from the equations in Figure 13 the resistor values needed to construct the slope-compensation network shown in Figure 14.

$$R_{THEV} = \frac{1}{\left[\frac{1}{(V_{THEV}/5V)(4k)}\right] + \left[\frac{1}{(5V - V_{THEV})/(5V)(4k)}\right]}$$

$$R_{SELECT} = \left(R_{POT2}\right)\left(0.8\right) \quad \text{(Margin)}$$

$$R_{TOTAL} = R_{THEV} + R_{SELECT}$$

$$R_{TOP} = \frac{(R_{TOTAL})(5)}{V_{THEV}}$$

$$R_{BOTTOM} = \frac{(R_{TOTAL})(5)}{5 - V_{THEV}}$$

Figure 13. Calculating the Resistor Values for a 2-Resistor Slope Compensation Network

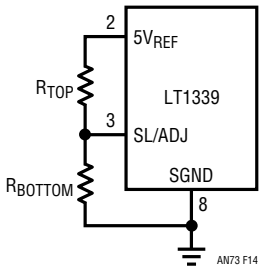


Figure 14. Two Resistor Slope Compensation

For the new design, refer to the "Inductor Selection" subsection of the section describing the topology you are designing.

The slope compensation in your system need only be enough to handle the steady-state operation at minimum V_{IN} with maximum V_{OUT} and maximum load current (UV lockout can be set to limit minimum input voltage and I_{RSENSE} can be set to limit maximum current). If the converter is stable in steady-state operation, it will also be free from current mode instability during load-step-induced duty factor variations.

I_{AVE} (PIN 5) AVERAGE CURRENT LOOP INTEGRATION CAPACITOR

This pin is used to smooth out the triangular wave shape of the current waveform and, in the process, to set up the loop compensation of the current limit loop. In the buck or boost converter, the current waveform in the inductor of the power converter is roughly triangular, the average of which represents the DC output current of the buck converter (DC input current for a boost converter). This main inductor current is converted into a voltage by the current sense resistor. The voltage across the sense resistor is applied to the $SENSE^-$ and $SENSE^+$ pins of the LT1339. Inside, it is amplified by a gain of 15 and is then offset by a V_{BE} so that 700mV represents zero programmed peak inductor current. This current signal representing inductor current is then given an impedance of 50k and brought out to the I_{AVE} pin. Placing a capacitor from the I_{AVE} pin to the V_C pin (Pin 7), sets up an integration network that smooths out the triangular ripple, yielding a DC voltage that represents the average current. This DC voltage is subtracted from 2.5V and converted to a current by a transconductance amplifier. If the resultant current is negative, it is subtracted from the error amplifier's output current. The transconductance of the conversion is 0.03A/V. Once the current reaches its threshold, the average current limit loop comes to life, taking control of the main control loop. The power converter changes from a constant voltage source to a constant current source. If the average current limit feature is not used, this pin should be grounded.

Using the I_{AVE} Pin to Implement an Adjustable Current Limit.

Refer to Figure 15. This circuit is a system-level application using the LT1339 where there is a motherboard that uses one-half of the available power and two daughter boards that, when present, each use one-quarter of the total available power. Using this circuit, one can protect the motherboard and daughterboards with current limits set appropriately for the actual load.

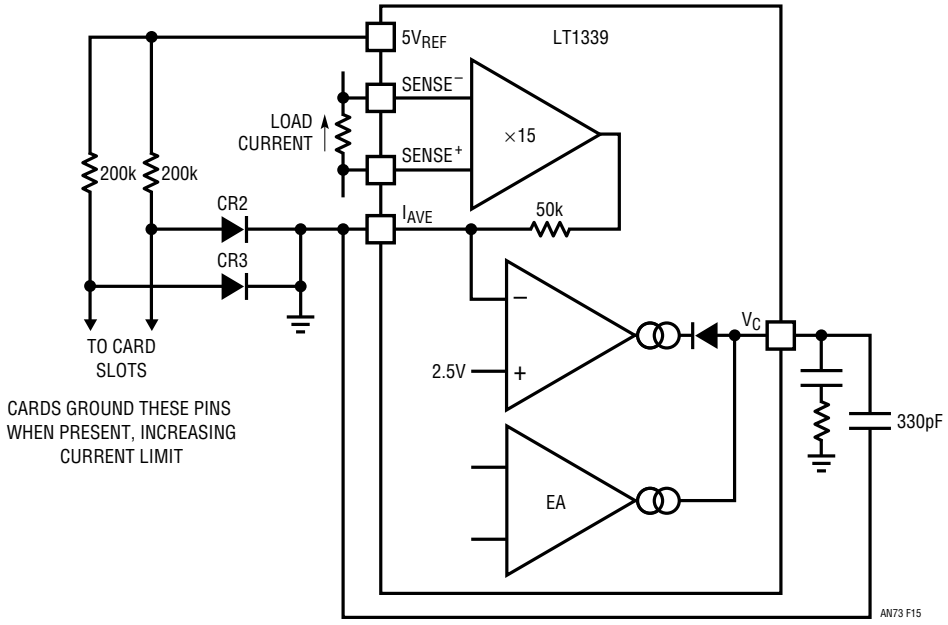
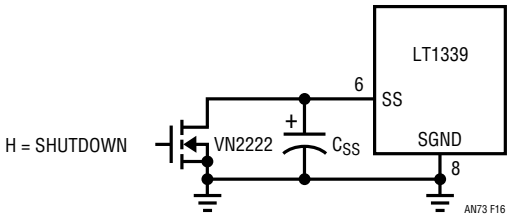


Figure 15. Multiple Level Automatic Current Limit

SS (PIN 6) SOFT-START INTEGRATION CAPACITOR

This pin, with its associated external capacitor, generates a ramp that limits the maximum voltage possible on the V_C pin. The V_C pin is clamped by a PNP transistor to be $1V_{BE}$ (~0.7V) maximum above the SS pin. This allows the current output of the power converter to start at zero and rise to the operating load current at a rate slower than the loop response. Soft-start ramps minimize or completely eliminate overshoot at turn-on. This pin is actively pulled to ground when either the $12V_{IN}$ pin voltage drops below the UV lockout point, disabling operation (see the section on the $12V_{IN}$ pin for details), or the RUN/SHDN pin is below its low voltage trip point (see the section on the RUN/SHDN pin for details). When the voltages on both the $12V_{IN}$ and the RUN/SHDN pins enable operation, approximately 8µA is sourced out of this pin, charging C_{SS}, the capacitor connected between ground and this pin. This current can vary from 4µA to 20µA. For tighter charge-current tolerance, an external resistor is recommended between the $5V_{REF}$ pin and the SS pin, setting up a much higher (100µA) charge current. The voltage on this pin is internally clamped at 3.5V and any resistor pulling up on this pin should be sized to limit the current to 150µA.

When the LT1339 pulls this pin low, the discharge current is 10mA. This discharge current becomes available whenever the voltage at the $12V_{IN}$ pin is greater than 3V. When the soft-start pin is fully discharged by the internal discharge transistor, the peak current programmed is zero. Grounding the SS pin will stop the top FET drive from turning on. The bottom FET drive will be on for the maximum time as set up by the running frequency and dead-time. Using the internal charge current, the time to full current is nominally Time (s) = $0.8 \bullet 10^5 C$. If this pin is unused, it should be left floating. If your design requires that the V_{REF5} output be active while the LT1339 output is shut down, use the circuit detailed in Figure 16.



NOTE: GROUNDING THE SOFT-START PIN WILL CAUSE THE OUTPUT TO BE DISCHARGED TO OR BELOW GROUND

Figure 16. Shutdown While Keeping $5V_{REF}$ Circuit Alive

V_C (PIN 7) CONTROL LOOP COMPENSATION NODE

This pin comprises the output of the error amplifier and the input of the peak current comparator. Normally it is used to compensate the output voltage control loop. Compensation is performed by adding a pole and a zero to the control loop function; sometimes an additional pole is needed—this is provided by C_{FINAL}. These two poles and one zero are configured by connecting this pin in the manner indicated in Figure 17. The total voltage loop is detailed in Figure 18. If your design requires gating on and off, use the RUN/SHDN pin as your first choice. If, however, you need to keep $5V_{REF}$ alive during the shutdown period, the V_C pin can be pulled down by an NPN transistor or MOSFET, as shown in Figure 19. This allows the soft-start function to work independently of the gating signal. If soft-start is desired on each turn-on of your gating sequence, refer to Figure 16 in the soft-start pin description. When using optoelectronic feedback in a forward converter, ground the feedback pin and connect the optoisolator to the V_C pin according to Figure 20.

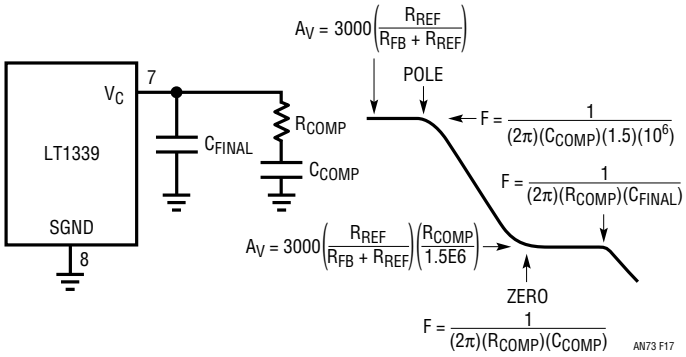


Figure 17. Control Loop Compensation

Current Sharing Multiple Power Converters

As with the synchronization of multiple LT1339 power converters, current sharing can be achieved by two different strategies: master/slave current sharing and peer-level sharing controlled by a system master control loop.

1. Master/slave current sharing is performed by the circuit detailed in Figure 21.
2. Operating peer-level power converters with a master system loop is detailed in Figure 22.

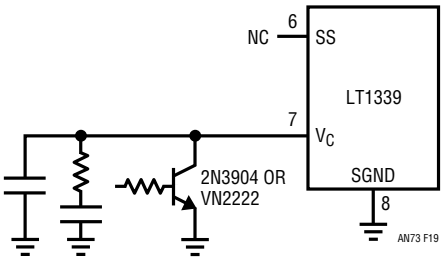


Figure 19. Gating the Power Converter On and Off Without Soft Start

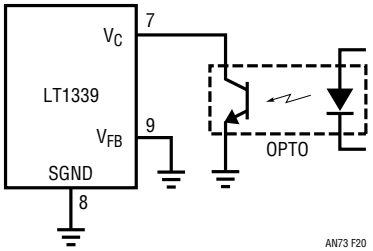


Figure 20. Optical Feedback Scheme

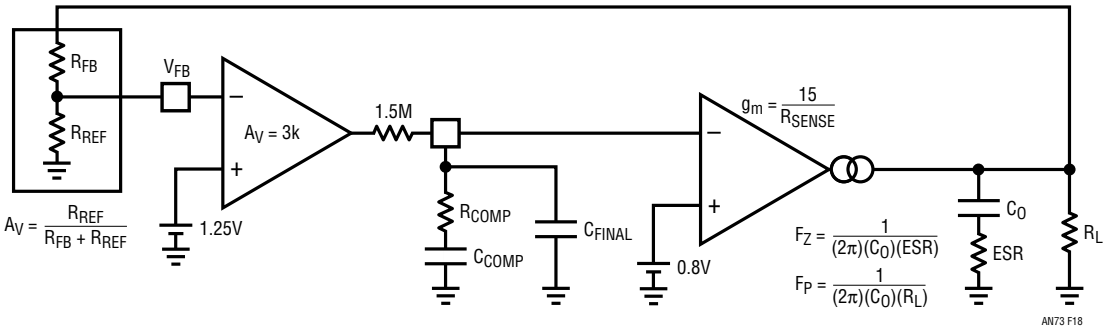


Figure 18. Total Voltage Loop

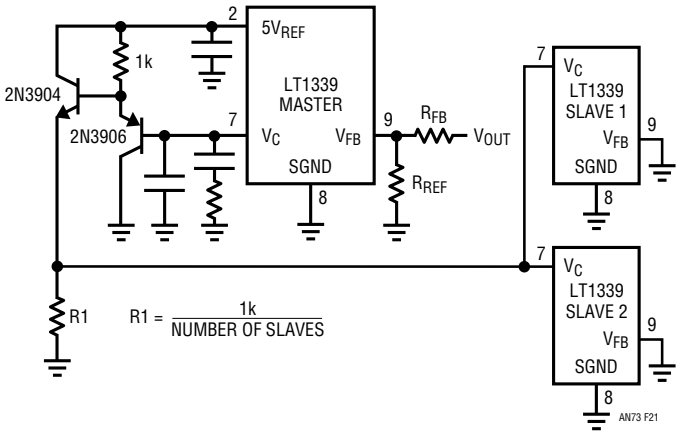


Figure 21. Master/Slave Current Sharing

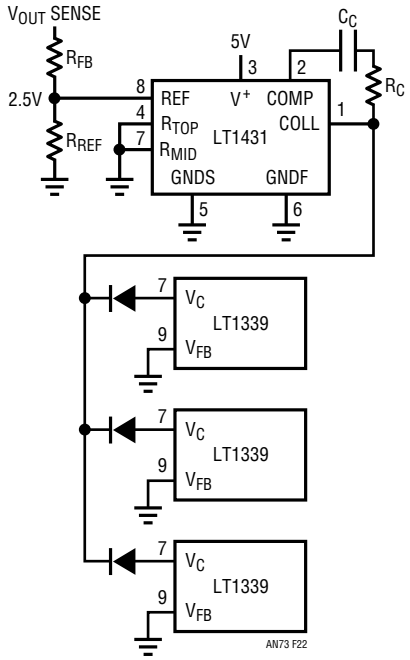


Figure 22. Peer Level Current Sharing

SGND (PIN 8) SIGNAL GROUND

This is the "clean" ground pin; it is for the returns of C_{CT}, the feedback resistor divider, C_{COMP}, C_{5VREF}, C_{IAVE}, C_{VREF} and $C_{SOFTSTART}$. This pin also is the reference for the RUN/SHDN pin. This pin is electrically connected to the PGND inside the LT1339; the resistance between these pins is approximately 10Ω. On the PCB there should be a trace connecting this pin to the PGND pin. This connecting trace should be situated so that no switching frequency AC or power level DC current flows through it. Placing the LT1339 on a ground plane with PGND and SGND connected to the plane works well.

V_{FB} (PIN 9) FEEDBACK PIN FOR OUTPUT VOLTAGE CONTROL

This pin is the inverting input to the error amplifier. The input voltage at the V_{FB} pin is subtracted from the voltage on the V_{REF} pin and converted into an error current by the error amplifier's transconductance of 0.002A/V. The LT1339, using its loop gain and current-controlled engine, is constantly forcing this pin to 1.250V. Thus, the output voltage is set by a resistor divider (See Figure 23) connected to this pin.

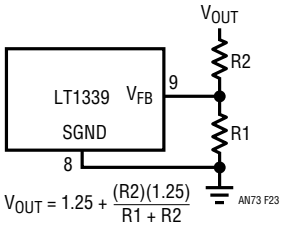


Figure 23. Programming LT1339's Output Voltage

Error Amplifier Characteristics

There is a DC voltage that, when placed on the feedback pin (V_{FB}), will cause the current output of the error amplifier to be zero. This voltage falls between 1.242V and 1.258V and is called V_{NULL}. Figure 24 details the DC characteristics of the error amplifier. Note the generous width of the linear region; this is important for noise immunity in high power systems. It is evident that a 200mV_{P-P} high frequency disturbance on the feedback pin will not take the error amplifier out of its linear region, and will be integrated in the compensation network. This is the essence of removing the nasty "R word" (rectification) from the

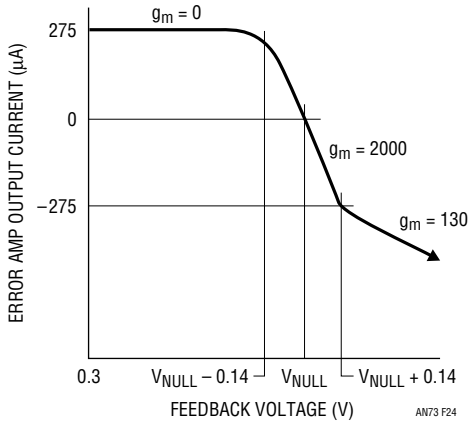


Figure 24. Error Amplifier Transconductance

arena of problems encountered with poorly designed parts. There is, however, a limit to the ability of the error amplifier to reject rectification when looking across the DC-to-daylight spectrum. Rectification happens when the dV/dT on the feedback pin approaches 50V/µs. The mechanism of this rectification is seen in Figure 25, as Q1 cuts off when the feedback pin's dV/dT goes positive faster than I_1 can charge C1. If the feedback pin slews at rates approaching this limit, we recommend that you add a small capacitor between the feedback pin and the V_{REF} pin or SGND pin to slow down the signals at the V_{FB} pin. The feedback pin has a maximum voltage and current restriction. If you pull the feedback pin above 5V, you will turn on a parasitic vertical PNP transistor and inject current into the substrate. Under such conditions the current into the feedback pin should be limited to less than 1mA.

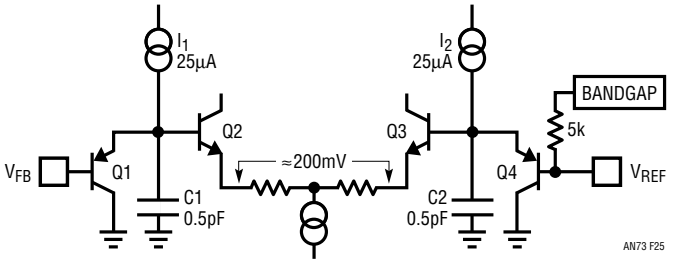


Figure 25. Error Amplifier Input Stage

V_{REF} (PIN 10) ERROR AMPLIFIER VOLTAGE REFERENCE DECOUPLING

The V_{REF} pin is connected directly to the noninverting input of the error amplifier. This pin is normally decoupled with a 0.1µF cap connected from this pin to SGND. Internally, there is a 5k isolation resistor between this pin and the bandgap reference. The dynamic output impedance of the bandgap reference is approximately 100Ω.

Setting Up a Voltage Soft-Start Using the V_{REF} Pin

The error amplifier that is connected to this pin has an input common mode range that extends below 0.6V. This pin can be used for a voltage soft-start circuit. The circuit shown in Figure 26 utilizes the error amplifier to program a soft-start that starts at 50% of nominal output voltage and ramps up to 100% of the nominal output voltage.

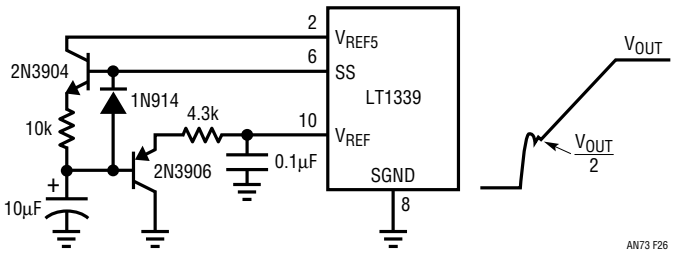
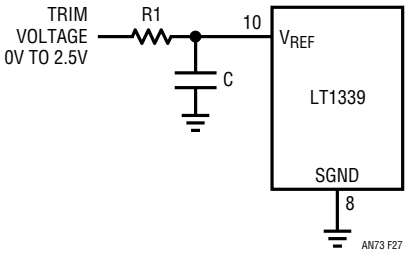


Figure 26. Voltage Soft Start

Using the V_{REF} Pin to Implement a Noise-Immune Output Voltage Trim

Although the output voltage can be easily trimmed by adding a resistor to the V_{FB} pin, the poor noise immunity of this trim method is less than desirable. A much better voltage trim is accomplished by connecting an appropriate valued resistor to the V_{REF} pin and adjusting the value of the decoupling capacitor for a time constant in the tens to hundreds of milliseconds (refer to Figure 27). The time constant of noise reduction on the V_{REF} pin has no effect on loop stability, unlike networks used on the V_{FB} pin. This function is also useful in applications requiring remote sense.



$$\text{TRIM RANGE WITH 0V TO 2.5V INPUT} = \left(\frac{V_{OUT}}{1.25}\right)\left(\frac{5k}{R1 + 5k}\right)$$

$$\text{TIME CONSTANT } (t_{NR}) = \frac{(5k)(R1)}{C(5K + R1)}$$

Figure 27. The Right Way to Trim Output Voltage

$SENSE^+$ (PIN 11) SENSE AMPLIFIER NONINVERTING INPUT

This pin, in conjunction with the $SENSE^-$ pin, forms the input to a wide common mode range differential amplifier. This amplifier takes its differential input voltage, adds an intentional 5mV offset, multiplies the result by 15 and adds it to a voltage that is one V_{BE} (~0.7V) above ground. This

provides an internal voltage representing the current flowing in the external current sense resistor (R_S). This voltage is used for current mode operation and in the average-current-limiting loop. The input common mode range extends from –0.3V to 60V. This common mode range spans two ranges of operation, –0.3V to (5V – $1V_{BE}$) and (5V – $1V_{BE}$) to 60V. We will investigate these two ranges of operation because the input characteristics of this amplifier change somewhat when going from one range to the other. The input structure of the current sense amplifier is shown in Figure 28.

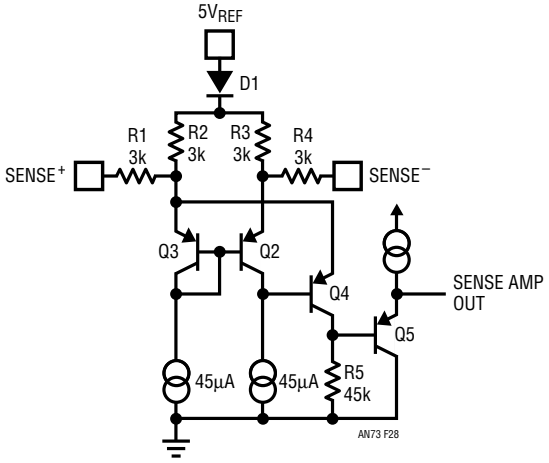


Figure 28. Current Sense Amplifier Equivalent Circuit

High Common Mode Voltage

When the SENSE+ and SENSE– pins are above (5V_{REF} – 1V_{BE}) D1 is not conducting and the input bias current is 45µA (the emitter current of the PNPs). When the voltage on SENSE+ goes positive with respect to the voltage on SENSE–, current in excess of 45µA flows through R1 and through Q4 into R5. The voltage across R5 thus becomes a representation of the voltage between SENSE+ and SENSE– multiplied by 15. Keep in mind that the emitter voltages of Q2 and Q3 are always the same. This amplifier has a bandwidth of 300kHz.

The Low Voltage Range

When these pins are pulled below (5V_{REF} – 1V_{BE}), the direction of input bias current changes and its magnitude depends upon how far the sense leads are pulled below (5V_{REF} – 1V_{BE}). When using this amplifier in the low voltage mode, the input bias current is high, so be sure that any external resistors connected to these pins are matched.

SENSE– (PIN 12) SENSE AMPLIFIER INVERTING INPUT

This pin complements the function of the SENSE+ pin (Pin 12).

See the Pin 11 definition.

RUN/SHDN (PIN 13) PRECISION REFERENCED SHUTDOWN CONTROL PIN

This pin implements the user-programmed undervoltage (UV) lockout. By placing a resistor divider from V_{IN} at this pin to ground, any UV lockout voltage from 1.25V through hundreds of volts can be programmed. Internal hysteresis of this pin is internally set at 15mV (1.2% of the 1.25V switching point). Additional hysteresis can be implemented by adding a resistor from this pin to the 5V_{REF} pin (see Figure 29a).

Figures 29b and 29c detail digital shutdown with and without UV lockout.

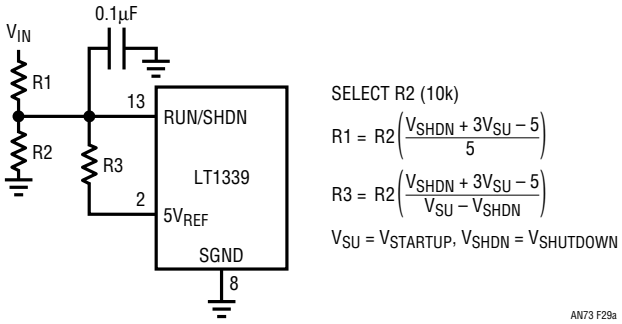


Figure 29a RUN/SHDN Pin

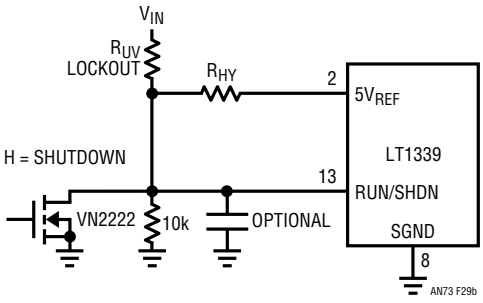


Figure 29b UV Lockout with Digital Shutdown

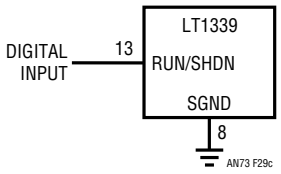


Figure 29c Digital Shutdown

PHASE (PIN 14) OUTPUT DRIVER PHASE CONTROL

This pin configures the LT1339 to function in one of its two separate modes:

1. Synchronous buck converter (pin left floating or tied to 5V)
2. Synchronous boost converter (pin grounded)

The threshold of this pin is at $1V_{BE}$ above ground and it has very good noise immunity when left floating. The input characteristics of this pin are such that sinking current from this pin (pulling it low) at about 40µA (approximately 15k to ground) brings the voltage down to the gray area of its threshold. In this gray area, the LT1339 is in a state where it is uncertain of the mode in which to operate; in this condition, the gate-drive level is diminished and certain failure will result.

Moral: either ground the PHASE pin, float the PHASE pin or tie it to $5V_{REF}$.

PGND (PIN 15) POWER GROUND

This is the "substrate pin" of the LT1339; the pin relative to which it is desirable to keep the voltages on all other pins positive. This pin carries the return current for the bottom gate drive current, the majority of the LT1339's quiescent current and the fault current generated when pins are carelessly allowed to swing more than $1V_{BE}$ below this pin. There should be a short trace from this pin to the IC decoupling capacitor, and this pin should be connected to the ground plane of the circuit.

BG (PIN 16) BOTTOM-SIDE GATE DRIVE

This pin is the output of the bottom gate driver, a hefty, fearless drive output. Due to the enormous size of the output drive transistors, pulling this pin negative with respect to PGND by $1V_{BE}$ turns on the large NPN collector-to-substrate diode. This injects current into the substrate. The bottom gate drive can easily push 10,000pF around, but efficiency tests have shown that about 1% to 2% of additional efficiency can be bought by adding a pair of external buffer transistors (see Figure 30).

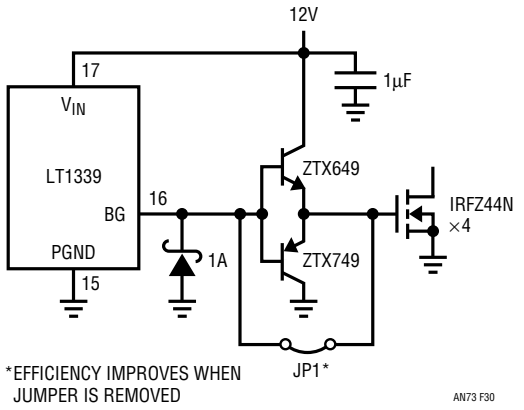


Figure 30. External Drivers Improve Efficiency

NULLIFYING THE PHANTOM TURN-ON

About 200ns prior to the top gate turning on, the bottom gate turns off. During that time (the underlap time), the main inductor current flows through the body diodes of the bottom FETs. By the time the topside FET turns on, significant stored charge is packed away in the body diode(s) of the bottom MOSFET(s). Upon turning on, the top MOSFET "sees" a short—the unrecovered body diodes of the bottom MOSFETs. Large currents start to flow as the stored charge in the body diode is swept out. Upon releasing the last of its charge, the bottom body diode snaps off (switch opens in a few nanoseconds). At this time the drains of the bottom MOSFETs are pulled positive by tens of volts in a few nanoseconds. Referring to Figure 31, it can be seen that the bottom MOSFET has phantom RC networks that act as little voltage dividers ($V_{G(STEP)S}$) with time constants τ_Gs. When the dV/dT and ΔV are high enough, the internal V_{GS} reaches one threshold voltage and bad things happen (efficiency drops). Figure 32 details the removal of the phantom turn-on mechanism by offsetting the bottom gate voltage to –3.3V when the bottom FET is off, effectively placing the gate-threshold point out of reach of $V_{G(STEP)}$.

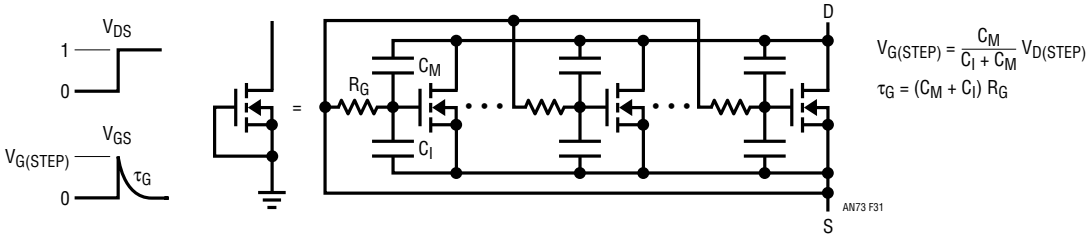


Figure 31. The Phantoms Lurking Inside Your Bottom Side MOSFETs. At Some dV/dT on the Drain with a Big Enough Step, This FET will Turn Itself On Even with the Gate Connected to the Source

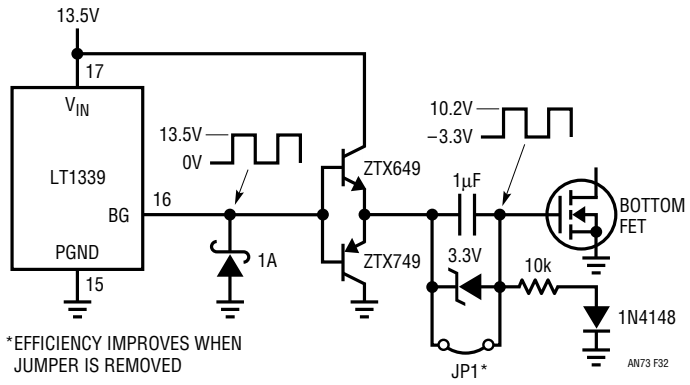


Figure 32. Offsetting the Bottom Gate Drive Removes Phantom Turn-On Losses from Higher Input Voltage Operation

$12V_{IN}$ (PIN 17) 12V POWER SUPPLY INPUT

Although the LT1339 is designed and optimized to run on input voltages ranging from 10V to 15V, it can run on voltages from UV lockout to 20V (the absolute maximum input voltage); however, operation above 18V is not recommended. This pin should be decoupled to the PGND pin with short traces, low ESR and capacitor values of at least 1µF (keep in mind that this pin is providing the positive drive current for the bottom-side MOSFET driver).

The current flowing into this pin can be divided into three parts: I_{ACTIVE} , $I_{DYNAMIC}$ and $I_{STANDBY}$

1. Active Supply Current

   Active V_{RUN} > 1.35V (1.25V typ) I_{ACTIVE} = 14mA typ, 20mA max

2. Dynamic supply current V_{RUN} > 1.35V (1.25V typ) $I_{DYNAMIC} = (Q_G \text{ (of bottom FETs)} \bullet f_{SW})$

3. Standby Supply Current V_{RUN} < 1.15V (1.25V typ) $I_{STANDBY}$ = 150µA typ, 220µA max
   I_{ACTIVE} includes $I_{STANDBY}$

The power dissipated by the LT1339, when active, is the sum of the power drawn by the $12V_{IN}$ pin and the V_{BOOST} pin, and is calculated below:

$$P_{TOTAL} = P_{12VIN} + P_{BOOST}$$

where:

$P_{12VIN} = (V_{IN})(Q_{GB} \bullet f_{SW} + 20mA)$
Q_{GB} = the sum of all Q_Gs of all of the bottom FETs
$P_{BOOST} = (V_{IN} – 0.6V)(Q_{GT} \bullet f_{SW} + 2.2mA)$
Q_{GT} = the sum of all Q_Gs of the top FETs

TS (PIN 18) BOOST OUTPUT DRIVER REFERENCE (TOP SOURCE)

This is the negative supply pin for the top driver. Externally it is connected to the source of the top MOSFET. This pin should be clamped to ground with a Schottky diode, preventing it from going below the substrate (PGND pin). The LT1339 is designed to be robust and will not latch up if this pin goes to –3V. Excursions of this pin below substrate will cause unwanted charge to be injected into the substrate. When injection occurs, changes can be seen in the operation of the LT1339 in the form of a shortening of the underlap time between the bottom gate drive and the top gate drive. In many high power applications, it is impossible to keep the source(s) of the top FET(s) from going volts below PGND. Depending upon which MOSFETs you use and upon your layout, this can become a real problem as top switch currents rise above 50A to 100A. The circuit detailed in Figure 33 uses a common mode transformer to solve this problem, and should be considered for very high power converters.

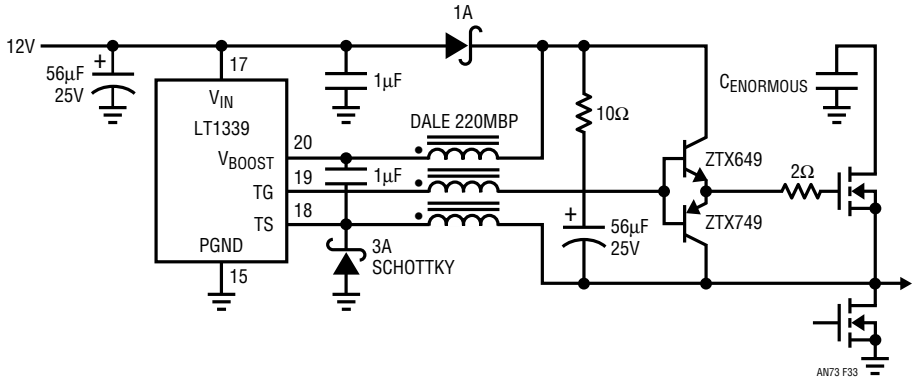


Figure 33. Using a Common Mode Transformer to Keep Large Negative BUS Excursions from Injecting into the Substrate Via the TS Pin

TG (PIN 19) TOPSIDE DRIVER GATE OUTPUT (TOP GATE)

This pin is the gate driver for the topside MOSFET. It acquires its current to charge the topside gate positive from the V_{BOOST} pin, which is sourced by the external boost capacitor. The negative drive current is obtained from the TS (Top Source) pin.

V_{BOOST} (PIN 20) TOPSIDE DRIVER POWER SUPPLY PIN.

This pin is the power supply pin for the top driver. It should be decoupled to the TS (Top Source) pin with a 1µF low ESR capacitor. This external capacitor is charged during the time the bottom transistor is on via an external diode from $12V_{IN}$.

BUCK REGULATOR DESIGN

OVERVIEW

The buck converter is a converter that has an input voltage greater than its output voltage. The simplest buck converter is the linear-pass regulator. Its input is a voltage that varies over the regulator's input range and its output is a constant voltage. The power dissipated in a linear-pass regulator is the product of the differential voltage ($V_{IN} – V_{OUT}$) and the output current. The efficiency of a linear-pass regulator is simply the ratio of output voltage divided by input voltage (multiplied by 100%). In some low differential voltage applications, the linear-pass regulator has efficiencies that rival those of switching regulators. It takes a well-designed switcher to surpass the efficiency of a linear-pass regulator in a 3.3V input/2.5V output application.

Switching buck converters have current multiplication, in that the output current exceeds the input current. In an ideal buck converter, the ratio of output current to input current is the same as the ratio of input voltage to output voltage (100% efficiency).

Characteristics of the Synchronous Switching Buck Converter

The synchronous buck converter has the following characteristics:

1. It has a minimum input voltage that it needs to provide rated output voltage. For the power converter (the LT1339 and its associated components), this voltage is usually limited by the maximum duty factor and the resistive losses in the top FET, inductor and sense resistor. In some designs (those with small inductors) the minimum input voltage will be the voltage at which the converter experiences current mode instability (an instability found in clocked, current mode converters operating at duty factors approaching unity), and design action should be taken: either increase the inductance, add slope compensation or use the undervoltage lockout capability of the RUN/SHDN pin to lock out operation.
2. There is a maximum input voltage, above which something will break.
3. The input current is discontinuous, with high AC RMS values that require large input capacitors just to accommodate the high AC current. This also causes high input ripple voltage; an input filter may be required to keep the switching frequency ripple from contaminating the power source.
4. The output current is continuous and has a triangular/sawtooth wave shape. This means small output capacitors and low output ripple.
5. There is no forward parasitic power path; hence, shutting down the buck converter turns off the output.
6. There is a parasitic reverse power path at the output: if the output is pulled below ground, current flows through the body diode of the bottom MOSFET, through the inductor, through the sense resistor and out. Were you to connect a car battery to the output of a synchronous buck converter backwards, current would be limited by very small resistances. This is not recommended.
7. There is also a parasitic reverse power path at the input: if the input is pulled below ground, the equivalent circuit simplifies to two diodes to ground. These diodes—the body diodes of the MOSFETs—are all that stands between your circuit and disaster. When reverse polarity input voltage is applied, there is no built-in mechanism to limit reverse current. The usual result is irrepairable damage.
8. If the output voltage is pulled above the input voltage, the body diode of the top MOSFET conducts to supply power from the output back to the input. If you have a car battery at the output, don't short the input.
9. Inductor value is not extremely critical; increasing the inductor value above the required minimum nets small returns.
10. Efficiencies range from the low 80%s to the high 90%s.
11. The optimum switching frequency is determined by tradeoffs in core losses in the inductor, switching losses and gate-charge losses against smaller inductors and capacitors and faster transient response. For modern core materials, capacitors and MOSFETs, the frequency typically falls in the 50kHz to 125kHz region.

GRAPHICAL DESIGN EXAMPLE

Although the LT1339 data sheet details the procedure for designing a buck converter, some of us like to see the pictures to make our decisions. Here is a graphical design guide for the LT1339 synchronous buck converter. Everything here is normalized to a 100kHz clock frequency and 1A I_{LIMIT}. Here we will design a 12V input, 3.3V/20A output converter. Since our maximum output current is 20A, we will set the current limit at 24A.

Now, we pick some value for the ratio of peak-to-peak ripple current to current limit output current. Any value between 10% and 80% will do; for this example we'll use 30%. This results in a ripple current of 24A • 0.3, or 7.2A

Look at Figure 34. Starting from the right, follow the 30% isocline to the left until it intercepts the input voltage = 12V grid line. (This is labeled "1" on Figure 34.) This yields 80µH, which is denormalized by dividing it by I_{LIMIT} (80µH/24 = 3.33µH). Note that this inductor value is well above the shaded areas where things get nasty. We could choose a higher ripple percentage and not get bitten.

Let's look at some of the other graphs to see what effect choosing a higher ripple ratio would have.

Referring to Figure 35, we see that the ripple current ratio doesn't make any significant difference in the AC RMS input current. Further, we see that the input capacitor AC RMS ripple current is 0.46A for the example above ("1A" on Figure 35); multiplying this by the rated output current of 20A yields 9.2A; hence big input caps will be required, regardless of inductor value. Note that if the minimum input voltage is 7V, the input AC RMS ripple current goes up to 10A (1B on Figure 35).

What about output capacitor AC RMS current? Refer to Figure 36 to see the interaction. Here we see that the AC RMS current is 0.087A ("1" on Figure 36); multiplying this by 20A yields 1.74A_{RMS}—no problem; maybe 30% is too low.

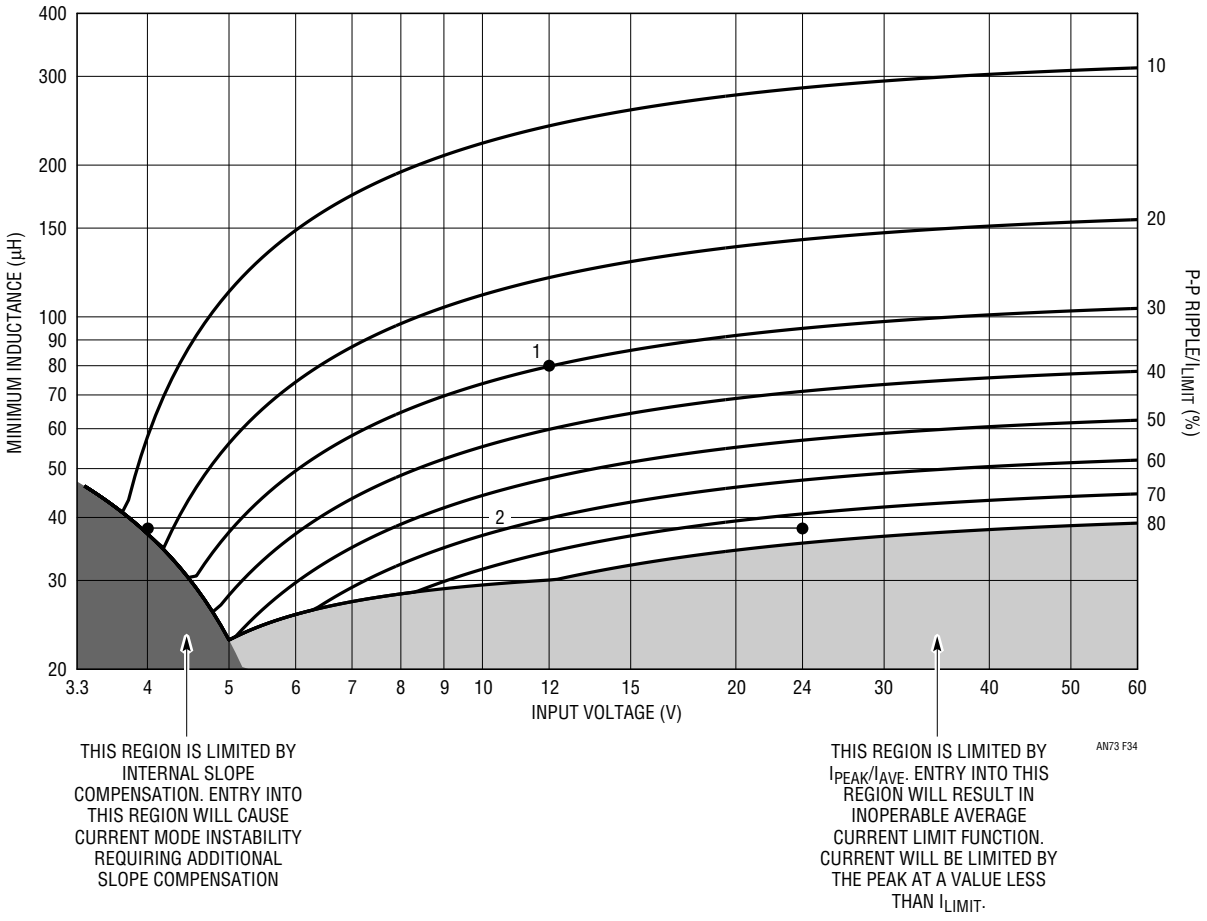


Figure 34. 3.3V Output Normalized Minimum Inductor Value

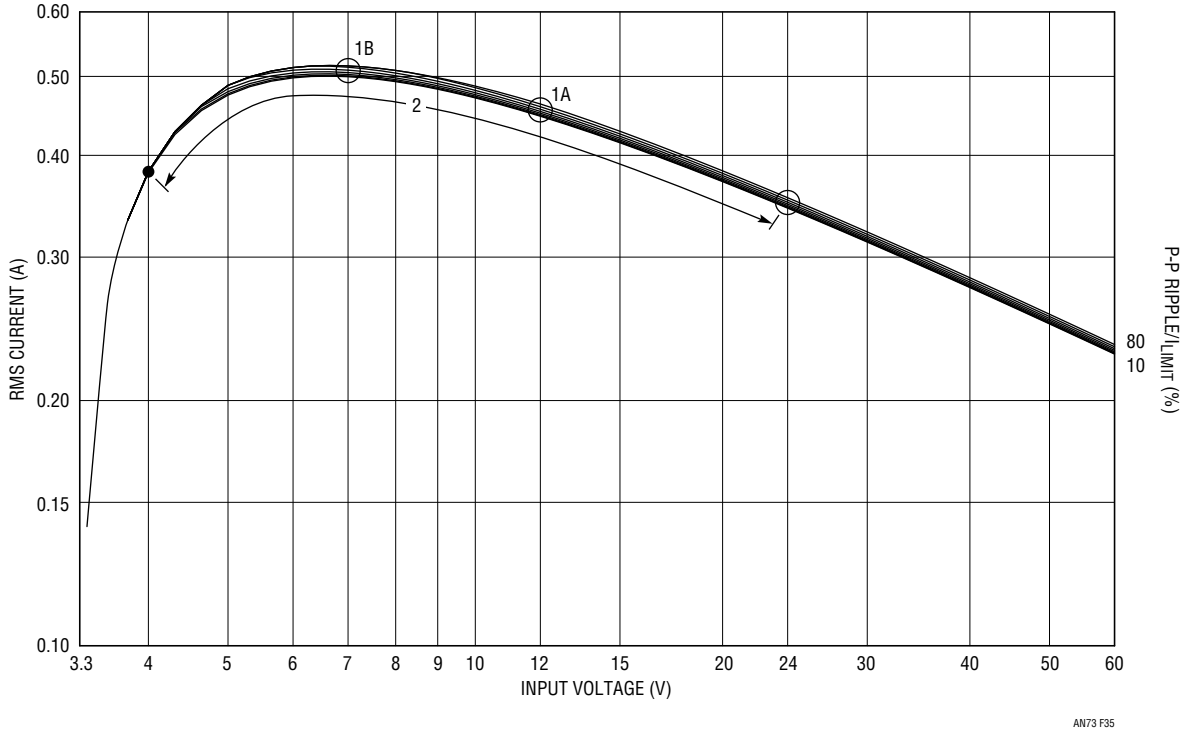


Figure 35. 3.3V Output Normalized RMS AC Input Capacitor Current

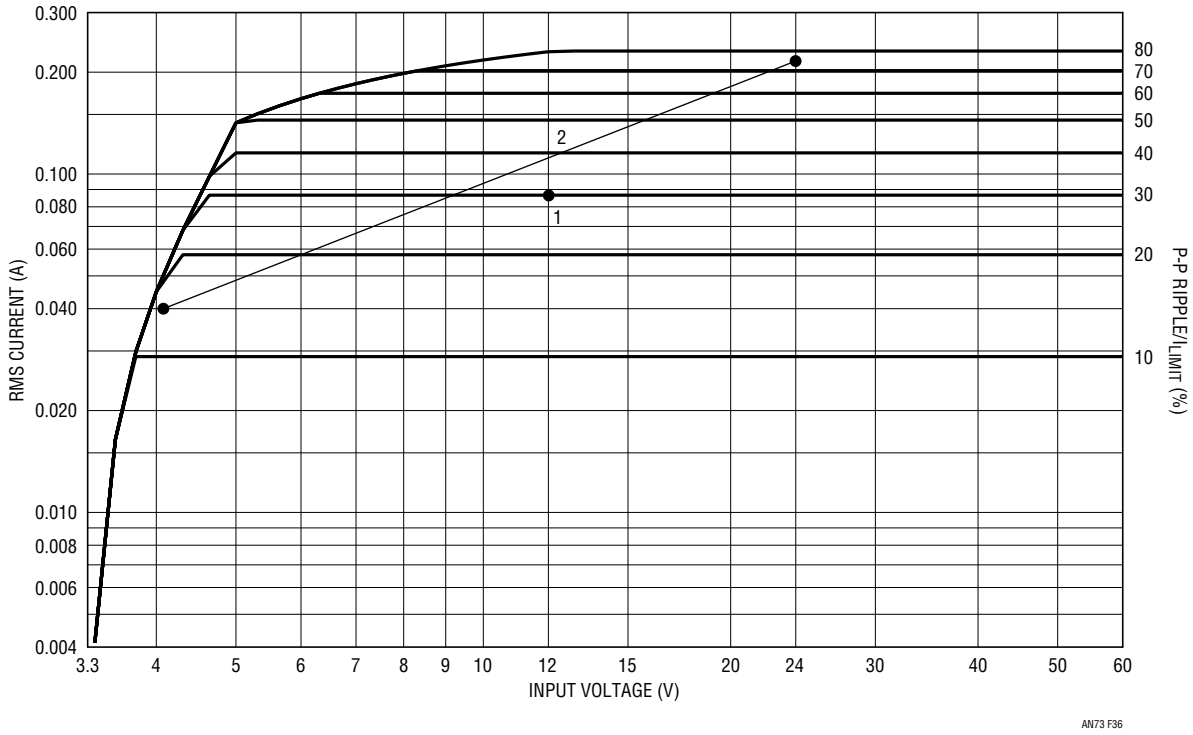


Figure 36. 3.3V Output Normalized Output Capacitor AC RMS Current

Let's look at the RMS current in our transistors. Figure 37 details the bottom MOSFET RMS current at 0.85A; multiplying this by 20A yields a modest 17A ("1" on Figure 37). Referring to Figure 38, the top MOSFET RMS current is 0.525A; multiplying this by 20A yields 10.5A.

HINDSIGHT

Other than the output capacitor's RMS current from Figure 36 and the shaded areas of Figure 34, the ratio of peak-to-peak ripple current to current limit will have little effect on the buck converter (the actual value of the inductor is quite noncritical).

THIS IS TOO EASY; LETS DO A HARD ONE

4V < V_{INPUT} < 24V, V_{OUTPUT} = 3.3V/20A, operating at 60kHz using the smallest inductance

Start with Figure 34; pick the inductor value bounded by the darker shaded zone to the left (current mode instability), see the point at the left of the line labeled as 2 on the figure. Draw a line of constant inductance from 4V to 24V.

The value of inductance we have chosen is 38µH, which denormalizes to 38/24 or 1.58µH, at 100kHz, which denormalizes to 100k/60k • 1.58µH or 2.63µH at 60kHz. Verify that we stay airborne (hitting mountains bends propellers). We notice from the isoclines that our peak-to-peak ripple/I_{LIMIT} varies from 15% at V_{IN} = 4V to 75% at V_{IN} = 24V. Move on to Figure 35 to verify that the peak input capacitor current will be at its maximum at V_{IN} = 7V which denormalizes to 10A (see line labeled "2"). Next, refer to Figure 36 and draw a line representing the change in P-P ripple/I_{LIMIT} vs input voltage that we learned from Figure 34 (this is the line labeled "2").

We can see that our maximum output capacitor AC RMS current will be 0.25A multiplied by 20A, or 5A.

From Figure 37 we learn that our maximum RMS bottom MOSFET current will be 0.95A • 20A, or 19A when the input voltage is at 24V.

Figure 38 informs us that our maximum top MOSFET RMS current will be 0.9A • 20A, or 18A.

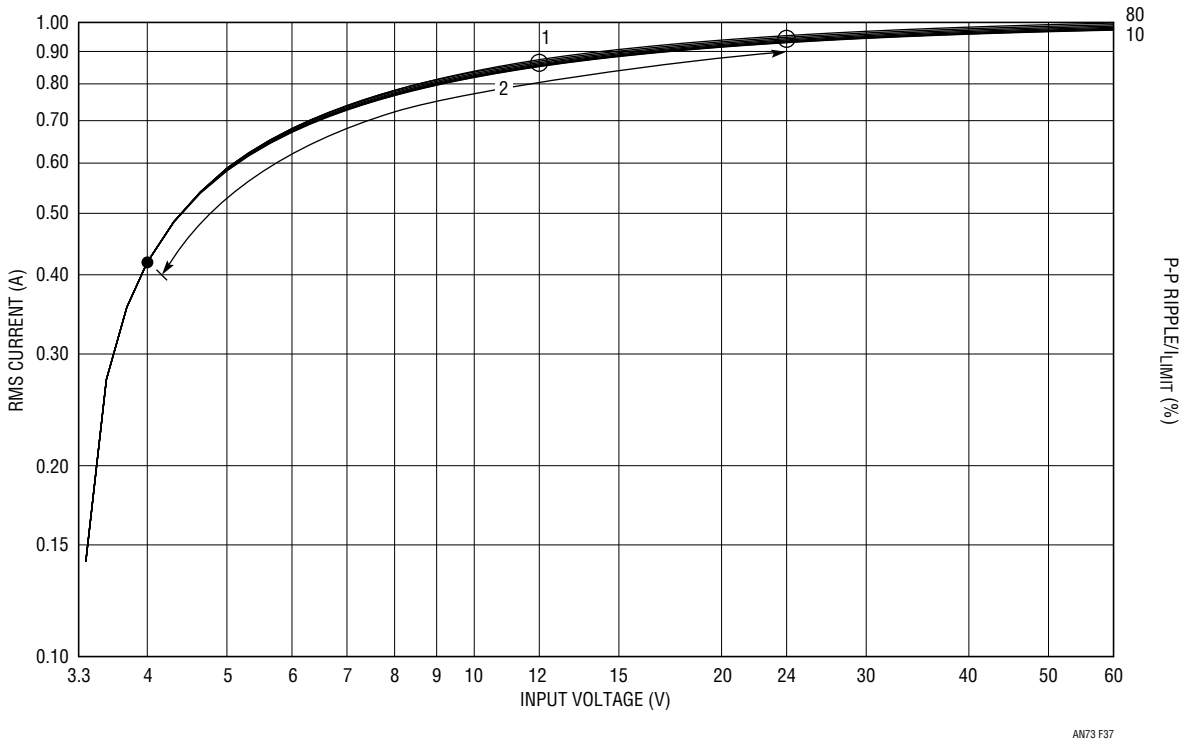


Figure 37. 3.3V Output Normalized RMS Bottom Transistor Current

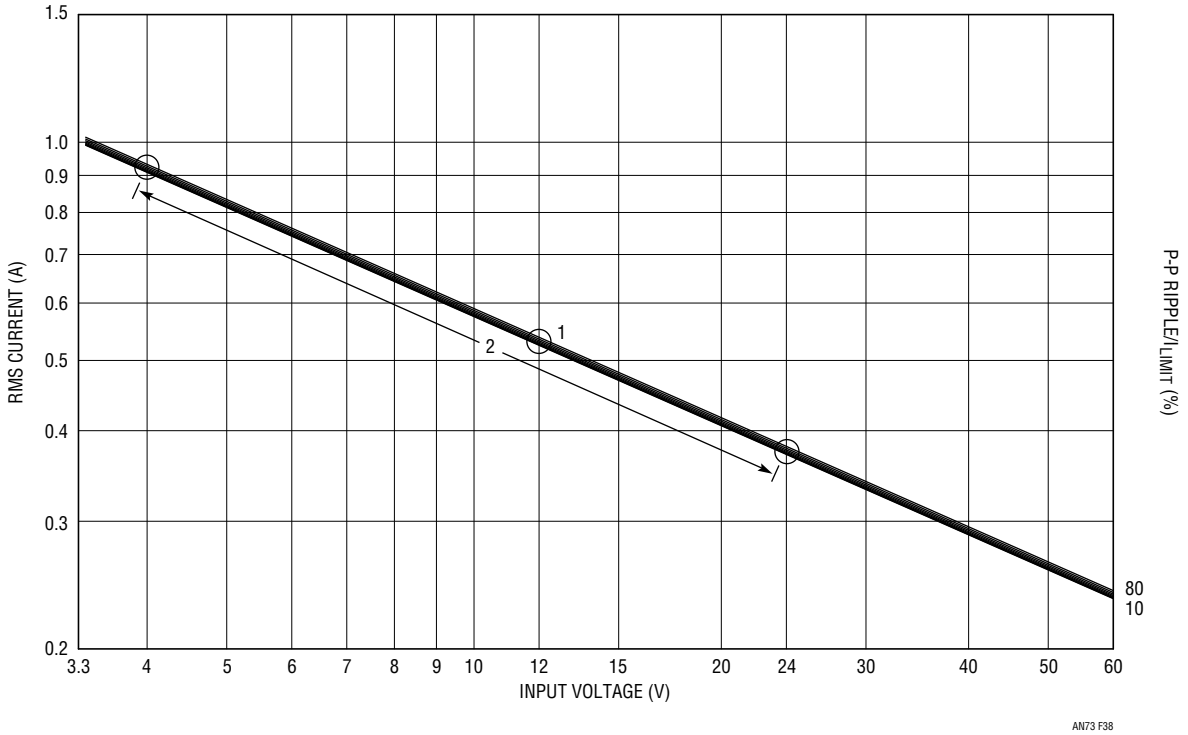


Figure 38. 3.3V Output Normalized Top Switch RMS Current

CONCLUSION

The LT1339 has plenty of internal slope compensation for most buck converters.

Inductor ripple current has little effect on anything except stability, average current limit and the inductor's own core loss.

The next four sections are graphical design aids for 3.3V, 5V, 12V and 24V converters. The procedure for using these design aids is the same as described in the preceding examples.

3.3V OUTPUT GRAPH SET

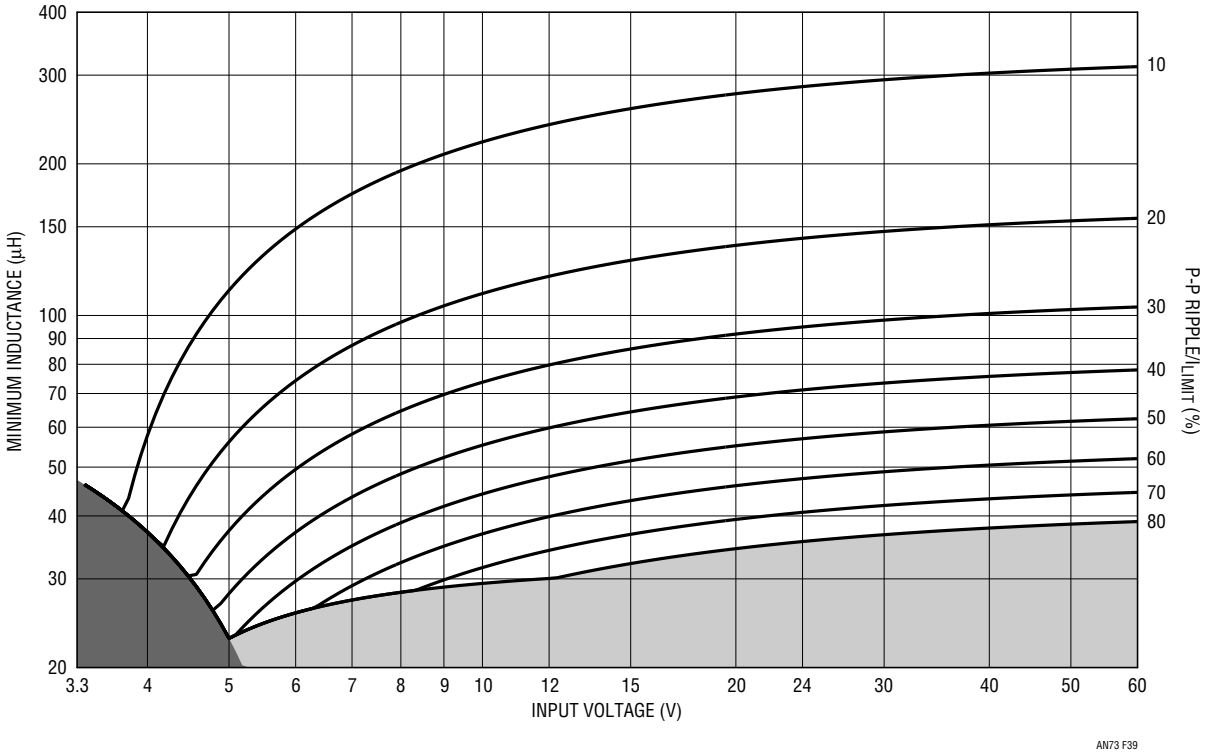


Figure 39. 3.3V Output Normalized Minimum Inductor Value

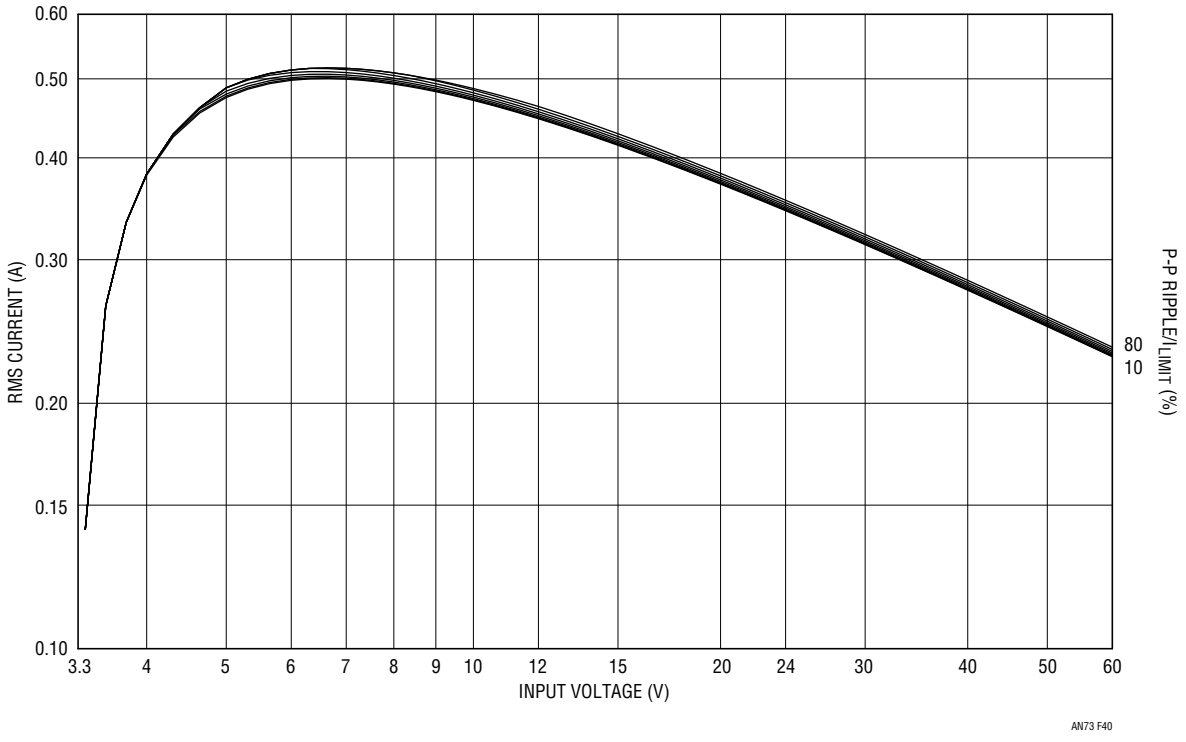


Figure 40. 3.3V Output Normalized RMS AC Input Capacitor Current

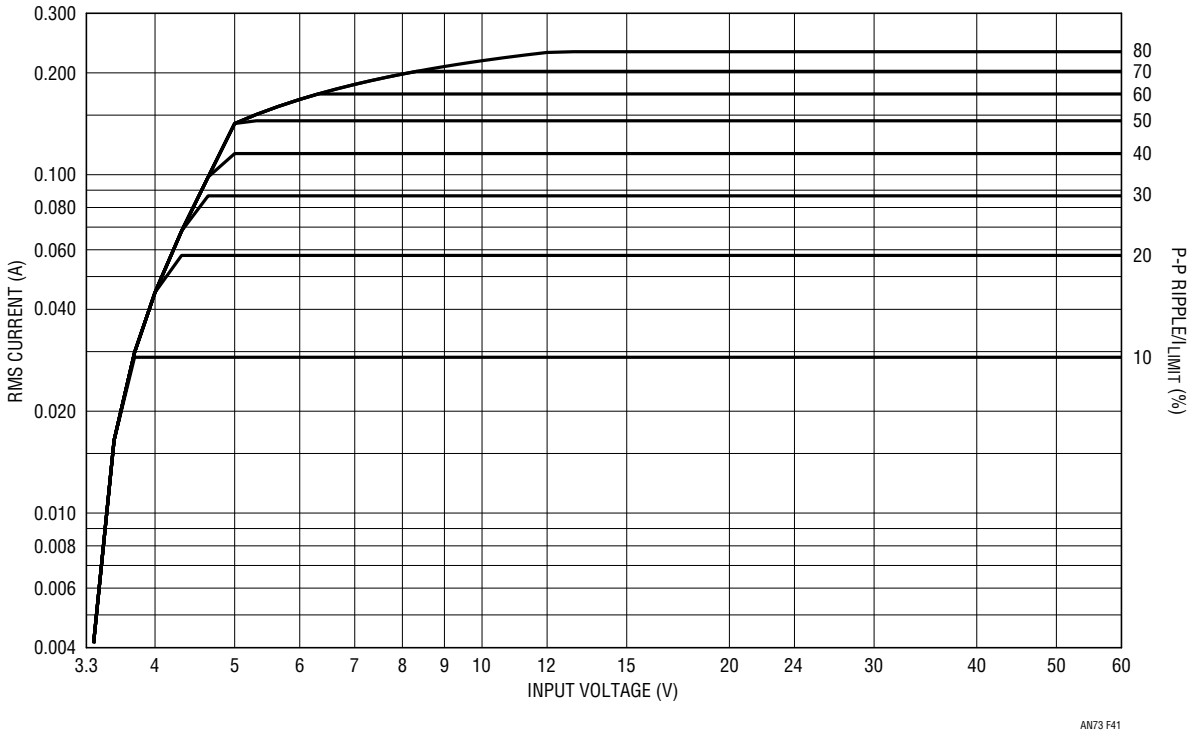


Figure 41. 3.3V Output Normalized Output Capacitor AC RMS Current

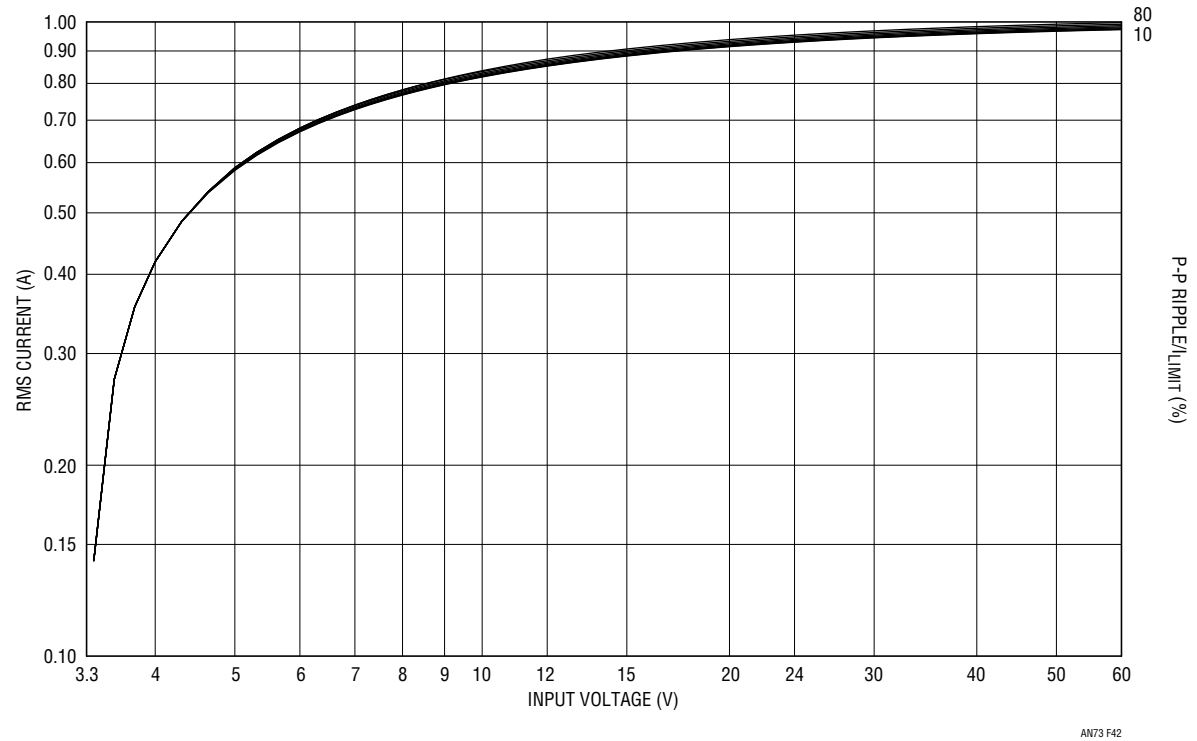


Figure 42. 3.3V Output Normalized RMS Bottom Transistor Current

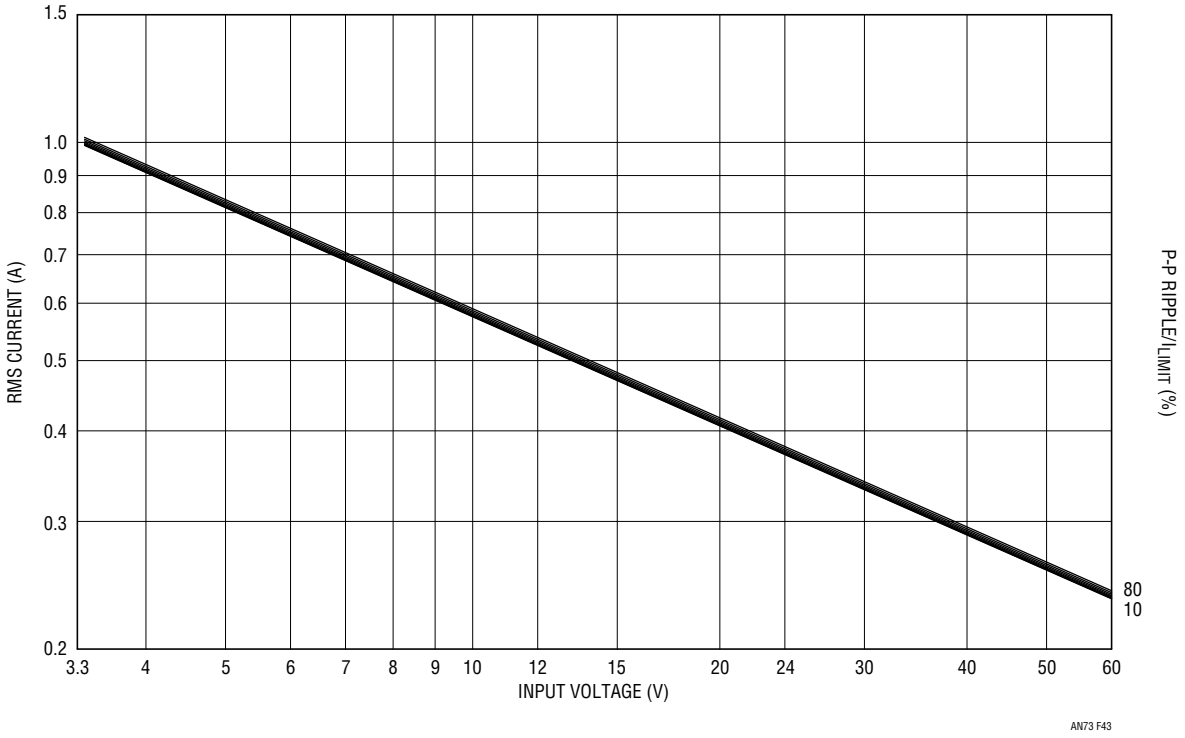


Figure 43. 3.3V Output Normalized Top Switch RMS Current

5V OUTPUT GRAPH SET

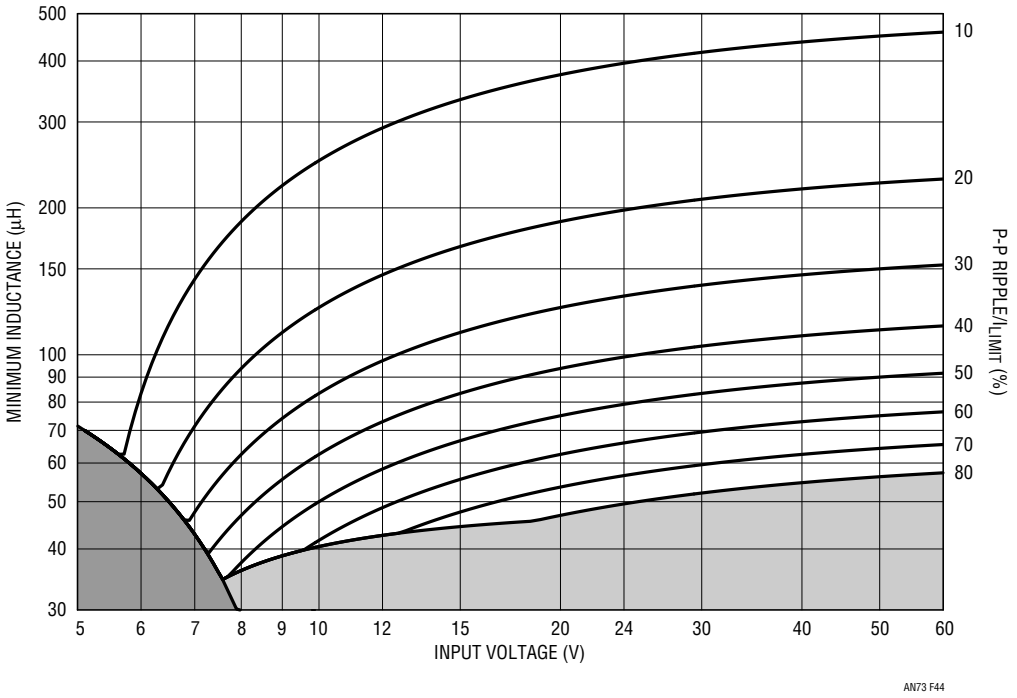


Figure 44. 5V Output Normalized Minimum Inductor Value

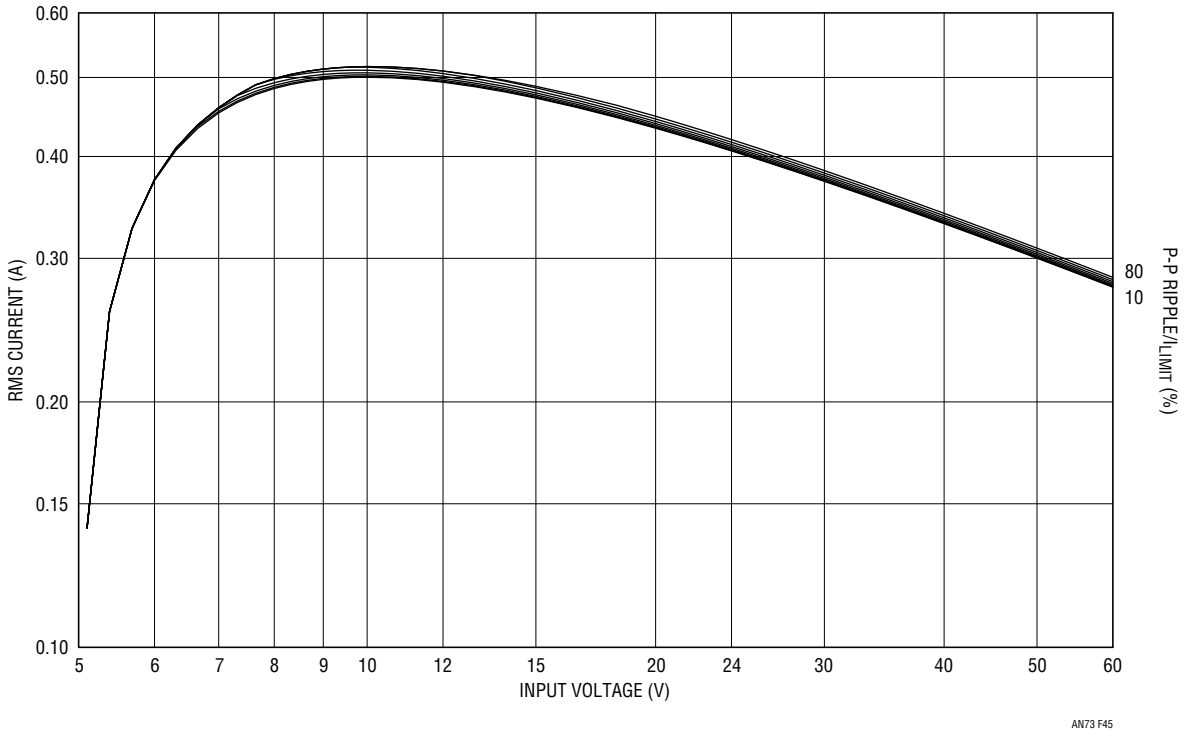


Figure 45. 5V Output Normalized RMS AC Input Capacitor Current

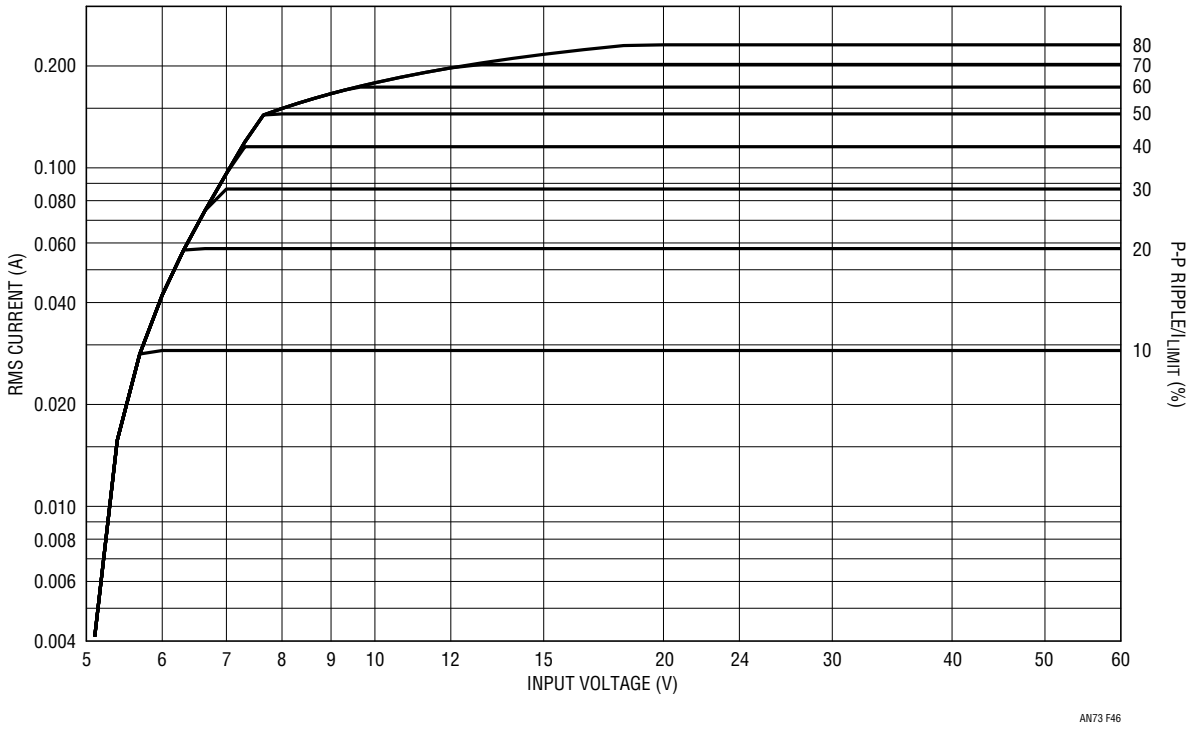


Figure 46. 5V Output Normalized Output Capacitor AC RMS Current

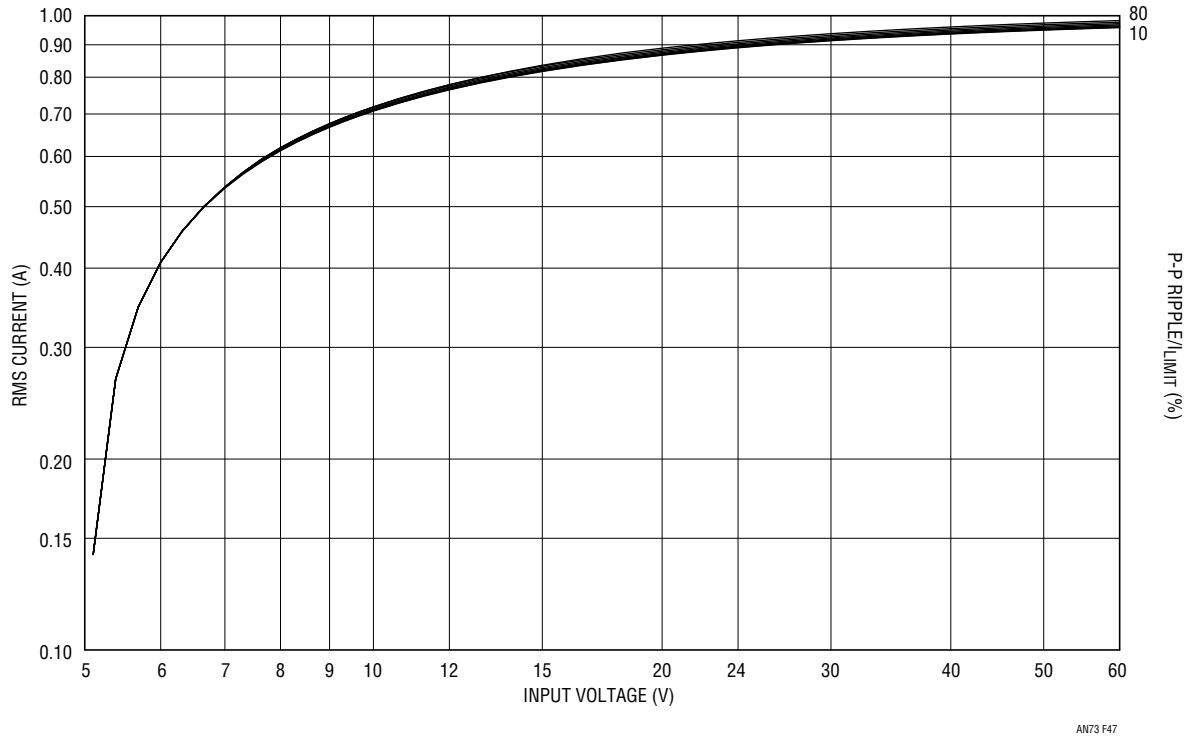


Figure 47. 5V Output Normalized RMS Bottom Transistor Current

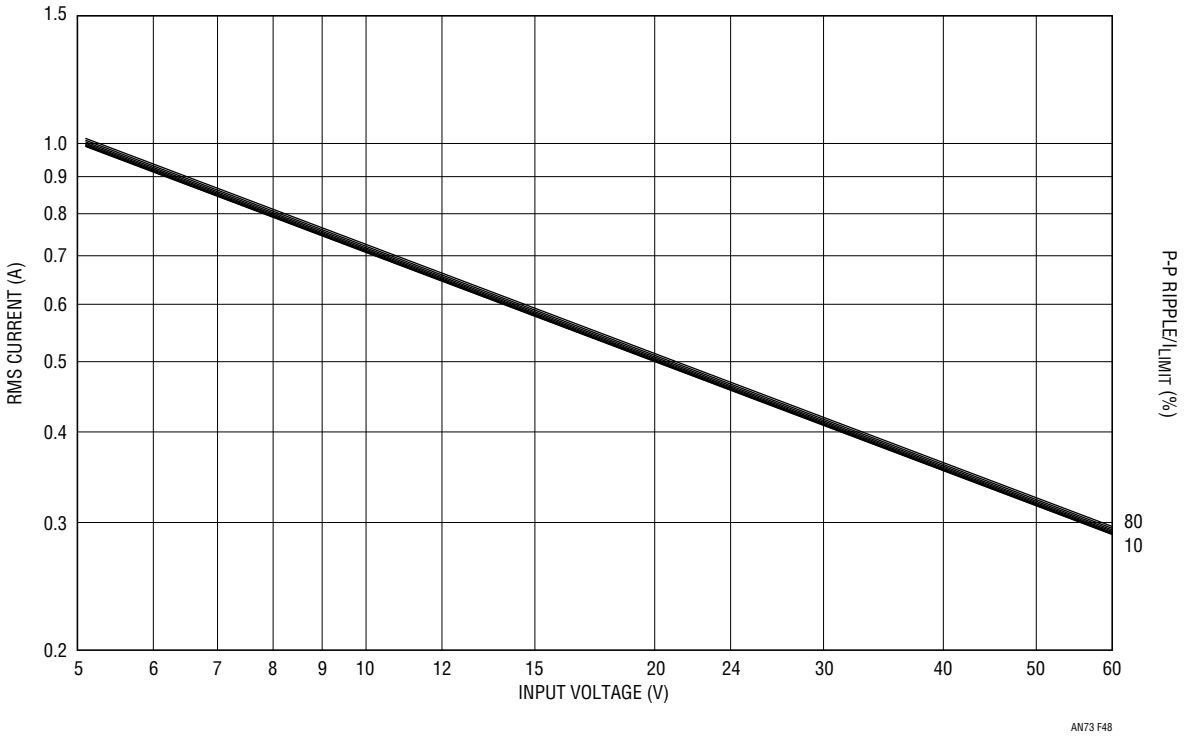


Figure 48. 5V Output Normalized Top Switch RMS Current

12V OUTPUT GRAPH SET

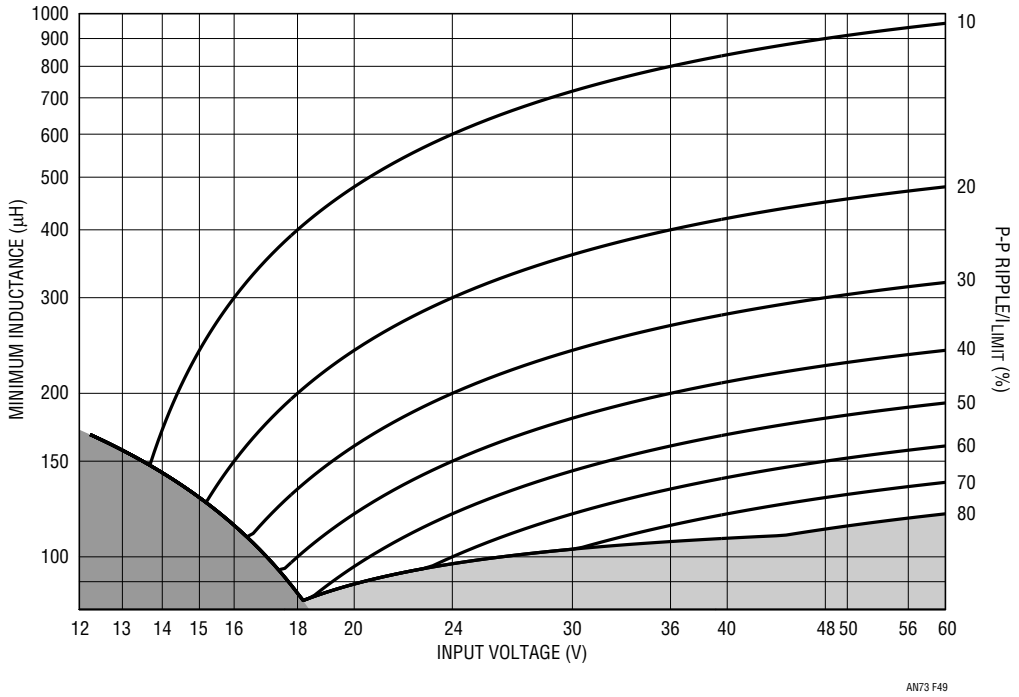


Figure 49. 12V Output Normalized Minimum Inductor Value

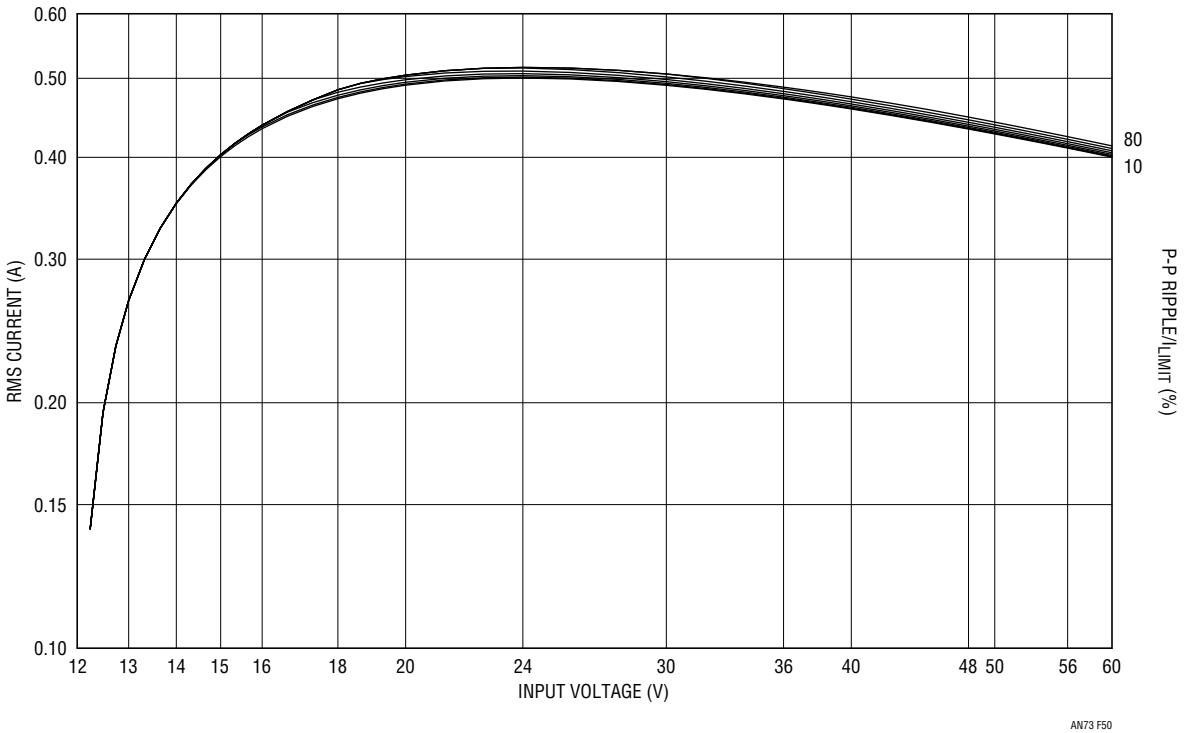


Figure 50. 12V Output Normalized RMS AC Input Capacitor Current

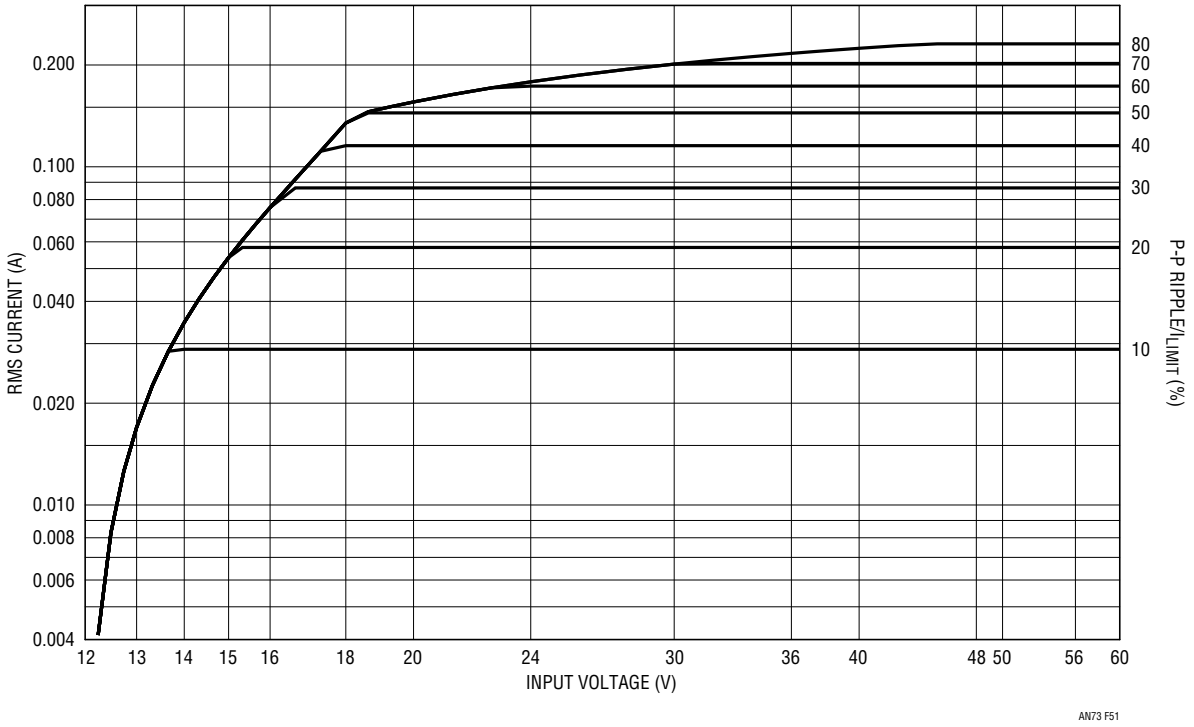


Figure 51. 12V Output Normalized Output Capacitor AC RMS Current

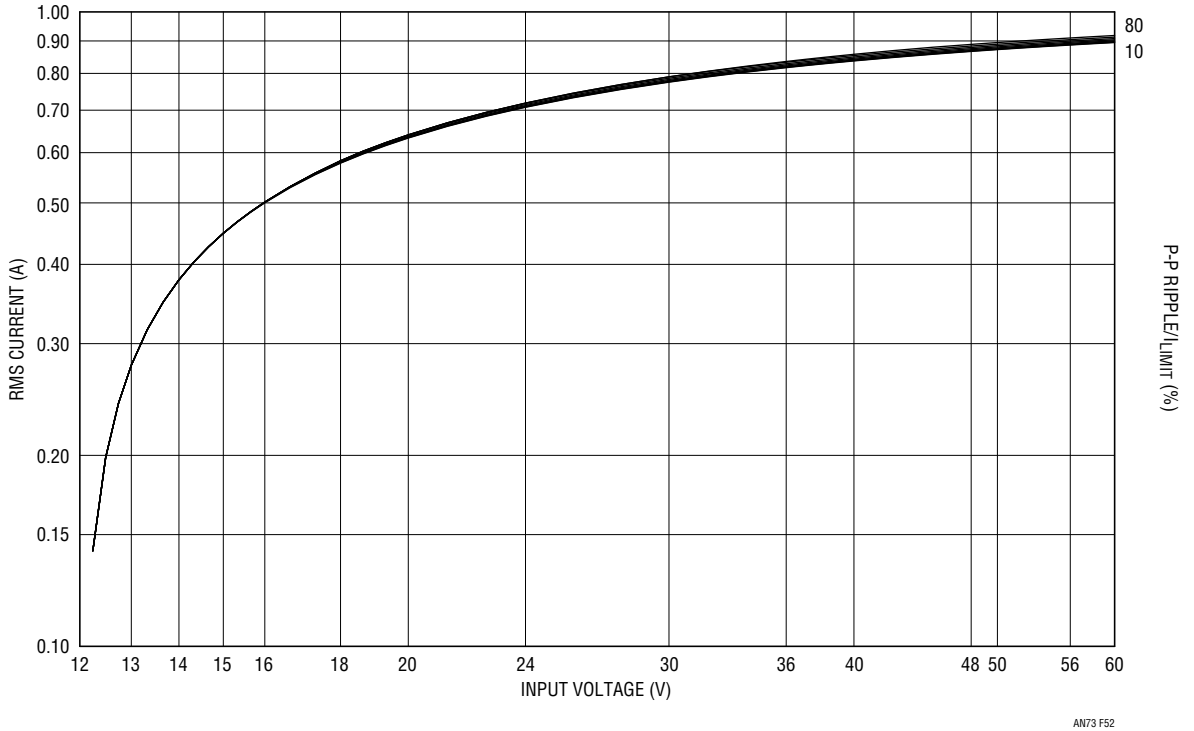


Figure 52. 12V Output Normalized RMS Bottom Transistor Current

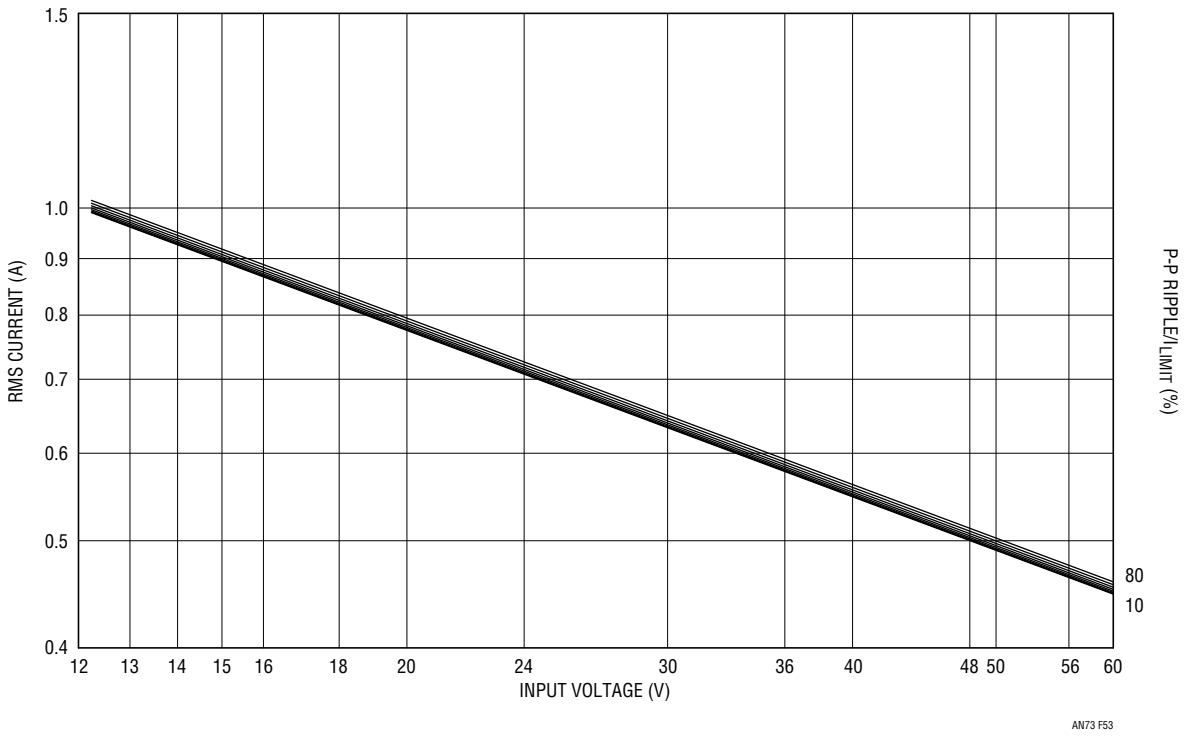


Figure 53. 12V Output Normalized Top Switch RMS Current

24V OUTPUT GRAPH SET

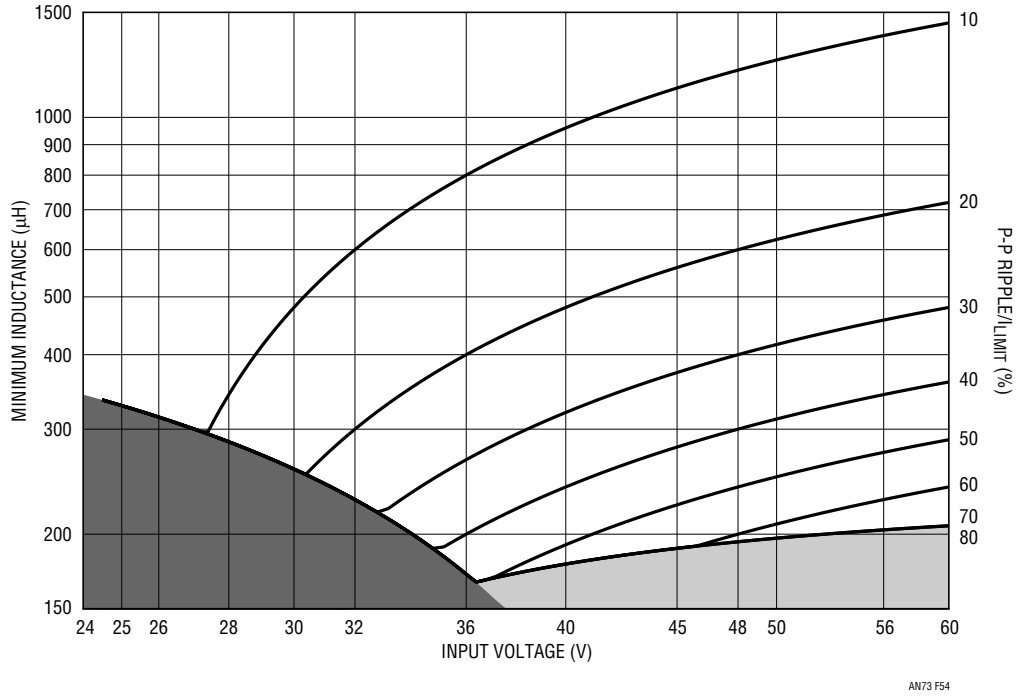


Figure 54. 24V Output Normalized Minimum Inductor Value

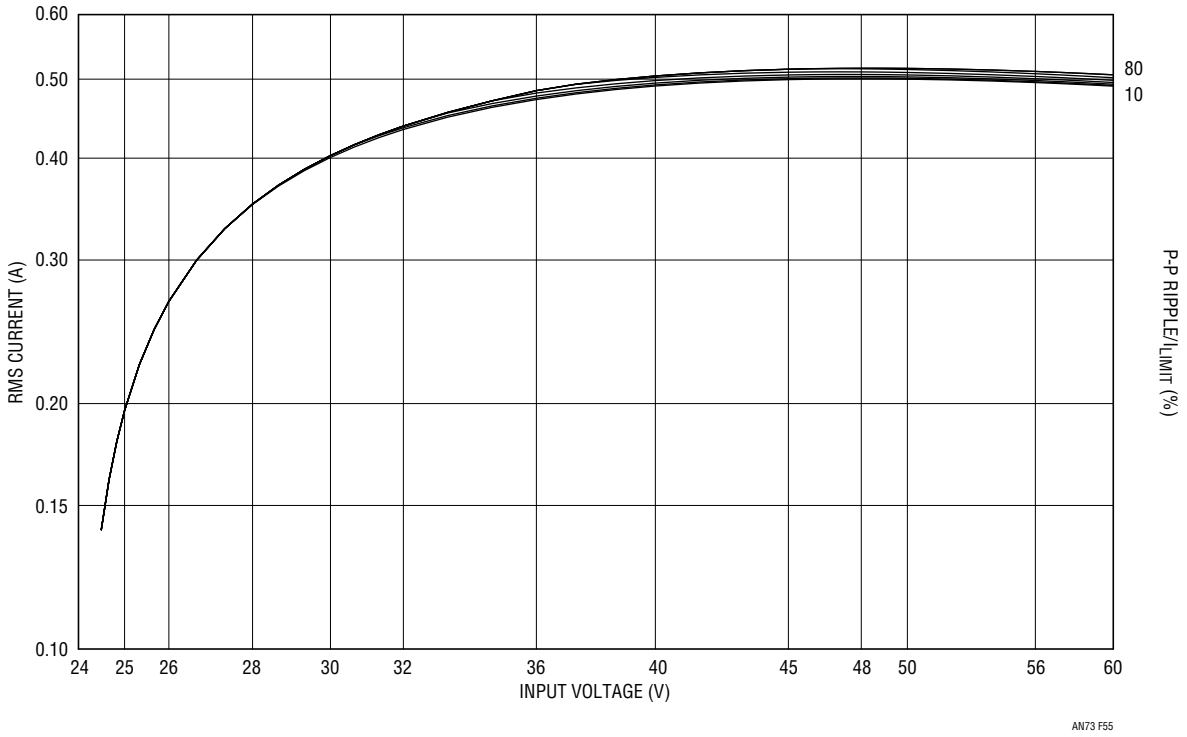


Figure 55. 24V Output Normalized RMS AC Input Capacitor Current

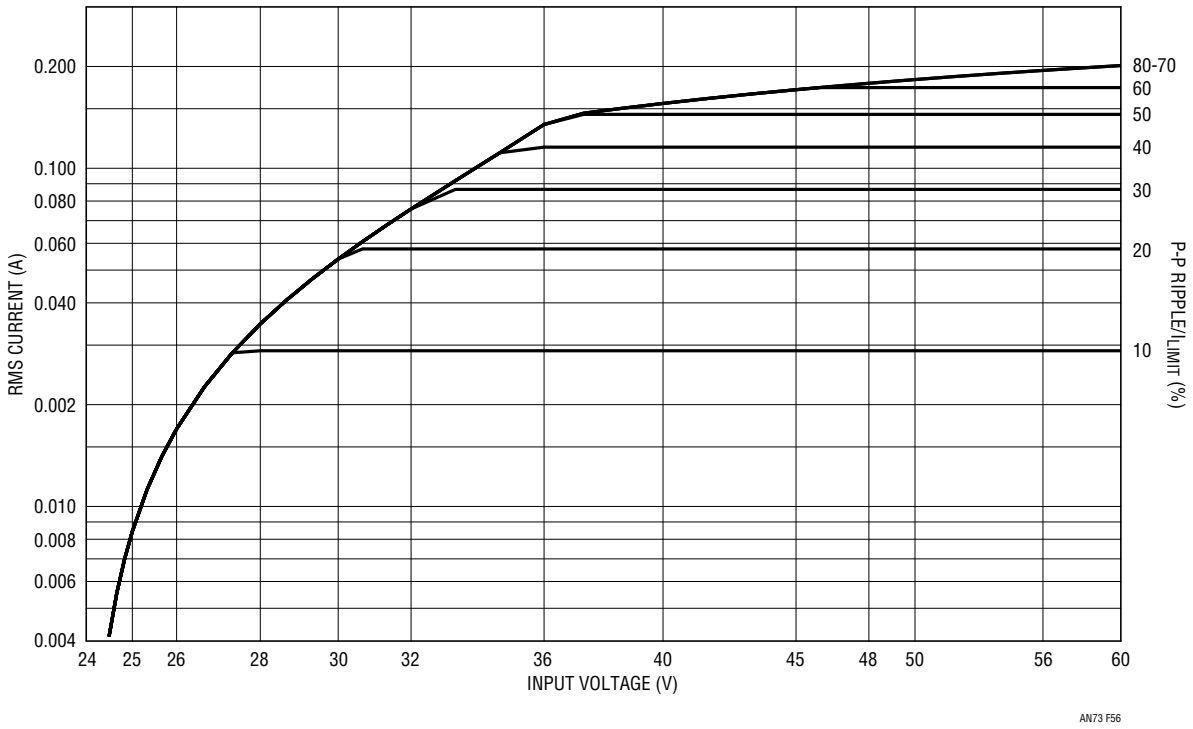


Figure 56. 24V Output Normalized Output Capacitor AC RMS Current

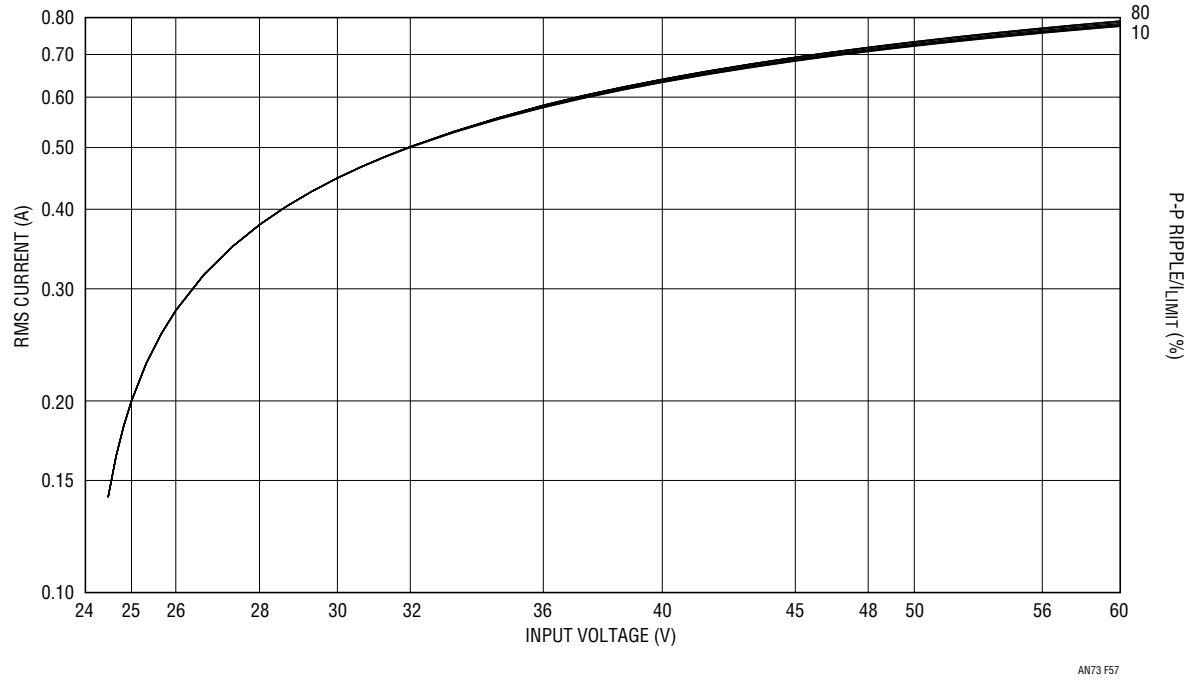


Figure 57. 24V Output Normalized RMS Bottom Transistor Current

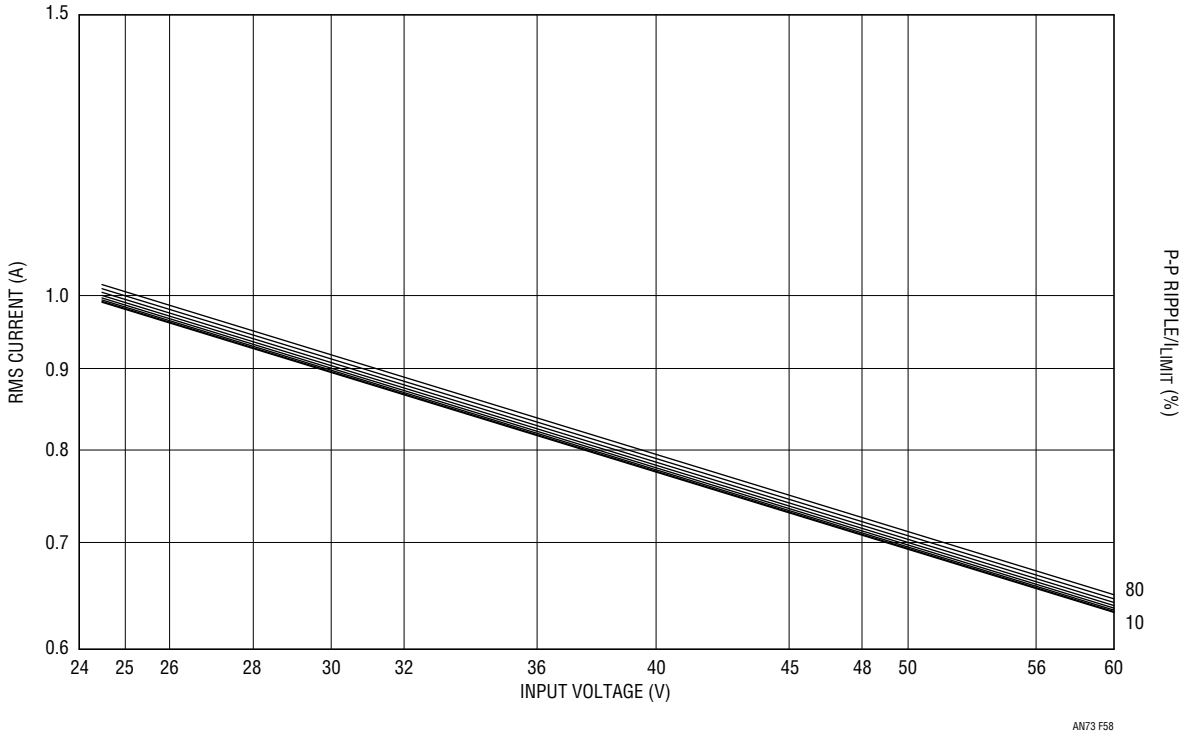


Figure 58. 24V Output Normalized Top Switch RMS Current

HOW TO CONVERT RMS CURRENT IN A CAPACITOR TO PEAK-TO-PEAK RIPPLE VOLTAGE

Figure 59 is a guide to assist in output capacitor selection and/or estimating peak-to-peak output ripple voltage. Divide the output ripple specification (expressed in mV_{P-P}) by the maximum output capacitor RMS current obtained from the design graphs to determine the effective resistance needed in the output capacitor. Using the right-hand scale of Figure 59, follow the isocline that approximates the needed effective resistance, calculated above. Looking at the scale to the left, determine the maximum allowable value for total capacitor ESR. Pick a capacitor for the output, and plot its capacitance and ESR on Figure 59. If the point is outside the effective-resistance isocline, you will either need to pick another capacitor or parallel multiple capacitors.

Here are the rules for paralleling capacitors:

1. You must parallel capacitors of the same capacitance and ESR to correctly use Figure 59.
2. Paralleling *n* capacitors into a block will move you to higher ground on the graph:
   - The RMS ripple current of the block will be *n* × the RMS ripple current of one capacitor.
   - The ESR of the block will be the ESR of one capacitor/*n*.
   - The capacitance of the block will be *n* × the capacitance of one capacitor.
3. Derate the capacitor block for end-of-life considerations (ESR doubles and the capacitance drops by 50%).
4. When using ceramic-type capacitors, the ESR is usually so low that only the block capacitance need be considered.
5. With aluminum and tantalum capacitors, you will probably be paralleling capacitors to get low enough block ESR to cross the isocline.

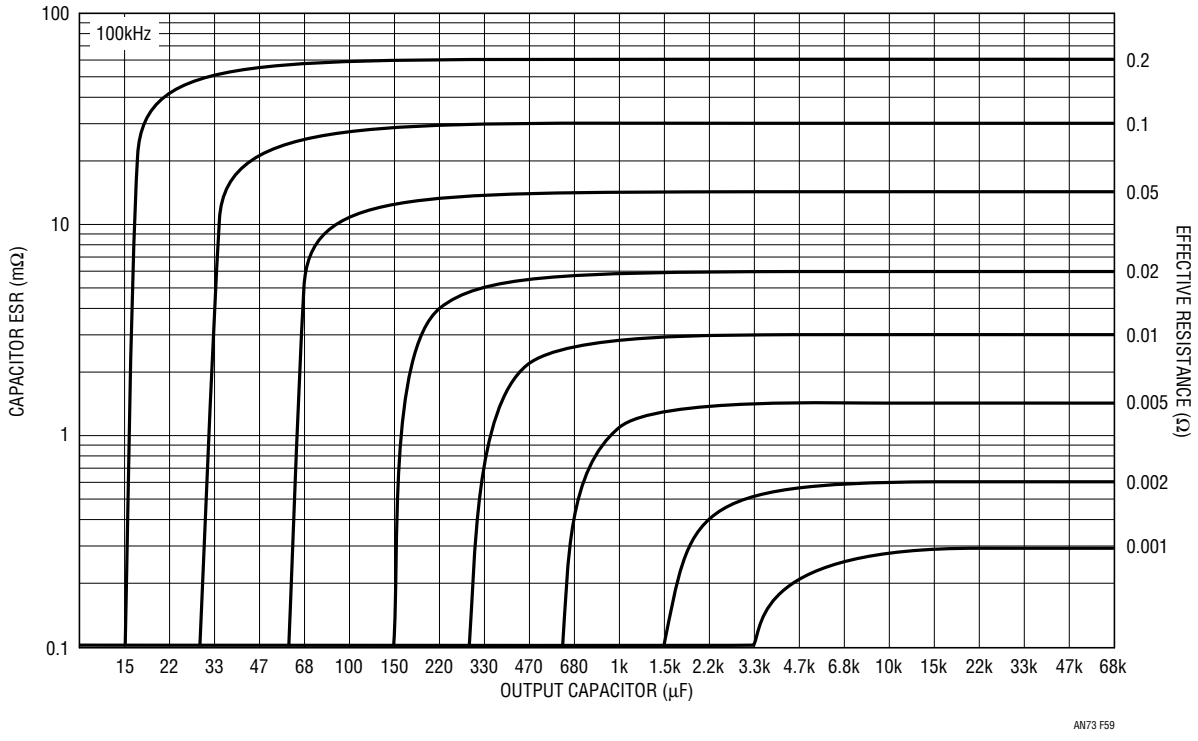


Figure 59. RMS Current to Peak-to-Peak Ripple

6. If you are tempted to parallel a 15µF, 0.001Ω ceramic capacitor with a 1000µF, 0.01Ω aluminum capacitor in order to get a 1015µF, 0.0009Ω capacitor, you will be surprised by the result:
   - Plot the 15µF, 0.001Ω capacitor on Figure 59.
   - Traverse the elevation isocline to its terminus at the right side of the graph and read its effective resistance (~0.22Ω).
   - Plot the 1000µF, 0.01Ω capacitor and follow its isocline to the right side terminus, read its effective resistance (0.04Ω)
   - Parallel the two impedances: 0.22 || 0.04 = 0.034; an effective resistance far more affected by the aluminum capacitor than the ceramic.
   - At 100kHz, a 100µF, 0.001Ω ceramic capacitor has about the same effective resistance as a 1000µF 0.01Ω aluminum electrolytic.

DENORMALIZING FIGURE 59 FOR OTHER FREQUENCIES

As far as Figure 59 is concerned, a 100µF capacitor at 100kHz will look like a 60µF capacitor at 60kHz. All other parameters stay the same. To plot a capacitor of *x*µF operating at *y*kHz, first calculate a new capacitance, *z*, where *z*(µF) = *y*(kHz)/100kHz • *x*(µF), then plot on Figure 59 using its native ESR value.

BOOST CONVERTERS

OVERVIEW

The boost converter is a converter that has an output voltage greater than its input voltage. Its input is a voltage that varies over the regulator's input range and its output is a constant voltage.

Switching boost converters have current division, in that the output current will be less than the input current. In an ideal boost converter, the ratio of output current to input current is the same as the ratio of input voltage to output voltage (100% efficiency).

Characteristics of the Synchronous Switching Boost Converter

The synchronous boost converter has the following characteristics:

1. It has a maximum input voltage that can be tolerated while providing rated output voltage. For the power converter (the LT1339 and its associated components), this voltage is usually limited first by the minimum duty factor and finally by the body diode of the top MOSFET. Excursions of input voltage above the output voltage result in uncontrolled rise in output voltage.
2. There is a minimum input voltage where boost conversion can be performed. Here several factors come into the picture: undervoltage lockout, current mode instability, average input current limit (if used) and peak current limit.

   In the boost converter the undervoltage lockout is used to prevent operation where the performance or robustness of the design would be compromised. Because of the negative input impedance of a boost converter, the input current increases as the input voltage drops. This increase in input current is accompanied by higher RMS currents throughout the power converter. Especially significant is the RMS output ripple current in the output capacitor. Undervoltage lockout is often used to prevent operation at duty factors where current mode instability would cause undesirable (audible) operation. Finally, undervoltage lockout is used to prevent operation with insufficient gate drive voltage.
3. The output current is discontinuous, with high AC RMS values that require large output capacitors just to accommodate the high AC current. This is also manifested in high output ripple voltage; an output filter may be required to keep the switching frequency ripple from disrupting the load.
4. The input current is continuous and has a triangular/sawtooth wave shape. This means small input capacitors and low input ripple voltage.
5. There is a forward parasitic power path; hence, shutting down the boost converter leaves a power path from input through the choke and body diode of the top MOSFET to the output. There is no provision for current limiting in this parasitic power path. Shorting the output of a boost converter can be disastrous, depending upon the current capability of the input source. This path exits both when the converter is operating and when it is in shutdown.
6. The average current limit function in the LT1339 monitors input current rather than output current. The maximum output current will depend on input voltage. If the average current limit loop is not used (I_{AVE}, Pin 5 grounded), the output current will be limited by the peak input current limit. Under this condition the maximum output current will depend on both the input voltage and the inductor value, and the amount of slope compensation used.
7. There is a parasitic reverse power path at the input. If the input is pulled below ground, current flows through the body diode of the bottom MOSFET, through the inductor, through the sense resistor and out. Were you to connect a car battery to the input of a synchronous boost converter backwards, very small resistances would limit current. This is not recommended.
8. There is a parasitic reverse power path at the output. If the output is pulled below ground, the equivalent circuit simplifies to two diodes to ground. These diodes, the body diodes of the MOSFETs, are all that stands between your circuit and disaster. When reverse polarity output voltage is applied, there is no built-in mechanism to limit reverse current.
9. If the output voltage is pulled below the input voltage, the body diode of the top MOSFET conducts to supply

power from the input to the output. If you have a car battery as the input, don't short the output.

10. Inductor value is not extremely critical; increasing the inductor value above the required minimum nets small returns. The main effect will be seen at minimum input voltage, where the inductor value will affect the stability of the current mode engine. If current mode instability is a problem, increasing the inductor value or adding additional slope compensation will be required.
11. Efficiencies range from the low 80%s to the high 90%s.
12. Several things should be considered when selecting a switching frequency. Higher switching frequency is usually accompanied by a smaller inductor, lower input, and output ripple voltages. In some cases higher switching frequency can allow the use of smaller or cheaper output capacitors. However, higher switching frequency is often accompanied by higher wire loss and core loss in the inductor, higher switching loss, and more drive power required by the MOSFETs. For the modern core materials, capacitors and MOSFETs, the most suitable frequency typically falls in the 50kHz to 125kHz region.

GRAPHICAL DESIGN SECTION

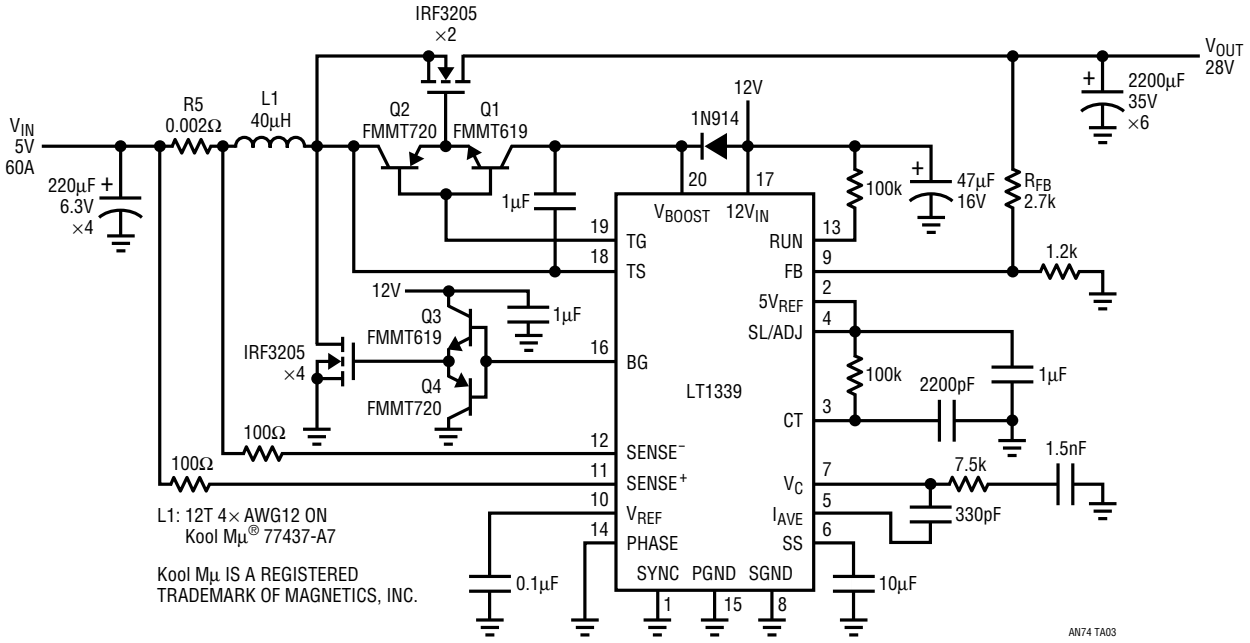
A boost converter can be designed using Figures 60 to 66 to select the inductor value. In boost mode, current mode stability is more of a problem, as can be seen by the respectively larger regions in the graphs where current mode stability is a problem. Once an inductor value and its ripple current are selected for the boost converter, the balance of the design is done using the graphs in the buck design section. Using these graphs with the input and output voltages in reversed roles will provide the correct answers. Keep in mind that the input capacitor and output capacitor have reversed roles also. Their ripple current charts should be applied accordingly.

CONCLUSION

As with the buck regulator design section, the use of the graph can simplify the design of most boost designs. If for some reason your application cannot be handled by the graphical method detailed here, the data sheet has equations that lead you through the design process.

As with any of our products, if these tools do not provide enough design support, call us. We will help you design a system that will meet your needs, or we will help you debug a design that isn't performing to specification.

5V/60A Input to 28V/9A Boost Converter



CIRCUIT COLLECTION

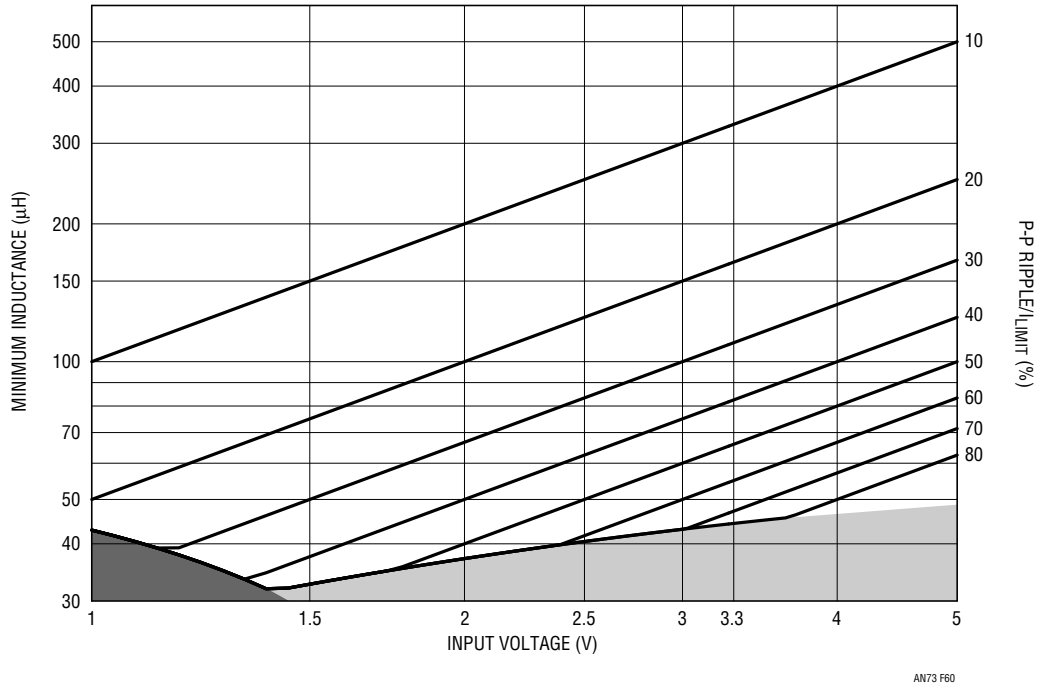


Figure 60. 5V Output Normalized Minimum Inductor Value

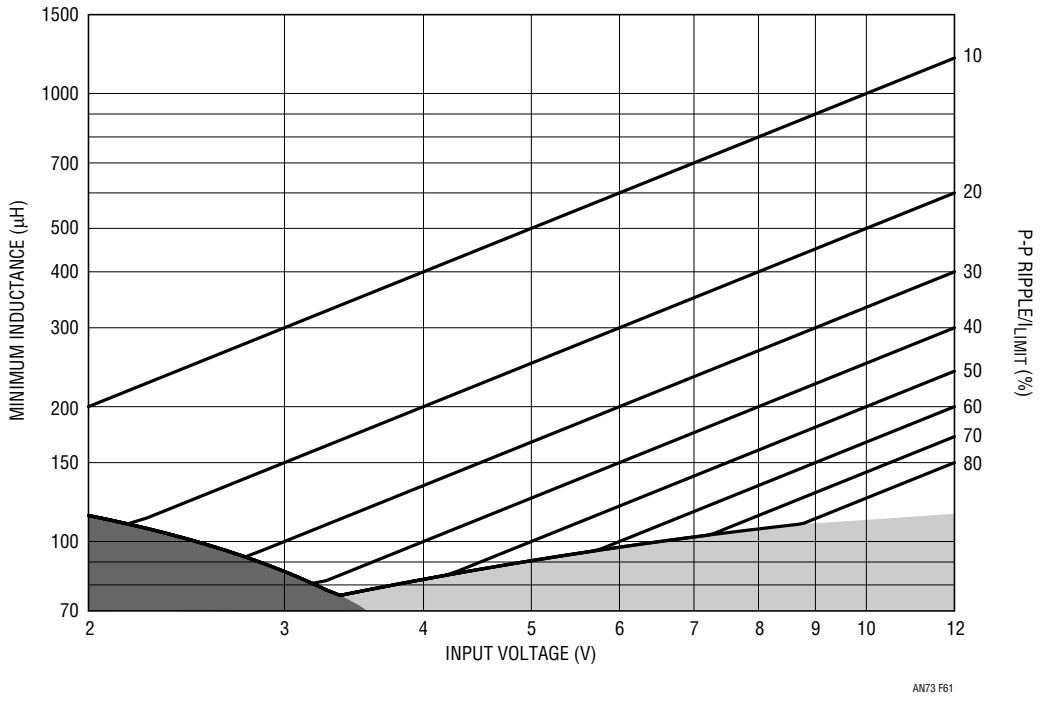


Figure 61. 12V Output Normalized Minimum Inductor Value

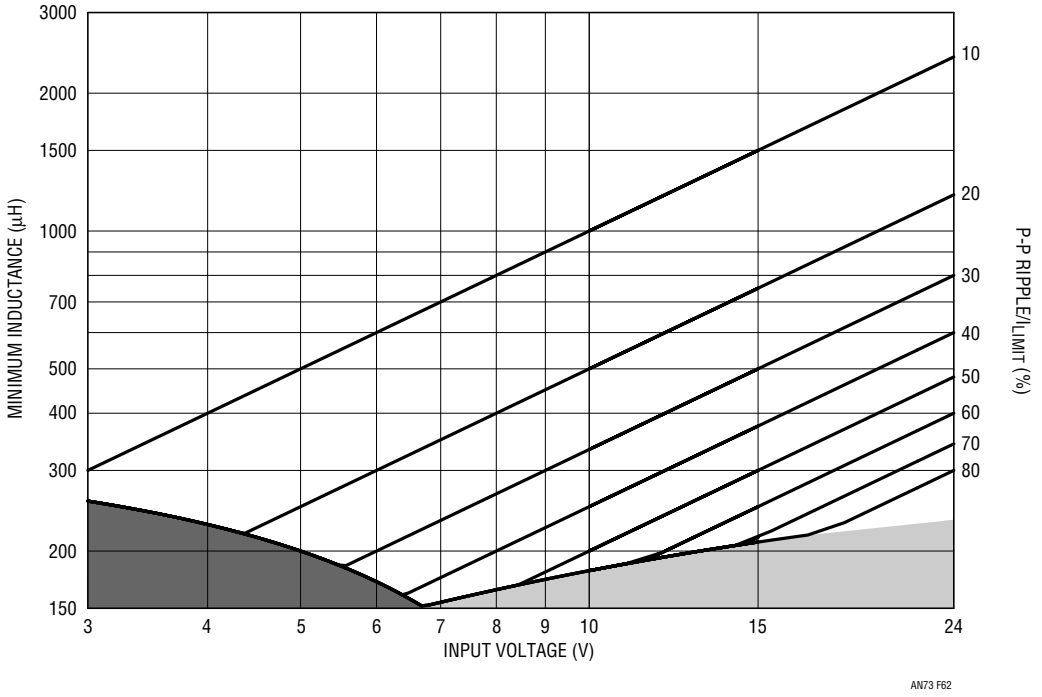


Figure 62. 24V Output Normalized Minimum Inductor Value

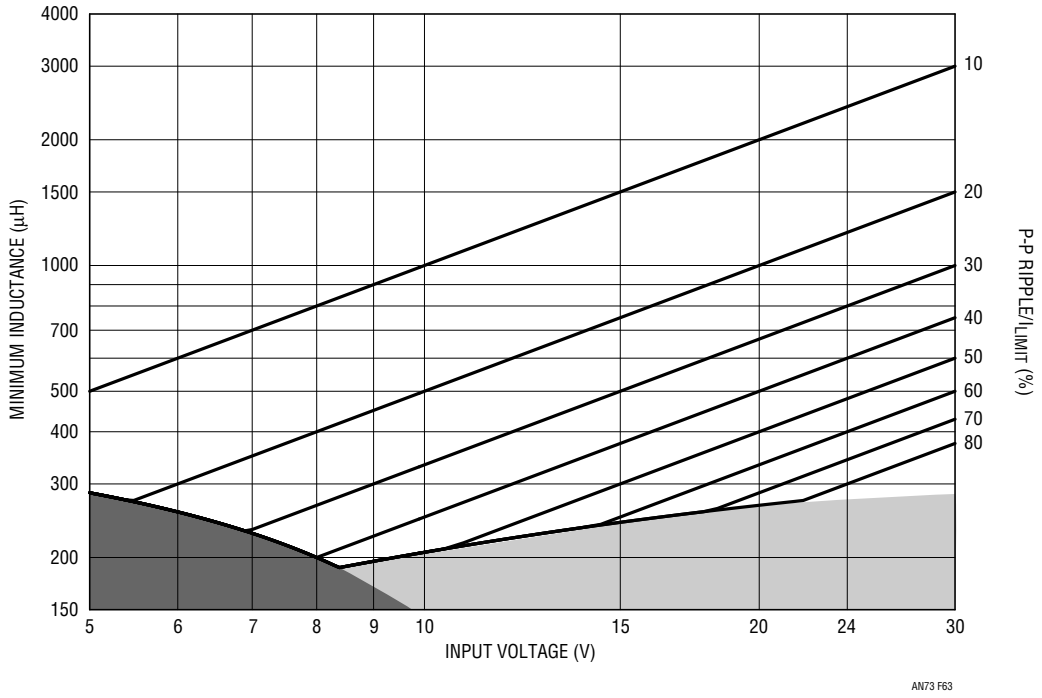


Figure 63. 30V Output Normalized Minimum Inductor Value

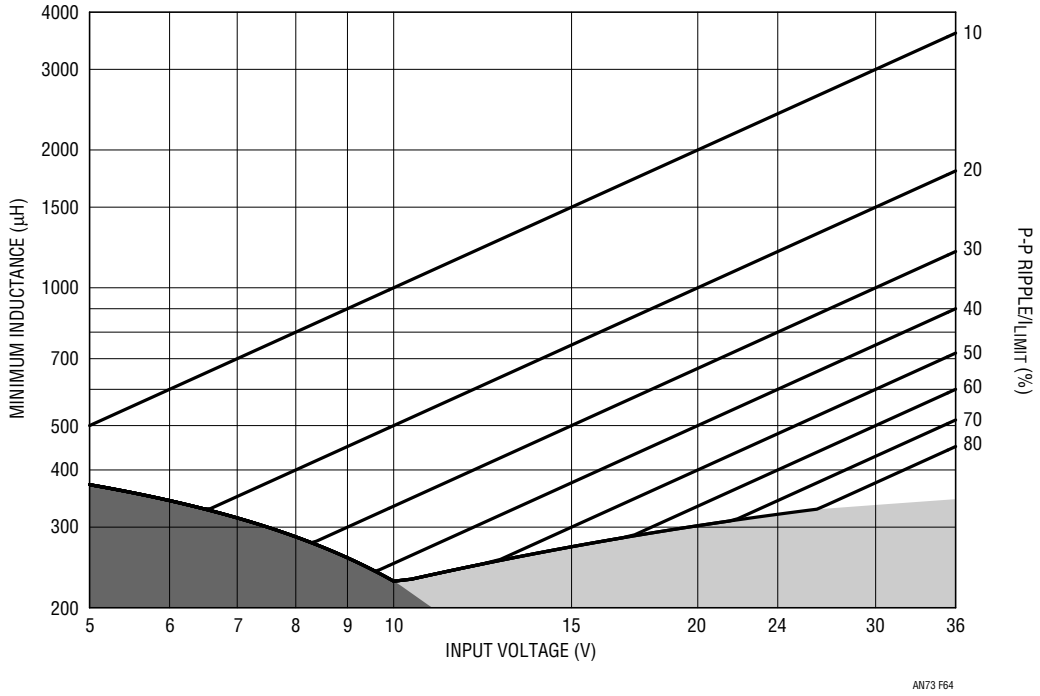


Figure 64. 36V Output Normalized Minimum Inductor Value

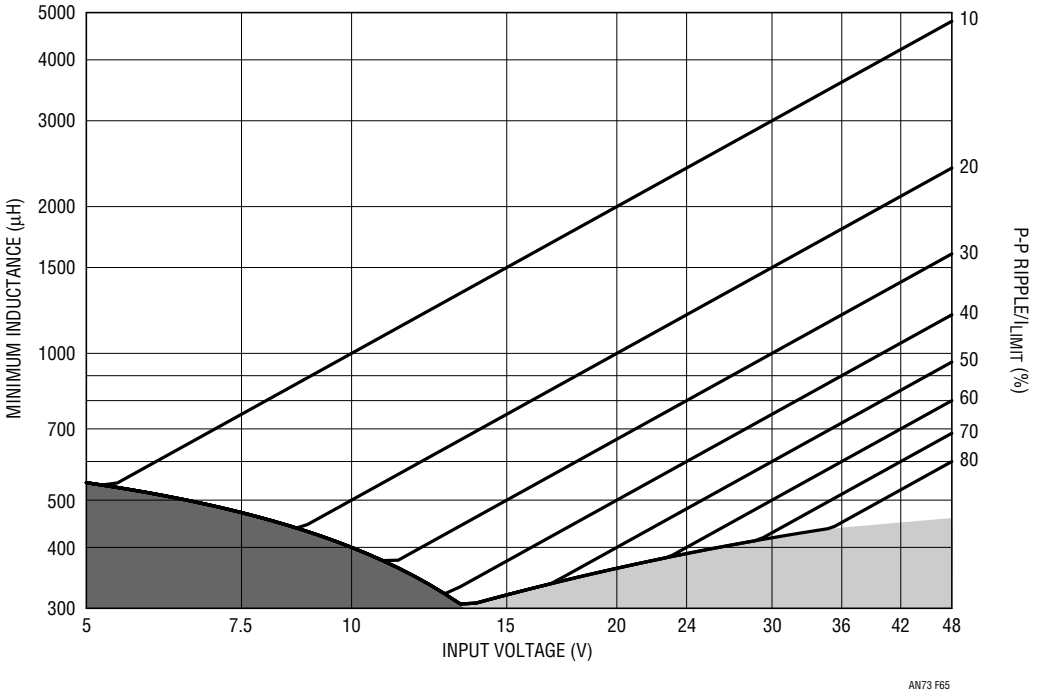


Figure 65. 48V Output Normalized Minimum Inductor Value

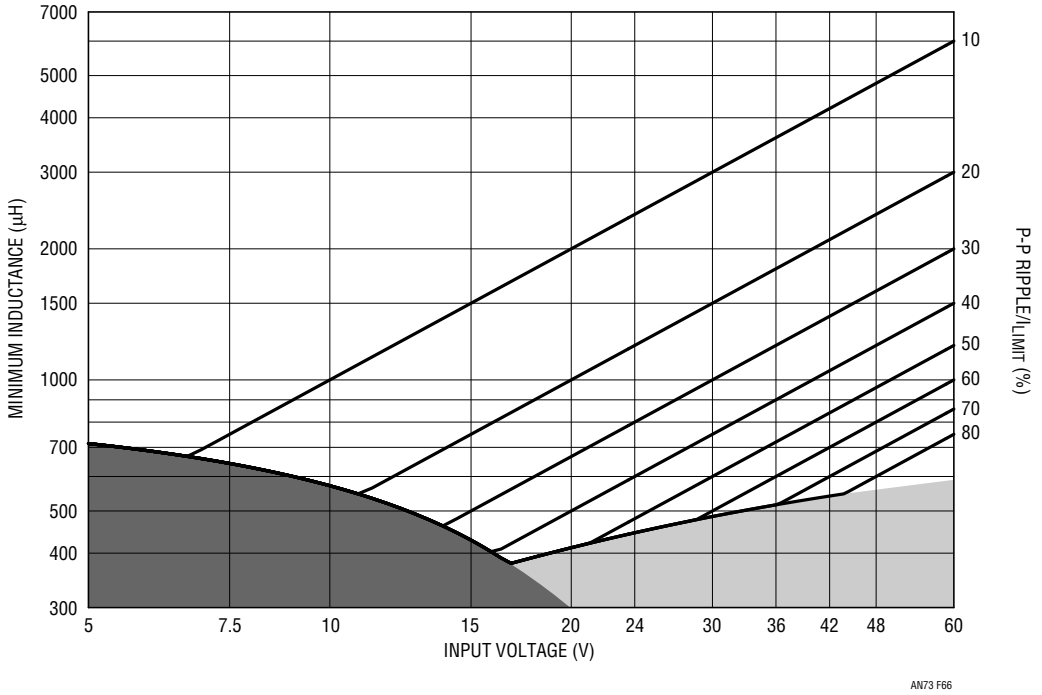
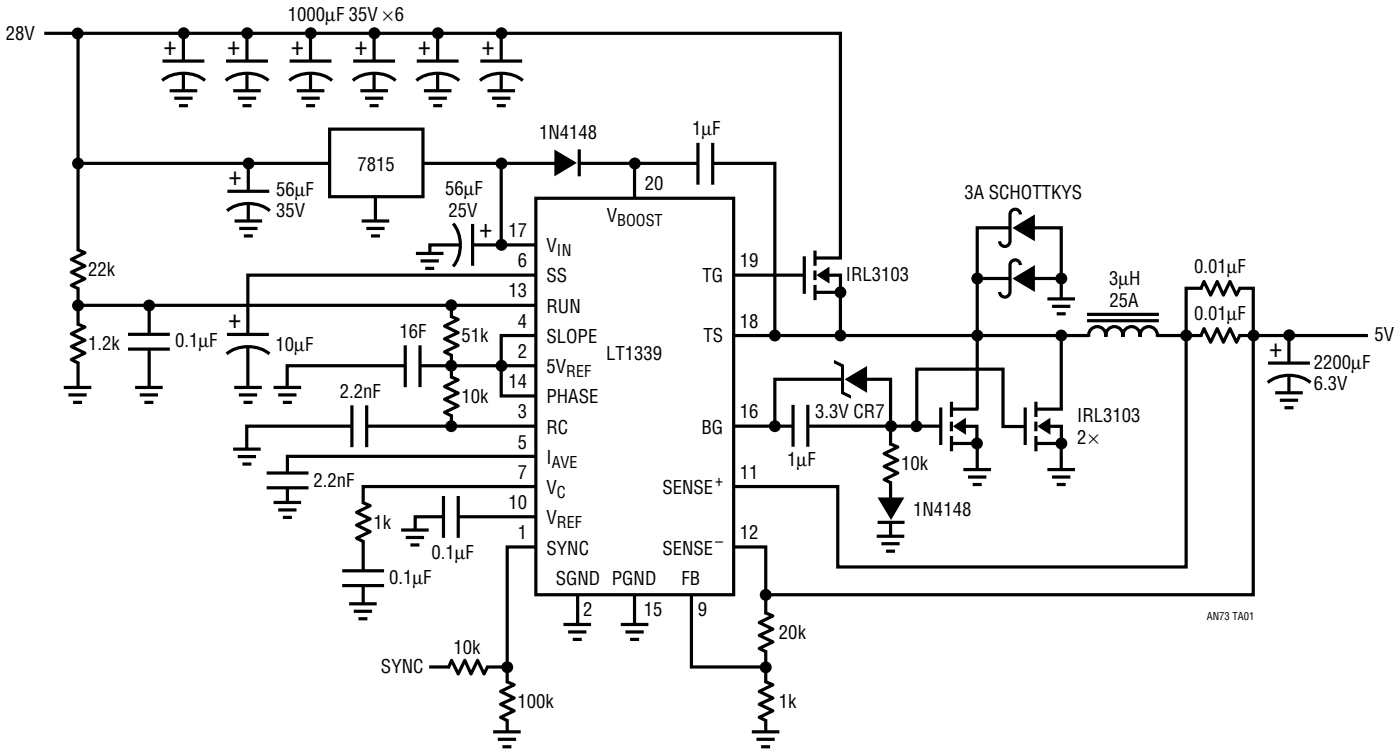


Figure 66. 60V Output Normalized Minimum Inductor Value

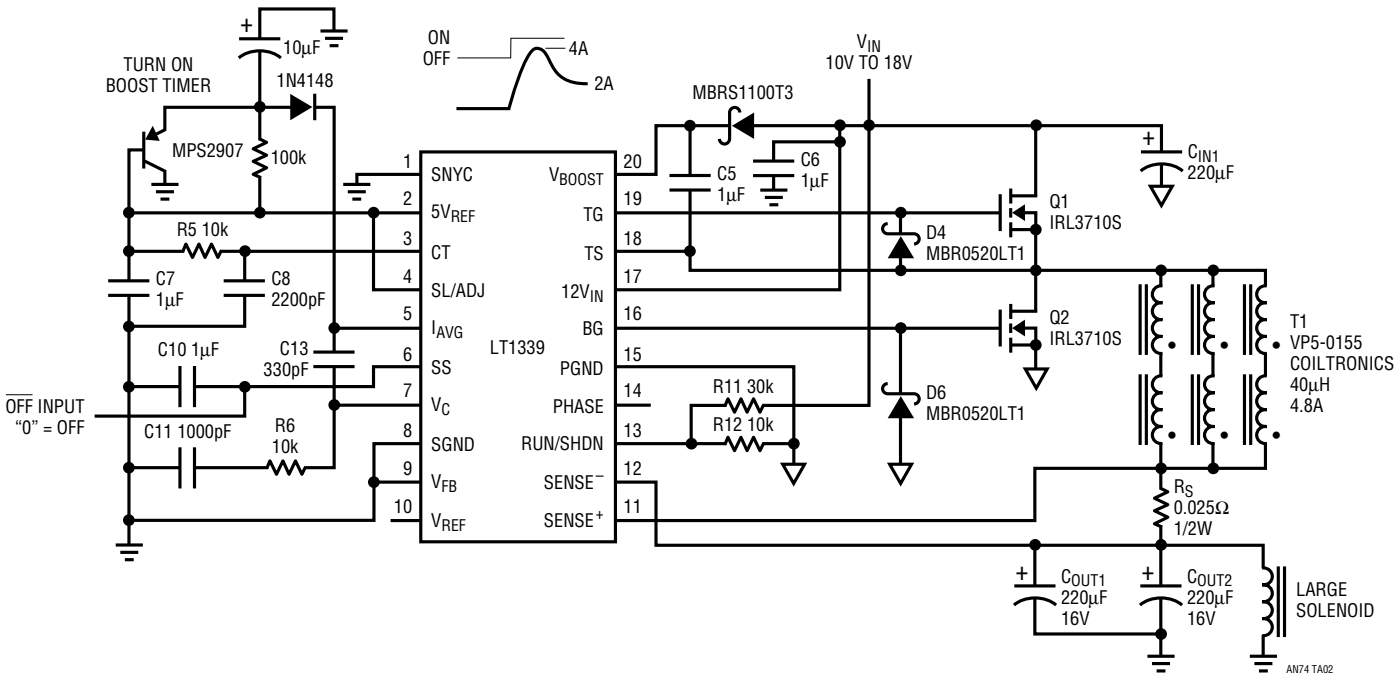
TYPICAL APPLICATIONS

28V to 5V/20A Buck Converter

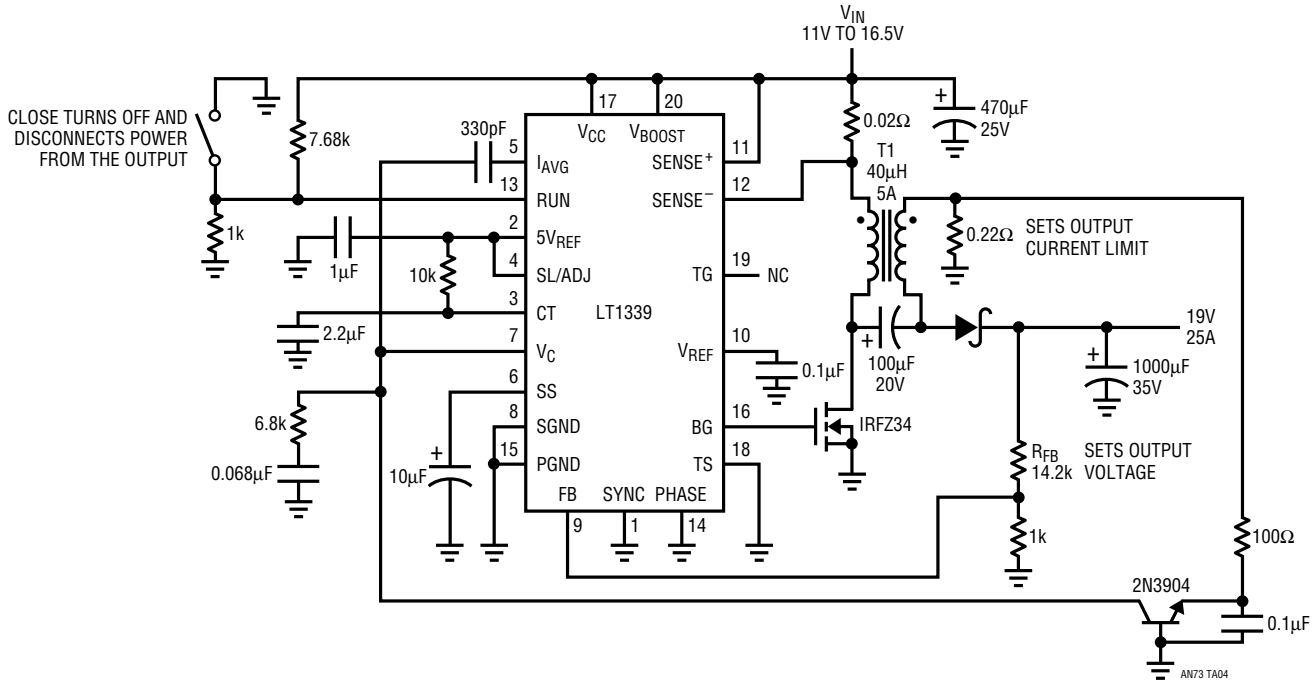


TYPICAL APPLICATIONS

Constant-Current Solenoid Driver with 2× Turn-On Boost



2.5A SEPIC Converter. The Output Voltage Can Be Lower or Higher Than the Input Voltage



Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7487
(408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977
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