SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

INTRODUCTION TO A 10A MONOLITHIC SWITCHING REGULATOR IN MULTIPOWER-BCD TECHNOLOGY

by C.Diazzi

The L497X series of high current switching regulator ICs exploit Multipower-BCD technology to achieve very high output currents with low power dissipation – up to 10A in the Multiwatt power package and 3.5A in a DIP package .

Switched mode techniques led to the development of high efficiency circuits offering space saving and a reduction in costs, mainly of the heatsink and output LC filter. For these applications a new technology, called MULTIPOWER-BCD, has been developed which allows the integration on the same chip of isolated power DMOS elements, Bipolar transistors and CMOS logic.

The technology is particularly suitable for the problems rising in the switch mode field, due to the characteristics of high efficiency, fast switching speed, no secondary breakdown of the power DMOS element.

The great flexibility that we have at our disposal for the choice of the signal and driving sections components allows optimization and compactness of the system. With MULTIPOWER-BCD it has been possible to implement the family L497X, a new series of fully integrated switching regulators suitable for DC-DC converters working in Buck configuration. The complete family consists of five devices which differ each other only by the output current value (2A, 3.5A, 5A, 7A, 10A) they can deliver to the load. The devices rated at 2A and 3.5A are assembled in Power Dip (16+2+2), while the others are assembled in the Multiwatt15 package. Each device integrates a DMOS output power stage, a control section, limiting current and supervisor functions like Reset and Power Fail signal for microprocessors applications.

Output voltage can be adjusted starting from the internal reference voltage (5.1V) up to 40V, allowing a maximum output power of 80W for the 2A version and of 400W for the 10A version. Maximum operating supply voltage is 55V.

THE TECHNOLOGY

The technology architecture is based on the vertical DMOS silicon gate process that allows a channel length of 1.5 micron ; using a junction isolation technique it has been possible to mix on the same chip Bipolar and CMOS transistors along with the DMOS power components (Fig. 2). Figure 1 shows how this process brings a rapid increase in power IC complexity compared to conventional bipolar technology.

Figure 1: BCD process and increase in power ICs complexity.

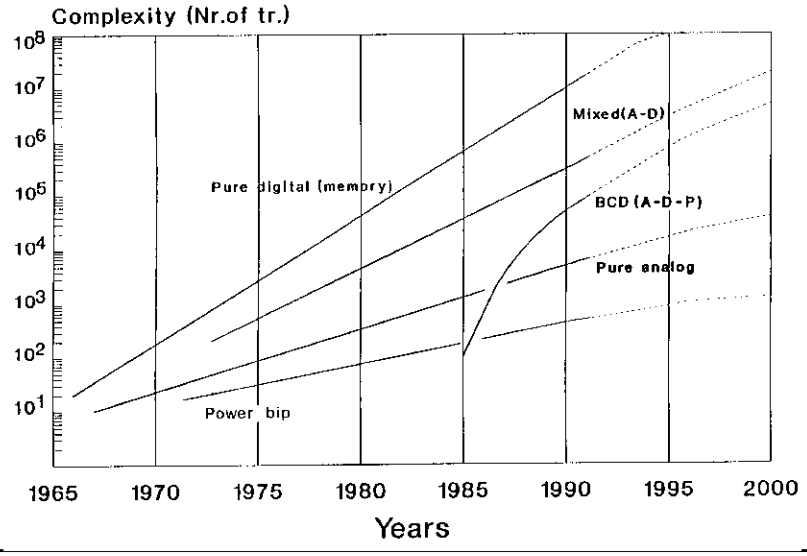
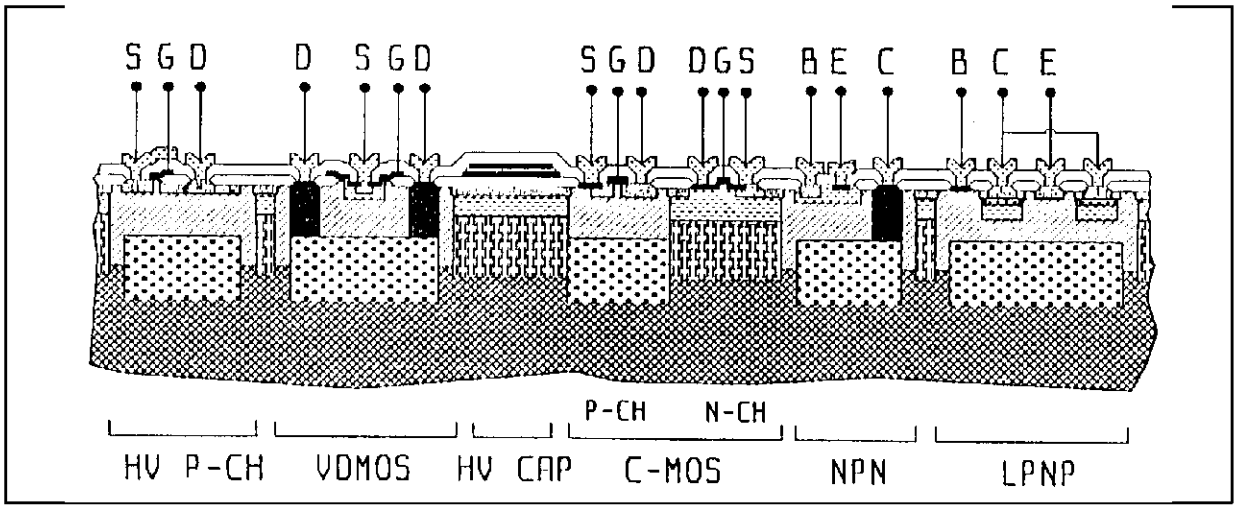


Figure 2: Cross section of the BCD mixed technology.



In the 70's class B circuits and DC circuits allowed output power in the range of 70W. By 1980 ,with the introduction of switching techniques in power ICs, output powers up to 200W were reached ; with BCD technology the output power increased up to 400W.

FUNCTIONS AND BLOCK DIAGRAM

The complete block diagram of the high power L4970A is shown in fig.3. Each block is analysed in the following.

POWER SUPPLY

The device is provided with an internal stabilized power supply (Vstart =12V), that provides the supply voltage to the analog and digital control blocks and also the supply voltage to the bootstrap section. The Vstart voltage supplies also the internal Reference Voltage section that provides accurate 5.1V voltage to the control loop. Through trimming techniques the 5.1V reference is within +- 2% limits.

OSCILLATOR and FEDFORWARD

The oscillator block (fig.4) generates the sawtooth

Figure 3: Block diagram of the 10A monolithic regulator L4970A.

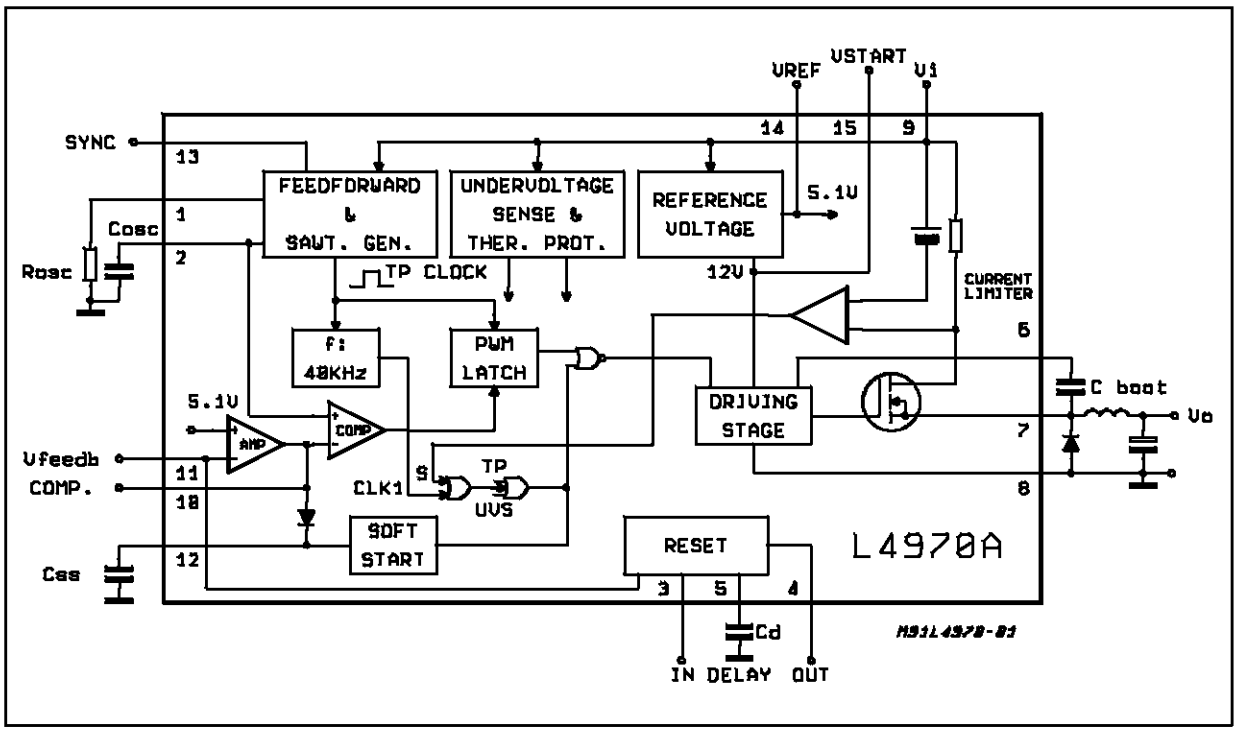


Figure 4: Oscillator circuit.

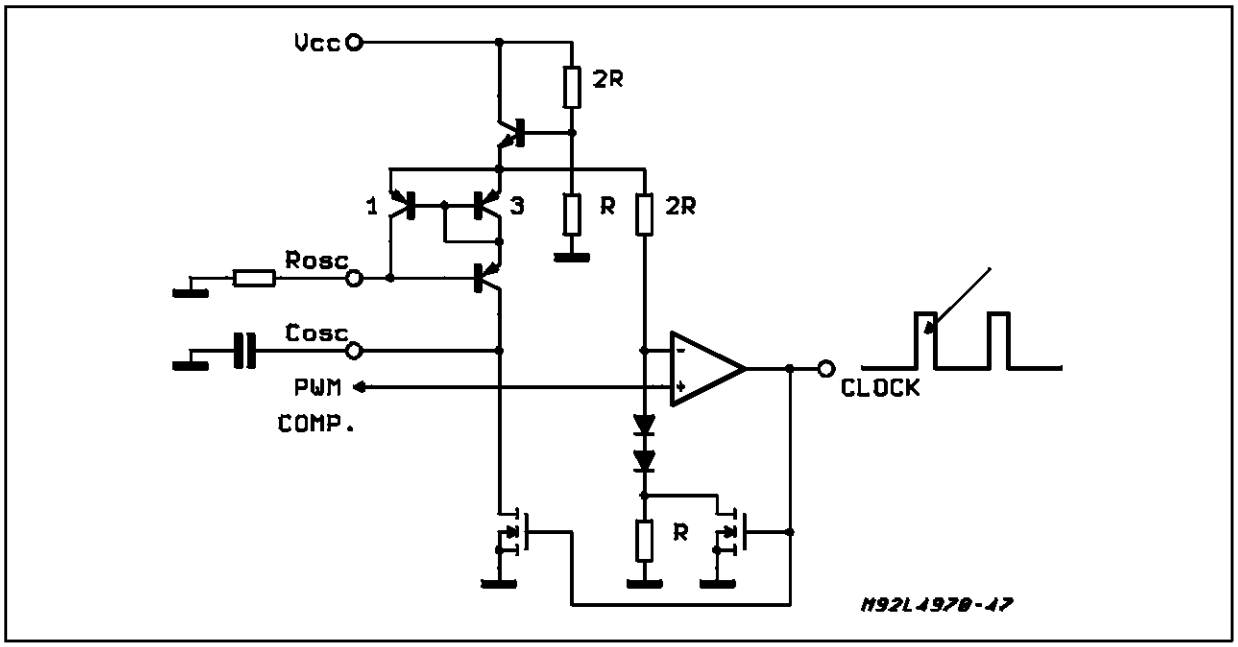
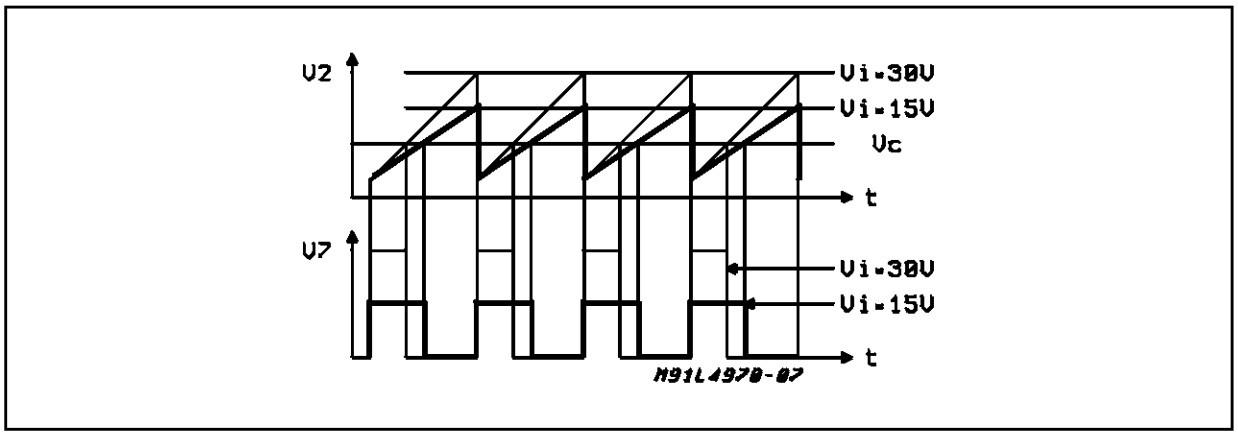


Figure 5: Voltage Feeforward waveform.



waveform that sets the switching frequency of the system. The signal, compared with the output voltage of the error amplifier, generates the PWM signal to be sent to the power output stage. The oscillator features a voltage feed-forward technique which is completely integrated and doesn't require any external component. Feed-forward function works in the supply voltage range 15-45V. The rate of increase of the sawtooth wavw-form is directly proportional to the input voltage Vcc. As Vcc increases, the output pulse-width (transistor on-time) decreases in such a manner as to provide a constant "volt-second' product to the inductance(fig.5).

From fig.5 it is shown that the duty cycle changes due to the ramp increase when Vcc increases. The error amplifier output doesn't have to change to keep the loop in regulation. This feature increases significantly the line regulation performance.

A resistor, between Rosc and GND , defines a current that is mirrored internally to charge the oscillator capacitor on the Cosc pin. The voltage at pin.Rosc is a function of Vcc value for the implementation of the feed-forward function (oscillator slope proportional to Vcc). A comparator is sensing the voltage across Cosc capacitor and discarge it when the ramp exceedes an upper threshold proportional to Vcc for the implementation of the feed-forward function. The Cosc discharge current is internally controlled at a value of about 20 mA. The lower threshold of the comparator is about 1.3V (2VBE). Here are reported basic equations for the oscillator:

$$I_{CHARGE} = \frac{V_{CC} - 9V_{BE}}{R_{osc.}} \text{ for } 15V \leq V_{CC} \leq 45V \quad (1)$$

$$I_{DISCH} \cong 20mA \quad (2)$$

$$V_{TH.HIGH} = \frac{V_{CC} - 9V_{BE}}{9} + 2V_{BE} \text{ for } 15V \leq \leq V_{CC} \leq 45V \quad (3)$$

$$V_{TH.\,LOW} = 2V_{BE} \quad (4)$$

$$F_{SWITCH} \cong \frac{9}{R_{OSC.}\, C_{OSC.}} \quad (5)$$

Note that formula (5) does not take in account the discharge time of C_{osc}, that is not negletable working at high F_{SWITCH} (200 KHz), and that is dependent on C_{osc} value.

$$T_{DISCH.} = \frac{(V_{TH.HIGH} - V_{TH.LOW}) \cdot C_{osc.}}{20mA} \quad (6)$$

By which :

$$F_{SWITCH} = \frac{1}{\frac{R_{osc}\, C_{osc}}{9} + T_{DISCH}} \quad (7)$$

During the discharge time of Cosc a clock pulse is generated that is available on pin.SYNC and that can be used to synchronize max 3 devices of the same family. See also fig. 6 and fig. 7 for the switching frequency versus value of R4 (R_{osc}).

PWM

The comparison between oscillator sawtooth and error amplifier output generates the PWM signal that feeds the driving stages. A PWM latch structure is implemented to avoid multiple pulses that could be dangerous for the power stage. A maximum duty cycle limitation is implemented in the PWM stage. Such limitation is obtained by the synchronization pulse generated in the oscillator section during the Cosc discharge time. When the pulse is present the driver is inhibited. In this way even if the error amplifier output completely overcomes the oscillator sawtooth, the power stage can not work in DC conditions, but is switched off during the clock pulse allowing a maximum duty cycle tipically in the range 90 - 95 %

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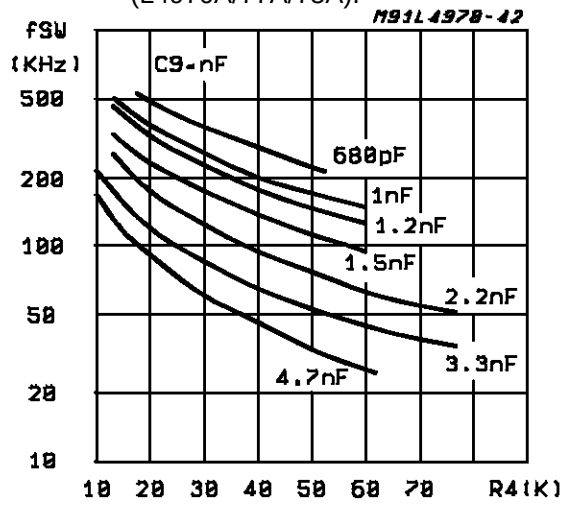
SOFT START

Soft start (see fig.8) is an essential function for correct start-up and to obtain a monotonically increasing output voltage, without overstressing the output power stage. Soft start operates at the start-up of the system and after the intervention of thermal protection. The function is realized through a capacitor connected to soft start pin, which is charged at constant current(about 100uA) up to a value of about 7V.

During the charging time , through PNP transistor Q1 the voltage at the output of the transconductance amplifier is forced to increase with the same rising speed of Css capacitor. As the capacitor is charged, the PWM signal begins to be generated as soon as the error amplifier output voltage crosses the ramp; the power stage starts

Figure 6: Switching frequency vs. R_{osc} (L4970A/77A/75A).



to switch with steadily increasing duty cycle (fig.9).

The charge of the soft-start capacitor is started every time the system begins to work after an anomalous condition occurred (undervoltage and thermal protection). The Css discharge current is in the range of about 20mA.

Figure 7: Switching frequency vs. R_{osc} (L4972A/74A).

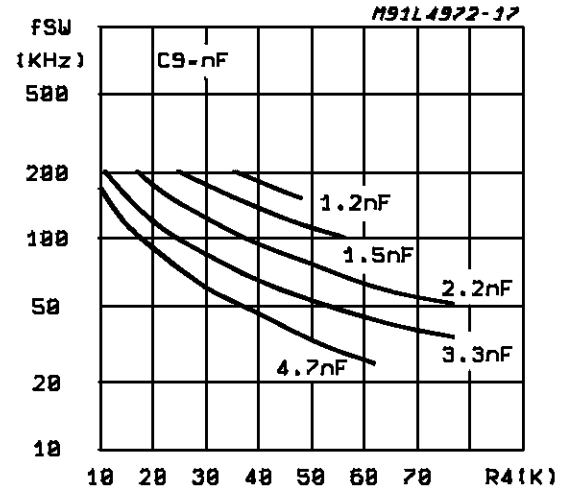


Figure 8: Soft start circuit.

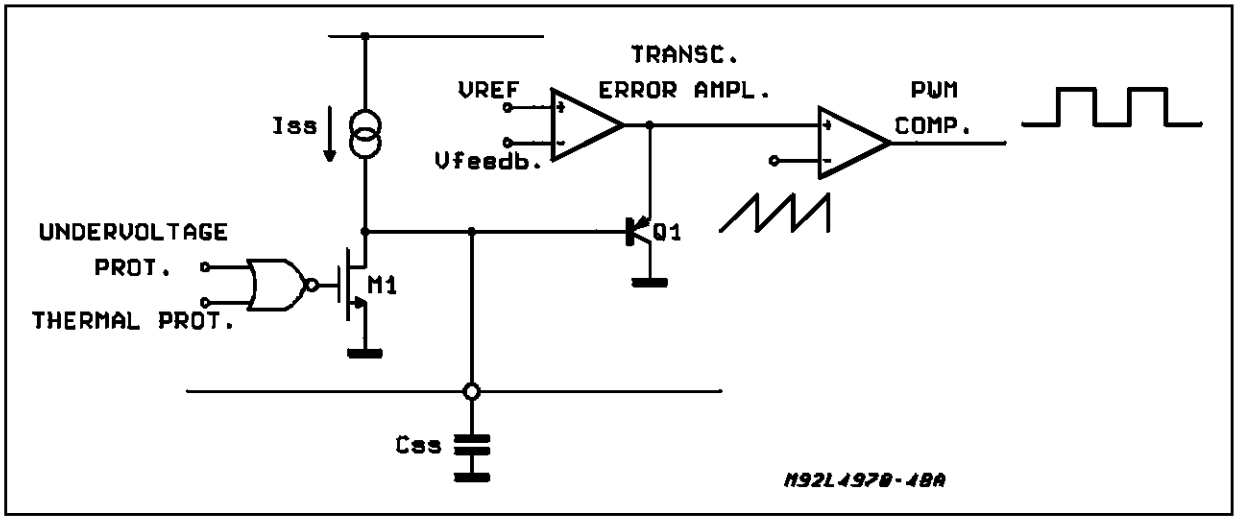


Figure 9: Soft start waveforms.

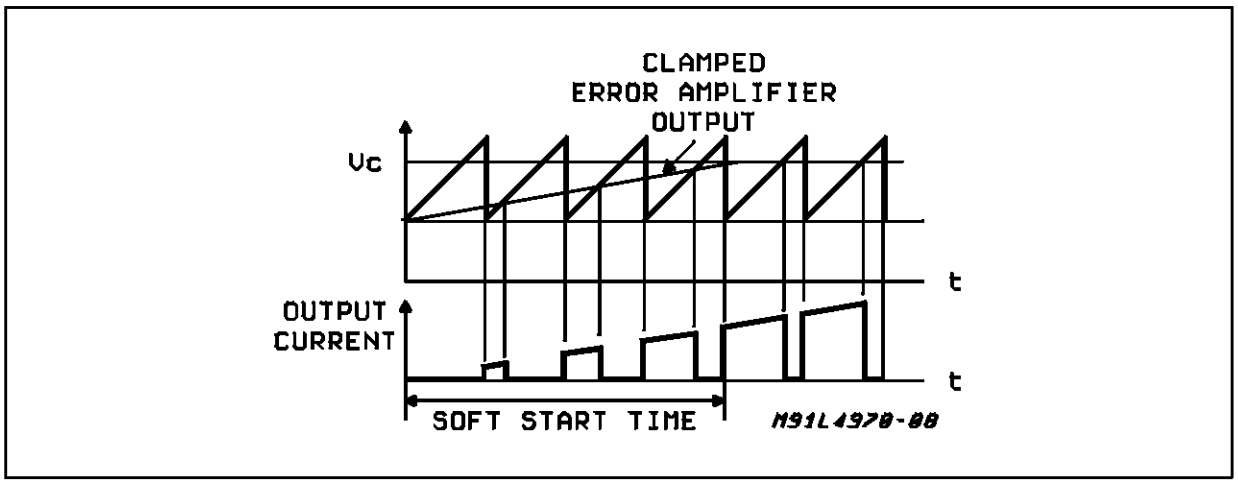
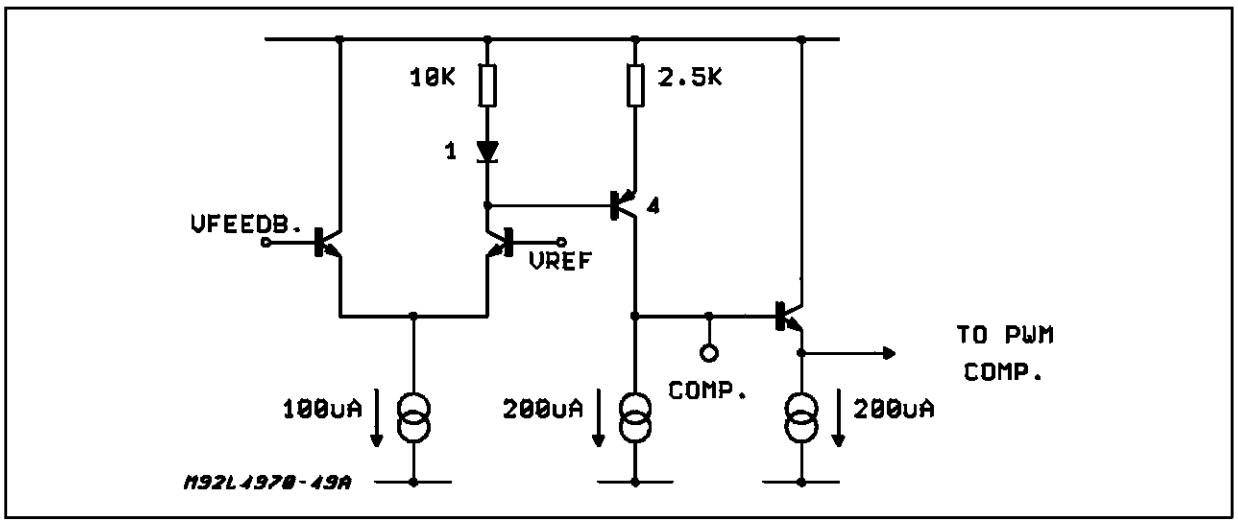


Figure 10: Error amplifier circuit.



UNDERVOLTAGE LOCKOUT

The chip features a complete built-in under voltage lock out protection, keeps the power output stage off up to the moment Vcc reaches 11v, with an hysteresis of 1V. After reaching the 11V value the system starts with the soft start feature.

ERROR AMPLIFIER

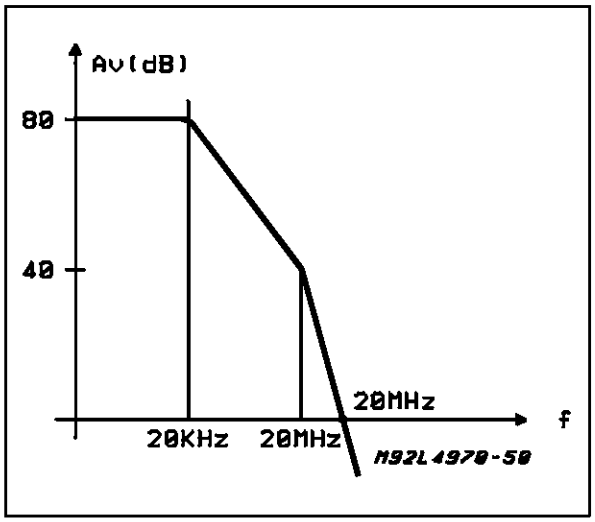
The error amplifier is a transconductance Operational Amplifier featuring a current output. The simplified schematic is represented in fig.10.

The basic characteristics of the uncompensated operational amplifier are the following:

- G_M = 4mA/V,
- R_o = 2.5Mohm,
- A_{Vo} =80dB,
- $I_{source/sink}$ = 200µA
- I_{Input} Bias Current = 0.3µA

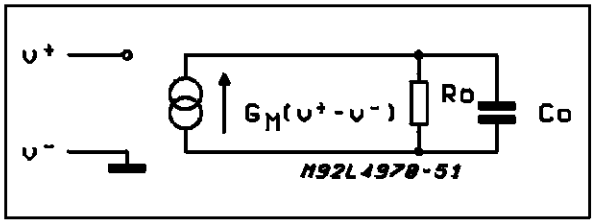
The frequency behavior of the uncompensated amplifier is reported in fig.11.

Figure 11: Open loop gain (error amplifier only).



Neglecting the high frequency behavior (in the hypotesis that in the overall frequency compensation of the loop the second pole of the operational amplifier is far below the 0 dB axis), we can make a first order approx. by which the error amplifier can be schematized by the equivalent circuit of fig.12.

Figure 12: Error amplifier equivalent circuit.



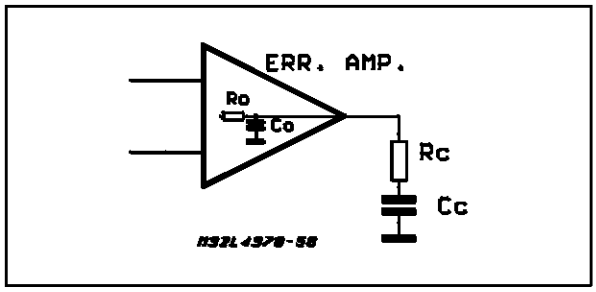
by which

$$A_V(s) = G_M \cdot \frac{R_o}{1 + SR_o C_o}$$

where C_o = 3pF.

The error amplifier is inserted in the regulation loop and can be easily compensated, thanks to its high output impedance, with a network between its output and ground. The typical compensated network is shown in fig.13.

Figure 13: Compensation network of the error amplifier.

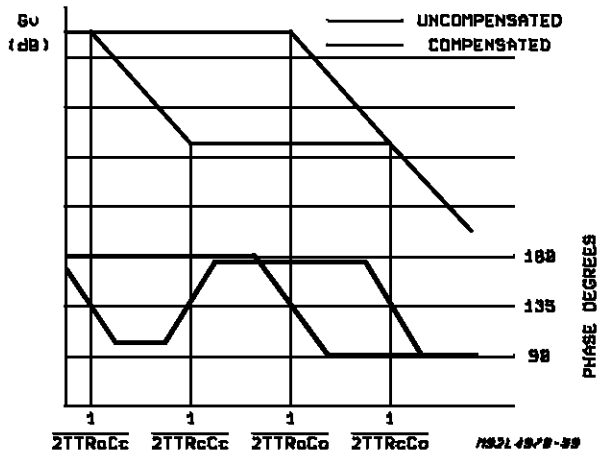


The transfer function is:

$$A_V(s) = G_M \cdot \frac{R_o (1 + S R_c C_c)}{S^2 R_o C_o R_c C_c + S (R_o C_c + R_o C_o + R_c C_c) + 1}$$

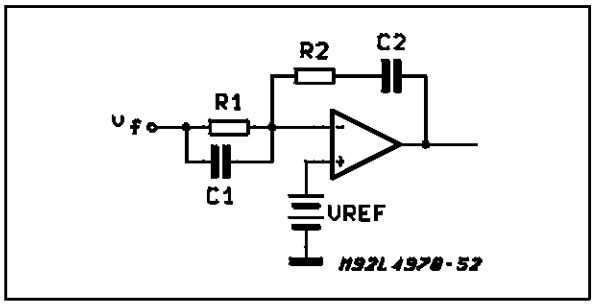
In the hypotesis that Rc<Ro and Cc>Co, the Bode diagram of the compensated amplifier is reported (see fig.14).

Figure 14: Bode plot showing gain and phase of compensated error amplifier.



The compensation network introduces a low frequency pole and a zero that usually is put at the frequency of the resonant pole of the output LC filter. The second high frequency pole is usually at a frequency of no interest. If needed , more sophisticated compensation circuits can be used by feedback with the opamp. An example is shown in fig.15.

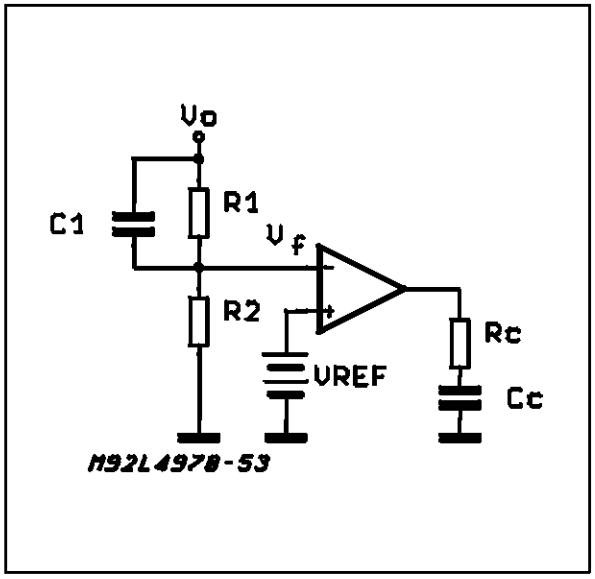
Figure 15: One pole, two zero compensation network.



Such a configuration introduces a low frequency pole and two zeros Z1 = 1/2ΠR1C1 and Z2 = 1/2ΠR2C2. Note that due to the high output impedance it is present also a second pole p2 = gm/2ΠC1. Usually it is better to use the highest possible value for R1, to have a low value for C1 in such a way to put p2 at the highest frequency. Limitations to R1 value are put by offset voltage due to opamp. input bias currents.

If a resistive divider is used at the output of the power supply, for voltages higher than 5.1V, it is possible to introduce a second zero with the network of fig.16.

Figure 16: Compensation network for output voltages higher than 51V.



Such a configuration introduce 2 zeros at:

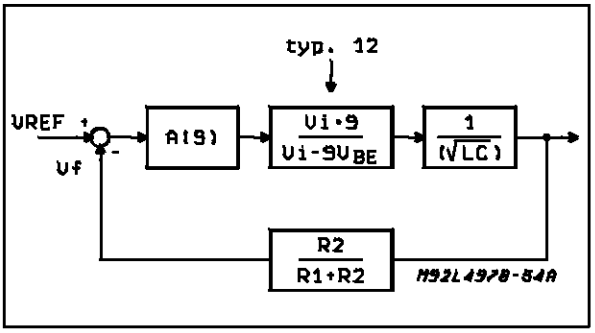
$$Z_1 = \frac{1}{2\Pi\ R_c\ C_c}\ ;\quad Z_2 = \frac{1}{2\Pi\ R_1\ C_1}$$

and 2 poles at:

$$P_1 = \frac{1}{2\Pi\ R_o C_c}\ ;\ P_2 = \frac{1}{2\Pi\ R_x\ C_1}\ ;\ R_X = \frac{R_1\ R_2}{R_1 + R_2}$$

APPLICATION EXAMPLE

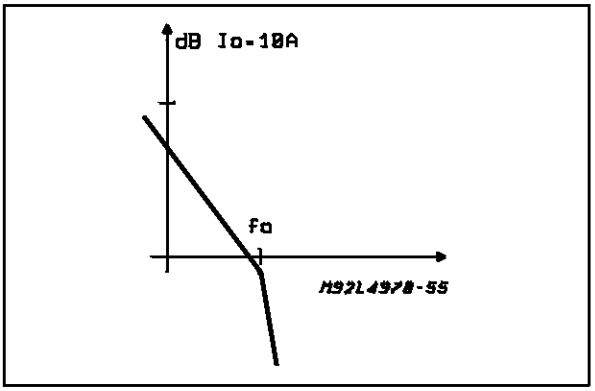
Figure 17: Block diagram used in stability calculation.



Consider the block diagram of fig.17, representing the internal control loop section, with the application values:
Fswitch = 200KHz, L = 100µH, C =1000µF, Po=50W, Vo =5.1V, Io =10A and Fo = 500Hz.

G_{loop} = PWM · Filter

Figure 18: Frequency behavior of the circuit of fig 17.



The system requires that DC gain is maximum to achieve good accuracy and line rejection. Beyond this a bandwidth of some KHz is usually required for a good load transient response. The error amplifier transfer function must guarantee the above constraints. A compensation network that could be used is shown in fig.19.

$$A(s) = \frac{(1 + sR_1 C_1)\ (1 + sR_2 C_2)}{sR_1 C_1\ (1 + s\frac{C_1}{G_M})}$$

Figure 19: Compensation network.

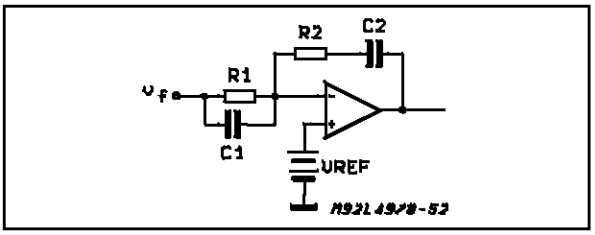
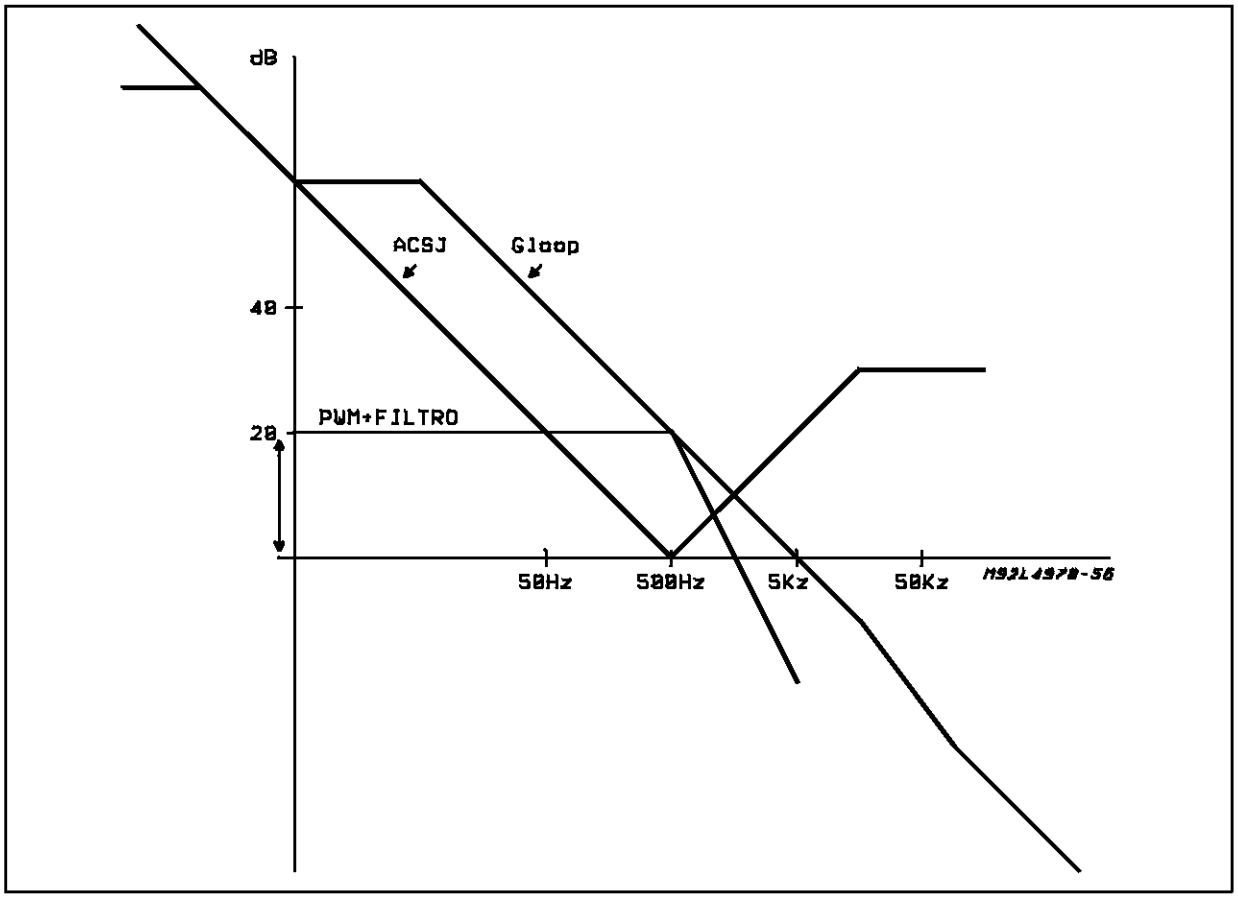


Figure 20: Bode plot of the regulation loop with the compensation network of fig. 19.



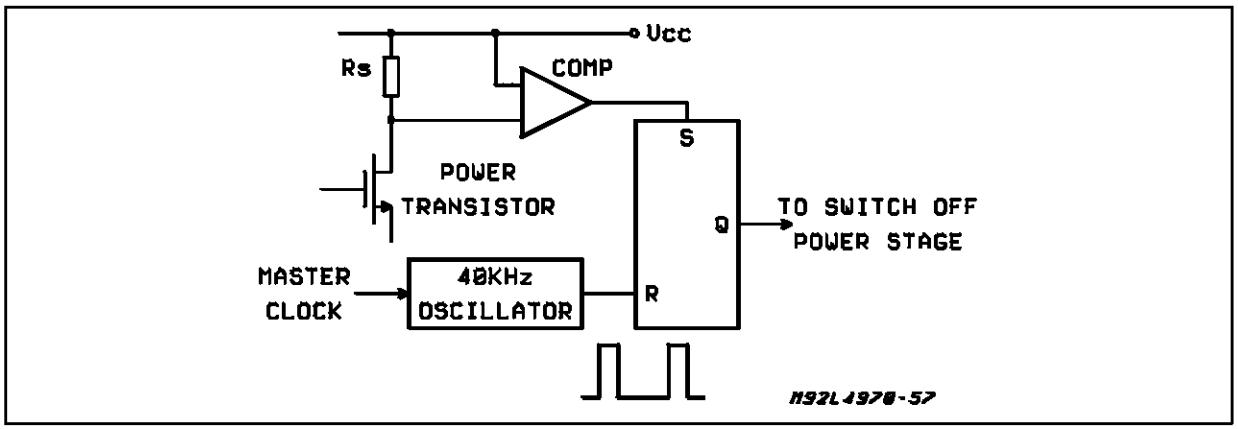
The criterium is to define Z1, Z2 close to the resonant pole of the output LC filter. The $Gm/2\Pi C_1$ pole must be placed at a frequency at which open loop gain is below 0 dB axis (Fig. 20).

CURRENT LIMITATION

Current limitation is implemented intrnally to the chip and doesn't need any external component. The output current is sensed by an internal resistor in series with the drain of the power transistor. On chip trimming guarantees $\pm$10% accuracy on the value of peak current limitation.

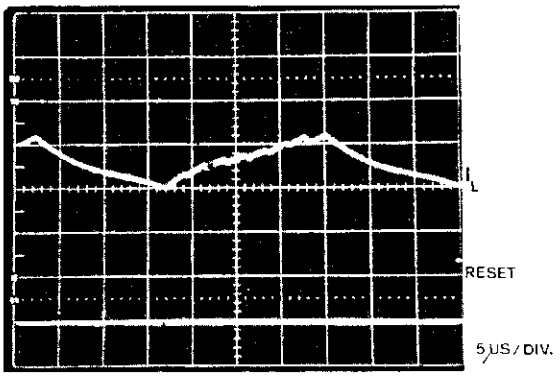
Current limit protection works pulse by pulse with lowering of tnhe switching frequency. Fig.21 shows circuital implementation of current protection.

Figure 21: Current protection circuit.



When the comparator senses an overcurrent, the flip-flop is set and an internal inhibit signal is generated. The flip-flop remains set until next reset clock pulse coming from the internal 40 KHz oscillator. After the reset pulse the regulation loop takes the control of the system and the output current begins to increase to the load value at the switching frequency of the master clock. If the overload condition is still present the protection cycle repeats. This mixed, pulse by pulse, lowering frequency current protection method, assures a constant current output when the system is in overload or short circuit and allows to implement a reliable current limitation even at high switching frequency (500 KHz) reducing the problems of signal delay through the protection stage. Fig.22 shows behavior of the inductance current when the system is in overload.

Figure 22: Overload inductance current.



The internal 40 KHz oscillator is synchronized with the master clock. When the system works with the master clock at a lower frequency of the internal clock, than the internal clock tracks the master frequency. This assures that the frequency does not increas during overload.

POWER FAIL-RESET CIRCUIT

The L4970A include a voltage sensing circuit that may be used to generate a power on power off reset signal for a microprocessor system. The circuit senses the input supply voltage and the output generated voltage and will generate the required reset signal only when both the sensed voltages have reached the required value for correct system operation. The Reset signal is generated after a delay time programmable by an external capacitor on the delay pin. Fig. 23 shows the circuit implementation of Reset circuit. The supply voltage is sensed on an external pin, for programmability of the threshold, by a first comparator. The second comparator has the reference threshold set at slightly less the ref. voltage for the regulation circuit and the other input connected internally at the feedback point on the error amplifier. This allows to sense the output regulated voltage. When both the supply voltage and the regulated voltage are in the correct range, transistor Q1 turns off and allows the current generator to charge the delay capacitor. When the capacitor voltage reaches 5V the output Reset signal is generated. A latch assures that if a spike is present on the sensed voltage the delay capacitor discharges completely before initialization of a new Reset cycle. The output gate assures immediate take of reset signal with-

Figure 23: Power fail and reset circuit.

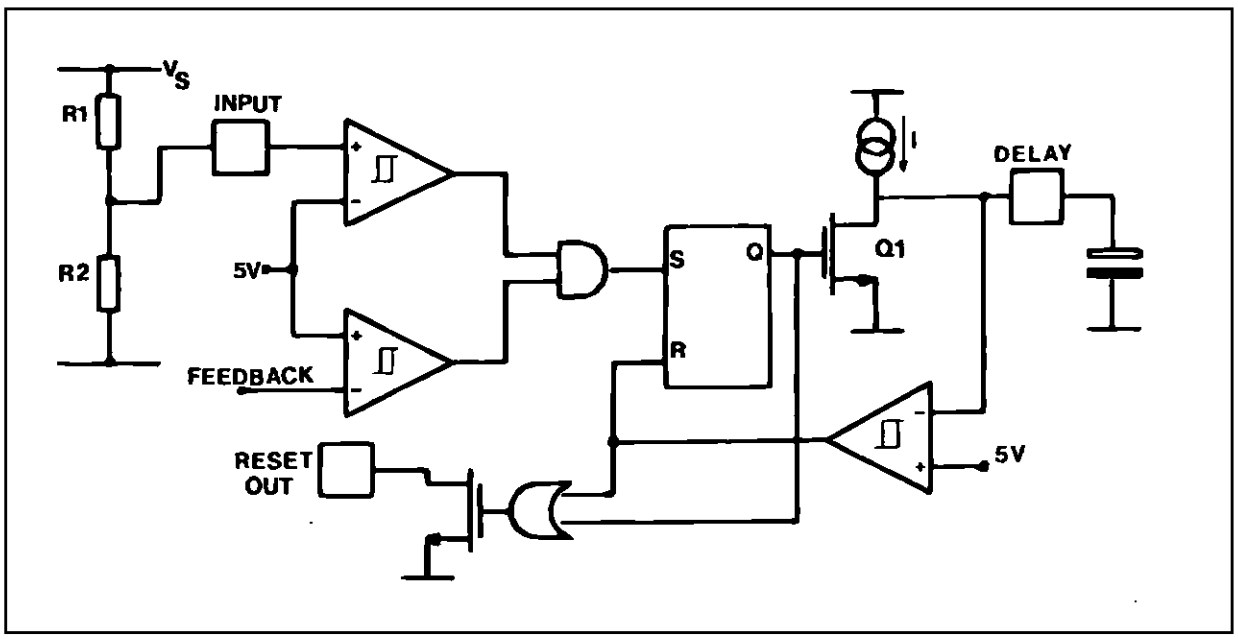
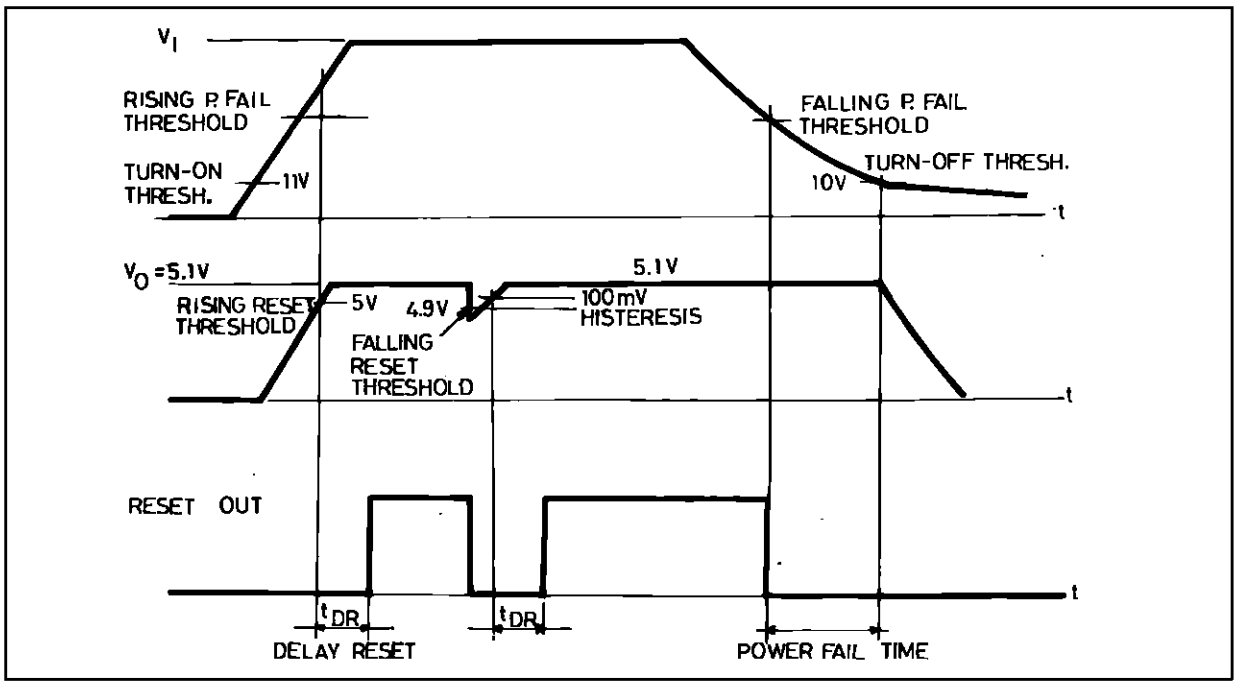


Figure 24: Reset and power fail waveforms.



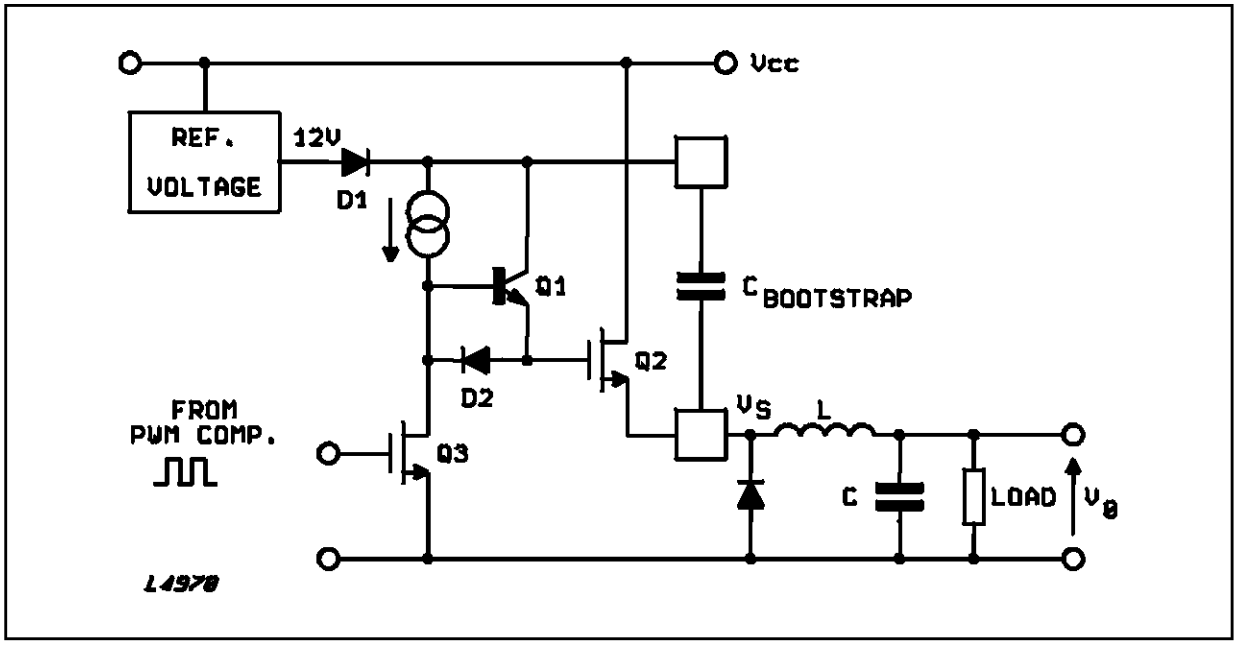
out waiting for complete discharge of delay capacitor. Reset output is an open collector transistor capable of sinking 20mA at 200mV voltage.Fig. 24 shows reset waveforms.

THE POWER STAGE

A simplified schematic of the output stage along with the external filter components is shown in fig.25.

Figure 25: Power stage circuit.

Power stage and associated driving circuits are among the most critical components to achieve good performances at high switching frequency. An external bootstrap capacitance, charged via diode D1 at 12V, is needed to provide the correct gate drive to the power DMOS N-channel transistor. The driving circuit is able to deliver a current peak of 0.5A, during turn on and turn off phases, to the gate of power DMOS transistor. The circuit-described shows commutation times of 50ns.



The five devices of L497X family differentiate each other only for the level of current protection, while the control part is the same and power device area is the same to guarantee low power dissipation also for low current versions in DIP package.

Table 1 and fig.26 shows electrical characteristics of the power DMOS implemented in the chip.

THERMAL PROTECTION

The thermal protection function operates when the junction temperature reaches 150°C; it acts directly on the power soft start capacitor, discharging it. The thermal protection is provided with hysteresis and therefore, after an intervention has occurred, it is necessary to wait for the junction temperature to decrease of about 30 degree C below the intervention threshold.

Figure 26: Gate-charge curve for the power DMOS.

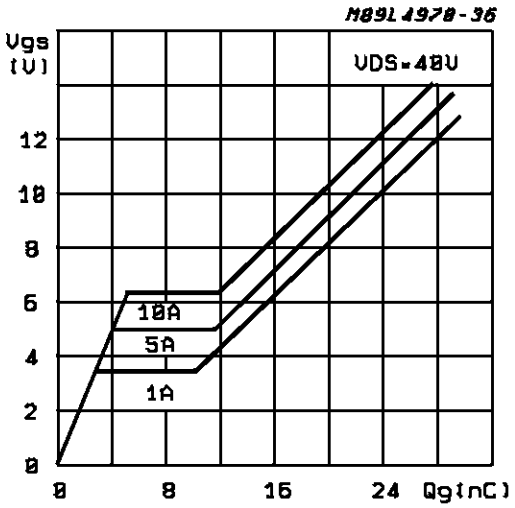


Table 1.

B_{VDSS} > 60V	at I_D = 1mA		V_{GS} = 0V
$R_{DS(ON)}$ = 100mΩ	at I_D = 10A	T_j = 25°C	V_{GS} = 10V
$R_{DS(ON)}$ = 150mΩ	at I_D = 10A	T_j = 150°C	V_{GS} = 10V
V_{TH} = 3V	at I_D = 1mA		