LT1074/LT1076 Design Manual

Carl Nelson

INTRODUCTION

The use of switching regulators increased dramatically in the 1980's and this trend remains strong going into the 90s. The reasons for this are simple; heat and efficiency. Today's systems are shrinking continuously, while simultaneously offering greater electronic "horsepower." This combination would result in unacceptably high internal temperatures if low efficiency linear supplies were used. Heat sinks do not solve the problem in general because most systems are closed, with low thermal transfer from "inside" to "outside."

Battery powered systems need high efficiency supplies for long battery life. Topological considerations also require switching technology. For instance, a battery cannot generate an output higher than itself with linear supplies. The availability of low cost rechargeable batteries has created a spectacular rise in the number of battery powered systems, and consequently a matching rise in the use of switching regulators.

The LT1074 and LT1076 switching regulators are designed specifically for ease of use. They are close to the ultimate "three terminal box" concept which simply requires an input, output and ground connection to deliver power to the load. Unfortunately, switching regulators are not horseshoes, and "close" still leaves room for egregious errors in the final execution. This Application Note is intended to eliminate the most common errors that customers make with switching regulators as well as offering some insight into the inner workings of switching designs. There is also an entirely new treatment of inductor design based on the mathematical models of core loss and peak current. This allows the customer to quickly see the allowable limits for inductor value and make an intelligent decision based on the need for cost, size, etc. The procedure differs greatly from previous design techniques and many experienced designers at first think it can't work. They quickly become silent after standard laborious trial-and-error techniques yield identical results.

There is an old adage in woodworking — "Measure twice, cut once." This advice holds for switching regulators, also. Read AN44 through quickly to familiarize yourself with the contents. Then reread the pertinent sections carefully to avoid "cutting" the design two, three, or four times. Some switching regulator errors, such as excessive ripple current in capacitors, are time bombs best fixed *before* they are expensive field failures.

Since this paper was originally written, Linear Technology has produced a CAD program for switching regulators called SwitcherCAD. This program uses the ideas presented in this application note, but adds an extra level of accuracy by factoring in more second order effects. It also takes the drudgery out of the iterative design procedure, allowing rapid "what if" exploration. I highly recommend using SwitcherCAD after absorbing the basic concepts presented here. It cuts design time considerably, presents detailed information on operating conditions, and has many safeguards to prevent unreliable designs. One caution, however; SwitcherCAD has an initial run sequence, called Novice Mode, which generates a very conservative design from database components. The results of this initial design may not correlate with AN44 procedures because of assumptions used in SwitcherCAD and because of the limited number of components in the database. Changing to Expert Mode allows all components to be changed at will.

SwitcherCAD does not calculate components for loop stability. Linear Technology will be creating several separate programs for this purpose during 1993. Contact our Application department for details.

TABLE OF CONTENTS

ABSOLUTE MAXIMUM RATINGS

Input Voltage
- LT1074/ LT1076 ..... 45V
- LT1074HV/76HV 64V

Switch Voltage with Respect to Input Voltage
- LT1074/ 76 ..... 64V
- LT1074HV/76HV 75V

Switch Voltage with Respect to Ground Pin (V_{SW} **Negative**)
- LT1074/76 (Note 6) 35V
- LT1074HV/76HV (Note 6) 45V

Feedback Pin Voltage ..... –2V, +10V

Shutdown Pin Voltage (Not to Exceed V_{IN}) 40V

Status Pin Voltage 30V
(Current Must Be Limited to 5mA When Status Pin Switches “On”)

I_{LIM} Pin Voltage (Forced) 5.5V

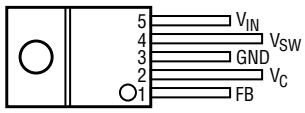
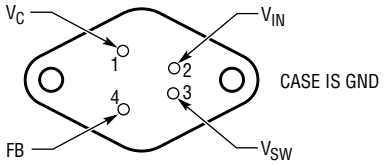
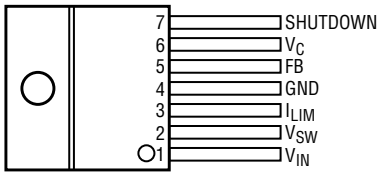
Maximum Operating Ambient Temperature Range
- LT1074C/76C, LT1074HVC/76HVC ..... 0°C to 70°C
- LT1074M/76M, LT1074HVM/76HVM –55°C to 125°C

Maximum Operating Junction Temperature Range
- LT1074C/76C, LT1074HVC/76HVC ..... 0°C to 125°C
- LT1074M/76M, LT1074HVM/76HVM –55°C to 150°C

Maximum Storage Temperature ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
FRONT VIEW  T PACKAGE 5-LEAD TO-220 LEADS ARE FORMED STANDARD FOR STRAIGHT LEADS, ORDER FLOW 06	LT1074CT LT1074HVCT LT1076CT LT1076HVCT
BOTTOM VIEW  K PACKAGE 4-LEAD TO-3 METAL CAN	LT1074MK LT1074HVMK LT1074CK LT1074HVCK LT1076MK LT1076HVMK LT1076CK LT1076HVCK
FRONT VIEW  Y PACKAGE 7-LEAD TO-220	LT1074CY

ELECTRICAL CHARACTERISTICS

T_j = 25°C, V_{IN} = 25V, unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Switch “On” Voltage (Note 1)	LT1074	I_{SW} = 1A, $T_j \geq 0°C$				1.85	V
		I_{SW} = 1A, $T_j < 0°C$				2.1	V
		I_{SW} = 5A, $T_j \geq 0°C$				2.3	V
		I_{SW} = 5A, $T_j < 0°C$				2.5	V
	LT1076	I_{SW} = 0.5A	●			1.2	V
		I_{SW} = 2A	●			1.7	V
Switch “Off” Leakage	LT1074	$V_{IN} \leq 25V$, V_{SW} = 0			5	300	µA
		$V_{IN} = V_{MAX}$, V_{SW} = 0 (Note 7)			10	500	µA
	LT1076	V_{IN} = 25V, V_{SW} = 0				150	µA
		$V_{IN} = V_{MAX}$, V_{SW} = 0 (Note 7)				250	µA
Supply Current (Note 2)	V_{FB} = 2.5V, $V_{IN} \leq 40V$		●		8.5	11	mA
	40V < V_{IN} < 60V		●		9	12	mA
	V_{SHUT} = 0.1V (Device Shutdown) (Note 8)		●		140	300	µA

ELECTRICAL CHARACTERISTICS $T_j = 25°C$, $V_{IN} = 25V$, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Supply Voltage	Normal Mode	●		7.3	8	V
	Startup Mode (Note 3)	●		3.5	4.8	V
Switch Current Limit (Note 4)	LT1074 I_{LIM} Open	●	5.5	6.5	8.5	A
	R_{LIM} = 10k (Note 5)			4.5		A
	R_{LIM} = 7k (Note 5)			3		A
	LT1076 I_{LIM} Open	●	2	2.6	3.2	A
	R_{LIM} = 10k (Note 5)			1.8		A
	R_{LIM} = 7k (Note 5)			1.2		A
Maximum Duty Cycle		●	85	90		%
Switching Frequency			90	100	110	kHz
	$T_j \leq 125°C$	●	85		120	kHz
	$T_j > 125°C$	●	85		125	kHz
	V_{FB} = 0V through 2kΩ (Note 4)			20		kHz
Switching Frequency Line Regulation	$8V \leq V_{IN} \leq V_{MAX}$ (Note 7)	●		0.03	0.1	%/V
Error Amplifier Voltage Gain (Note 6)	$1V \leq V_C \leq 4V$			2000		V/V
Error Amplifier Transconductance			3700	5000	8000	μmho
Error Amplifier Source and Sink Current	Source (V_{FB} = 2V)		100	140	225	μA
	Sink (V_{FB} = 2.5V)		0.7	1	1.6	mA
Feedback Pin Bias Current	$V_{FB} = V_{REF}$	●		0.5	2	μA
Reference Voltage	V_C = 2V	●	2.155	2.21	2.265	V
Reference Voltage Tolerance	V_{REF} (Nominal) = 2.21V			±0.5	±1.5	%
	All Conditions of Input Voltage, Output Voltage, Temperature and Load Current	●		±1	±2.5	%
Reference Voltage Line Regulation	$8V \leq V_{IN} \leq V_{MAX}$ (Note 7)	●		0.005	0.02	%/V
V_C Voltage at 0% Duty Cycle				1.5		V
	Over Temperature	●		– 4		mV/°C
Multiplier Reference Voltage				24		V
Shutdown Pin Current	V_{SH} = 5V	●	5	10	20	μA
	$V_{SH} \leq V_{THRESHOLD}$ (≅2.5V)	●			50	μA
Shutdown Thresholds	Switch Duty Cycle = 0	●	2.2	2.45	2.7	V
	Fully Shut Down	●	0.1	0.3	0.5	V
Status Window	As a Percent of Feedback Voltage		4	±5	6	%
Status High Level	I_{STATUS} = 10μA Sourcing	●	3.5	4.5	5.0	V
Status Low Level	I_{STATUS} = 1.6mA Sinking	●		0.25	0.4	V
Status Delay Time				9		μs
Status Minimum Width				30		μs
Thermal Resistance Junction to Case	LT1074				2.5	°C/W
	LT1076				4.0	°C/W

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: To calculate maximum switch "on" voltage at currents between low and high conditions, a linear interpolation may be used.

Note 2: A feedback pin voltage (V_{FB}) of 2.5V forces the V_C pin to its low clamp level and the switch duty cycle to zero. This approximates the zero load condition where duty cycle approaches zero.

Note 3: Total voltage from V_{IN} pin to ground pin must be ≥ 8V after startup for proper regulation.

Note 4: Switch frequency is internally scaled down when the feedback pin voltage is less than 1.3V to avoid extremely short switch on times. During testing, V_{FB} is adjusted to give a minimum switch on time of 1μs.

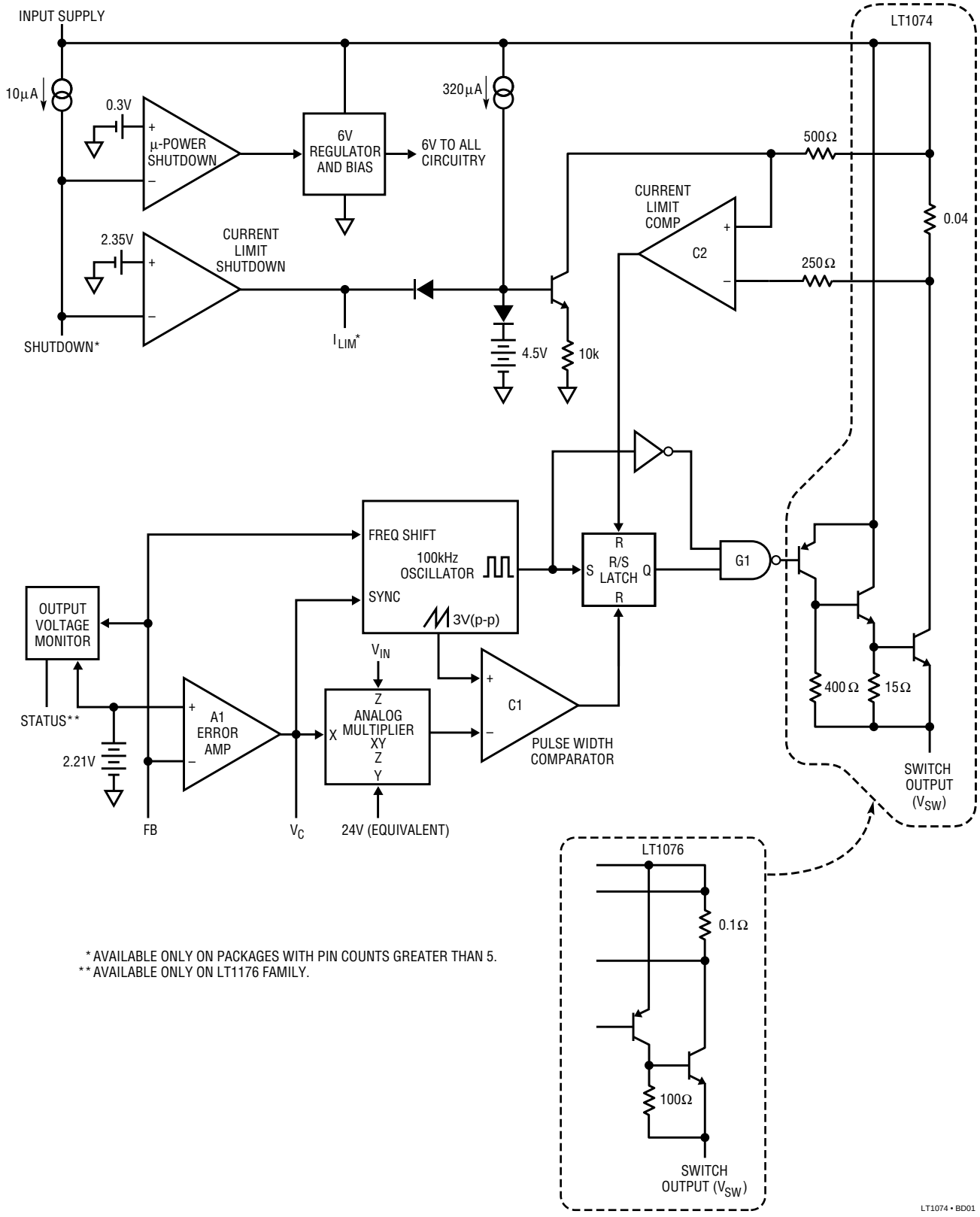
Note 5: $I_{LIM} \approx \frac{R_{LIM} - 1k}{2k}$ (LT1074), $I_{LIM} \approx \frac{R_{LIM} - 1k}{5.5k}$ (LT1076).

Note 6: Switch to input voltage limitation must also be observed.

Note 7: V_{MAX} = 40V for the LT1074/76 and 60V for the LT1074HV/76HV.

Note 8: Does not include switch leakage.

BLOCK DIAGRAM



* AVAILABLE ONLY ON PACKAGES WITH PIN COUNTS GREATER THAN 5.
** AVAILABLE ONLY ON LT1176 FAMILY.

BLOCK DIAGRAM DESCRIPTION

A switch cycle in the LT1074 is initiated by the oscillator setting the R/S latch. The pulse that sets the latch also locks out the switch via gate G1. The effective width of this pulse is approximately 700ns, which sets the maximum switch duty cycle to approximately 93% at 100kHz switching frequency. The switch is turned off by comparator C1, which resets the latch. C1 has a sawtooth waveform as one input and the output of an analog multiplier as the other input. The multiplier output is the product of an internal reference voltage, and the output of the error amplifier, A1, divided by the regulator input voltage. In standard buck regulators, this means that the output voltage of A1 required to keep a constant regulated output is independent of regulator input voltage. This greatly improves line transient response, and makes loop gain independent of input voltage. The error amplifier is a transconductance type with a G_M at null of approximately 5000μmho. Slew current going positive is 140μA, while negative slew current is about 1.1mA. This asymmetry helps prevent overshoot on startup. Overall loop frequency compensation is accomplished with a series RC network from V_C to ground.

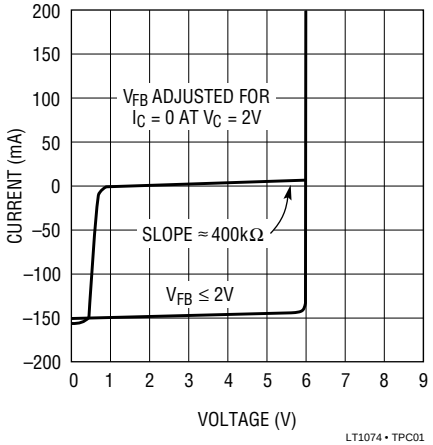
Switch current is continuously monitored by C2, which resets the R/S latch to turn the switch off if an overcurrent condition occurs. The time required for detection and switch turn-off is approximately 600ns. So minimum switch "on" time in current limit is 600ns. Under dead shorted output conditions, switch duty cycle may have to be as low as 2% to maintain control of output current. This would require switch on time of 200ns at 100kHz switching frequency, so frequency is reduced at very low output voltages by feeding the FB signal into the oscillator and creating a linear frequency downshift when the FB signal drops below 1.3V. Current trip level is set by the voltage on the I_{LIM} pin which is driven by an internal 320μA current source. When this pin is left open, it self-clamps at about 4.5V and sets current limit at 6.5A for the LT1074 and 2.6A for the LT1076. In the 7-pin package an external resistor can be connected from the I_{LIM} pin to ground to set a lower current limit. A capacitor in parallel with this resistor will soft start the current limit. A slight offset in C2 guarantees that when the I_{LIM} pin is pulled to within 200mV of ground, C2 output will stay high and force switch duty cycle to zero.

The "Shutdown" pin is used to force switch duty cycle to zero by pulling the I_{LIM} pin low, or to completely shut down the regulator. Threshold for the former is approximately 2.35V, and for complete shutdown, approximately 0.3V. Total supply current in shutdown is about 150μA. A 10μA pull-up current forces the shutdown pin high when left open. A capacitor can be used to generate delayed startup. A resistor divider will program "undervoltage lockout" if the divider voltage is set at 2.35V when the input is at the desired trip point.

The switch used in the LT1074 is a Darlington NPN (single NPN for LT1076) driven by a saturated PNP. Special patented circuitry is used to drive the PNP on and off very quickly even from the saturation state. This particular switch arrangement has no "isolation tubs" connected to the switch output, which can therefore swing to 40V below ground.

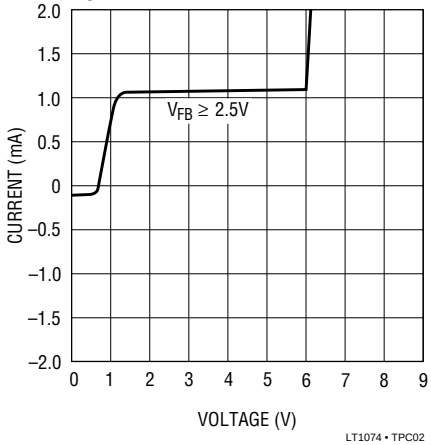
TYPICAL PERFORMANCE CHARACTERISTICS

V_C Pin Characteristics



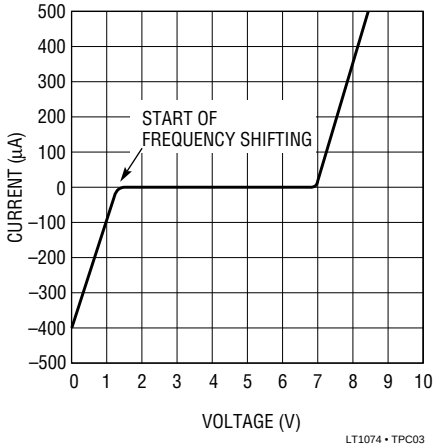
LT1074 • TPC01

V_C Pin Characteristics



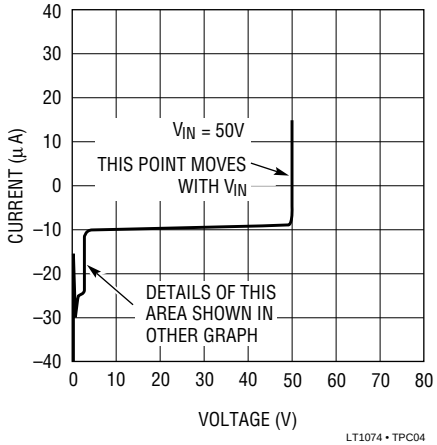
LT1074 • TPC02

Feedback Pin Characteristics



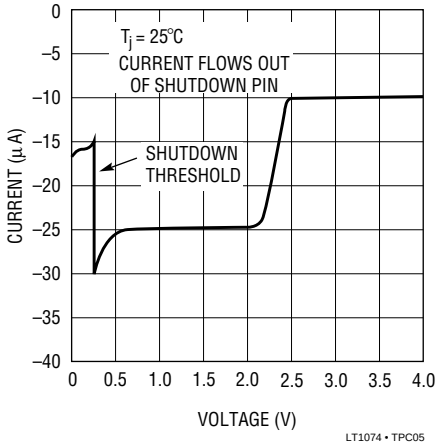
LT1074 • TPC03

Shutdown Pin Characteristics



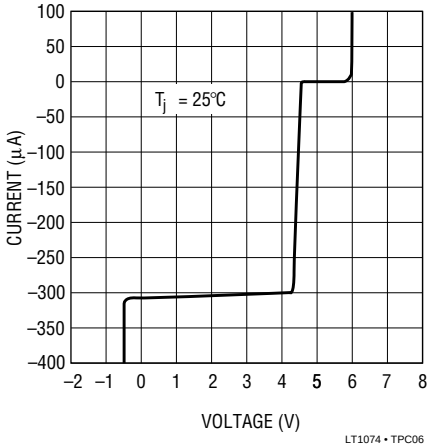
LT1074 • TPC04

Shutdown Pin Characteristics



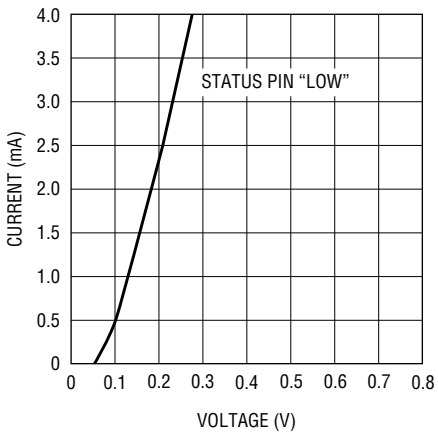
LT1074 • TPC05

I_{LIM} Pin Characteristics



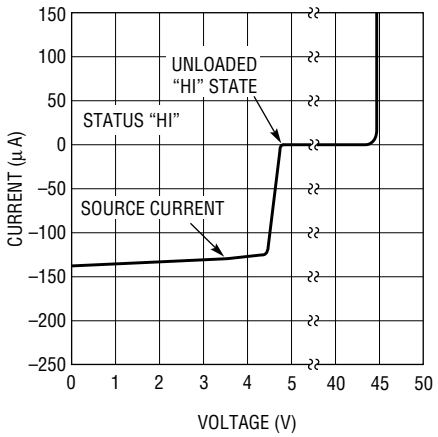
LT1074 • TPC06

Status Pin Characteristics



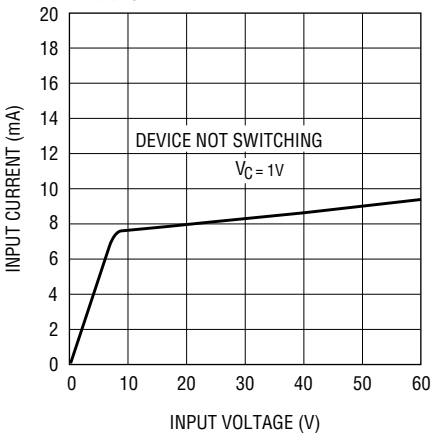
LT1074 • TPC08

Status Pin Characteristics



LT1074 • TPC09

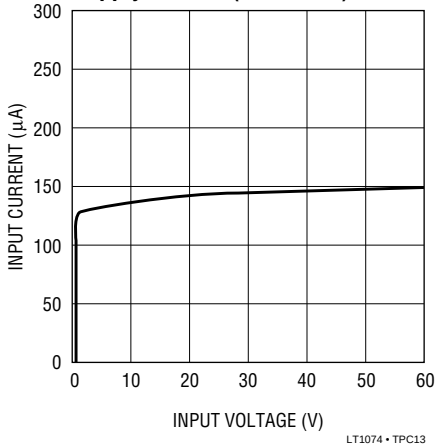
Supply Current



LT1074 • TPC11

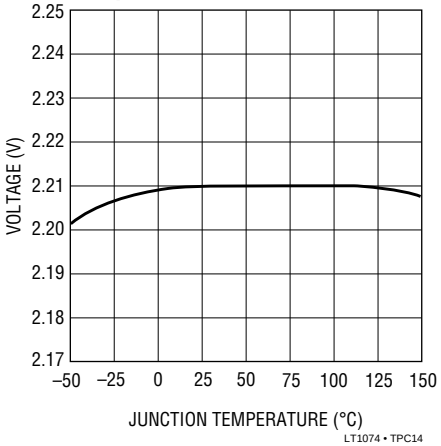
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current (Shutdown)



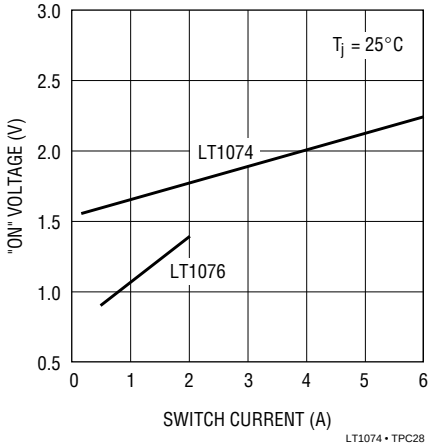
LT1074 • TPC13

Reference Voltage vs Temperature



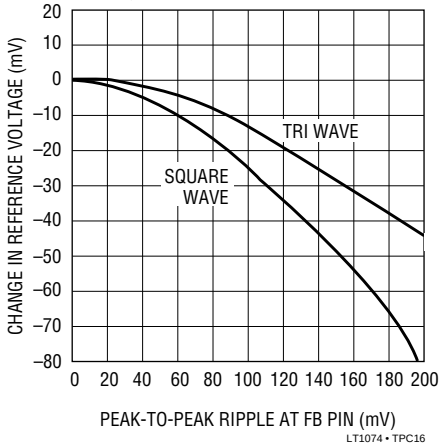
LT1074 • TPC14

Switch "On" Voltage



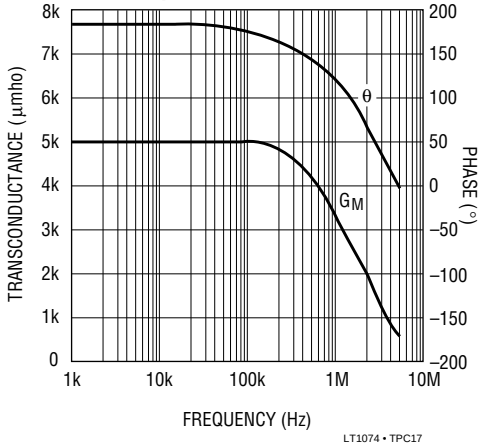
LT1074 • TPC28

Reference Shift with Ripple Voltage



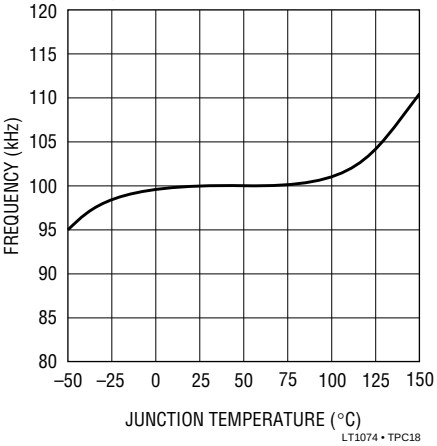
LT1074 • TPC16

Error Amplifier Phase and G_M



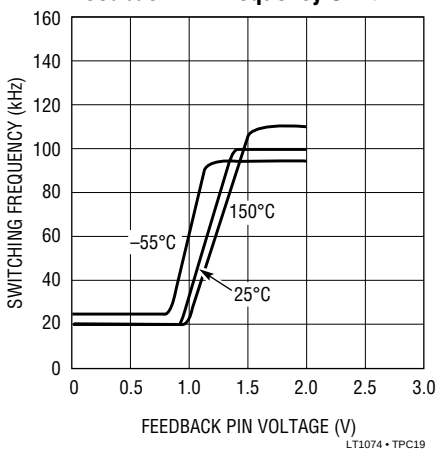
LT1074 • TPC17

Switching Frequency vs Temperature



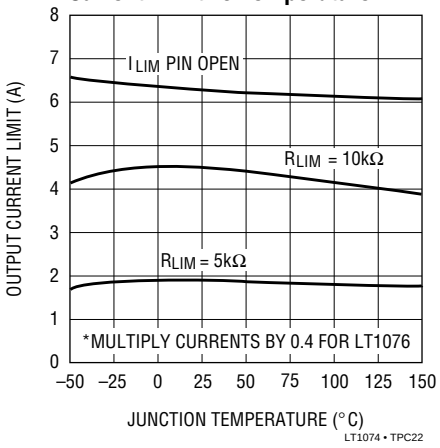
LT1074 • TPC18

Feedback Pin Frequency Shift



LT1074 • TPC19

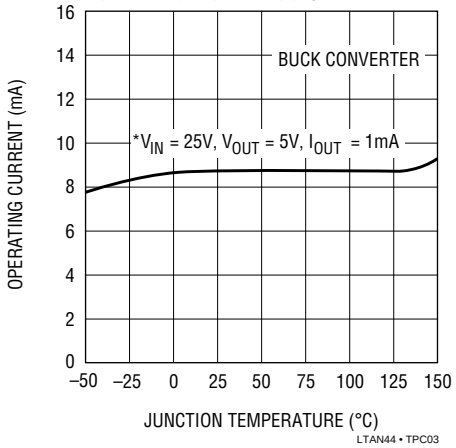
Current Limit vs Temperature*



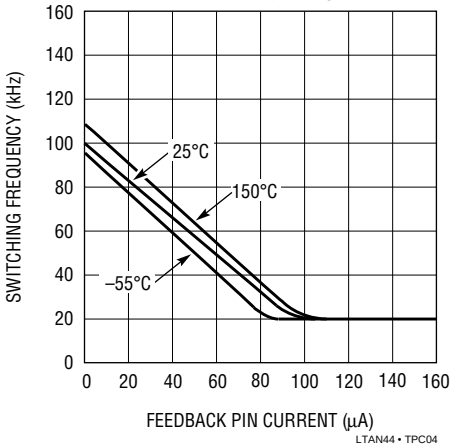
LT1074 • TPC22

TYPICAL PERFORMANCE CHARACTERISTICS

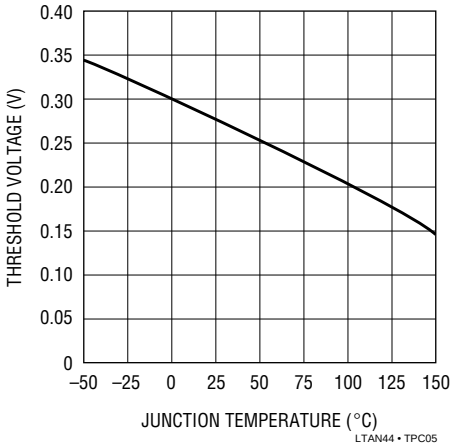
Operating Input Supply Current*



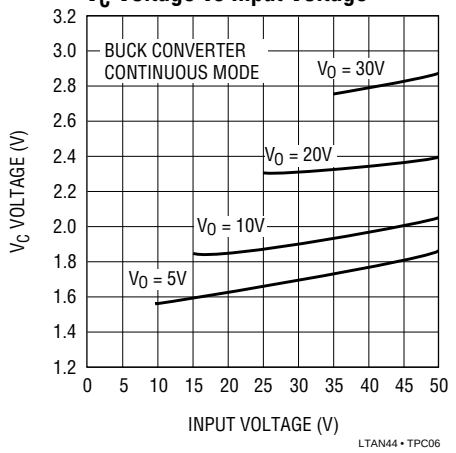
Feedback Pin Frequency Shift



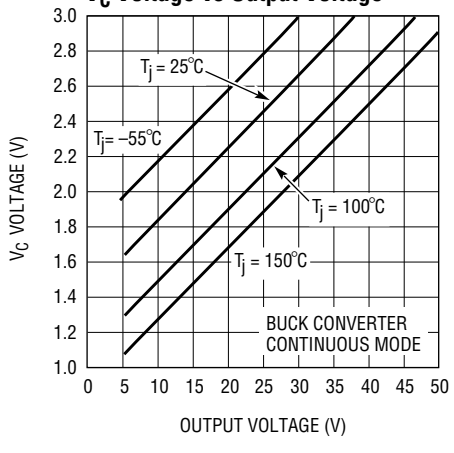
Shutdown Threshold



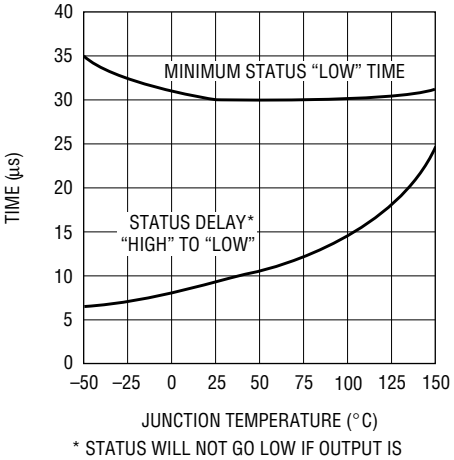
V_C Voltage vs Input Voltage



V_C Voltage vs Output Voltage



Status Delay and Minimum Timeout



PIN DESCRIPTIONS

V_{IN} PIN

The V_{IN} pin is both the supply voltage for internal control circuitry and one end of the high current switch. It is important, *especially at low input voltages*, that this pin be bypassed with a low ESR, and low inductance capacitor to prevent transient steps or spikes from causing erratic operation. At full switch current of 5A, the switching transients at the regulator input can get very large as shown in Figure 1. Place the input capacitor very close to the regulator and connect it with wide traces to avoid extra inductance. Use radial lead capacitors.

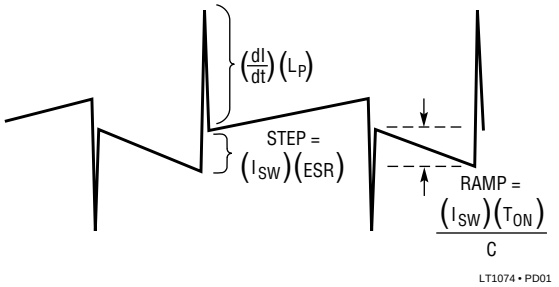


Figure 1. Input Capacitor Ripple

L_P = Total inductance in input bypass connections and capacitor.

"Spike" height $\left(\frac{dI}{dt} \bullet L_P\right)$ is approximately 2V *per inch* of lead length.

Step = 0.25V for ESR = 0.05Ω and I_{SW} = 5A is 0.25V.

Ramp = 125mV for C = 200µF, T_{ON} = 5µs, and I_{SW} = 5A is 125mV.

Input current on the V_{IN} Pin in shutdown mode is the sum of actual supply current (≈140µA, with a maximum of 300µA) and switch leakage current. Consult factory for special testing if shutdown mode input current is critical.

GROUND PIN

It might seem unusual to describe a ground pin, but in the case of regulators, the ground pin must be connected properly to ensure good load regulation. The internal reference voltage is referenced to the ground pin; so any error in ground pin voltage will be multiplied at the output;

$$\Delta V_{OUT} = \frac{(\Delta V_{GND})(V_{OUT})}{2.21}$$

To ensure good load regulation, the ground pin must be connected directly to the proper output node, so that no high currents flow in this path. The output divider resistor should also be connected to this low current connection line as shown in Figure 2.

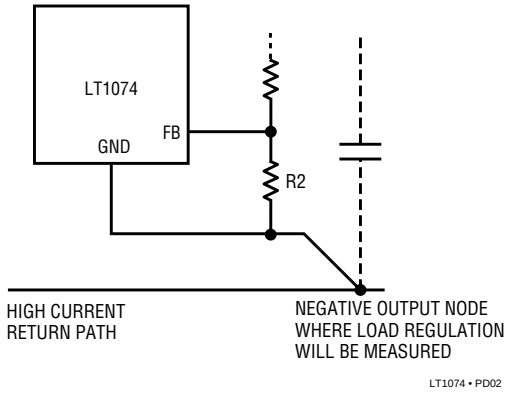


Figure 2. Proper Ground Pin Connection

FEEDBACK PIN

The feedback pin is the inverting input of an error amplifier which controls the regulator output by adjusting duty cycle. The non-inverting input is internally connected to a trimmed 2.21V reference. Input bias current is typically 0.5µA when the error amplifier is balanced (I_{OUT} = 0). The error amplifier has asymmetrical G_M for large input signals to reduce startup overshoot. This makes the amplifier more sensitive to large ripple voltages at the feedback pin. 100mVp-p ripple at the feedback pin will create a 14mV offset in the amplifier, equivalent to a 0.7% output voltage shift. To avoid output errors, output ripple (p-p) should be less than 4% of DC output voltage at the point where the output divider is connected.

See the "Error Amplifier" section for more details.

Frequency Shifting at the Feedback Pin

The error amplifier feedback pin (FB) is used to downshift the oscillator frequency when the regulator output voltage is low. This is done to guarantee that output short circuit

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current is well controlled even when switch duty cycle must be extremely low. Theoretical switch "on" time for a buck converter in continuous mode is;

$$t_{ON} = \frac{V_{OUT} + V_D}{V_{IN} \bullet f}$$

V_D = Catch diode forward voltage (≈ 0.5V)
f = Switching frequency

At f = 100kHz, t_{ON} must drop to 0.2μs when V_{IN} = 25V and the output is shorted (V_{OUT} = 0V). In current limit, the LT1074 can reduce t_{ON} to a minimum value of ≈ 0.6μs, much too long to control current correctly for V_{OUT} = 0. To correct this problem, switching frequency is lowered from 100kHz to 20kHz as the FB pin drops from 1.3V to 0.5V. This is accomplished by the circuitry shown in Figure 3.

Q1 is off when the output is regulating (V_{FB} = 2.21V). As the output is pulled down by an overload, V_{FB} will eventually reach 1.3V, turning on Q1. As the output continues to drop, Q1 current increases proportionately and lowers the frequency of the oscillator. Frequency shifting starts when the output is ≈ 60% of normal value, and is down to its minimum value of ≅ 20kHz when the output is ≅ 20% of normal value. The rate at which frequency is shifted is determined by both the internal 3k resistor R3 and the external divider resistors. For this reason, R2 should not be increased to more than 4kΩ, if the LT1074 will be subjected to the simultaneous conditions of high input voltage and output short circuit.

SHUTDOWN PIN

The shutdown pin is used for undervoltage lockout, micropower shutdown, soft start, delayed start, or as a general purpose on/off control of the regulator output. It controls switching action by pulling the I_{LIM} pin low, which forces the switch to a continuous "off" state. Full micropower shutdown is initiated when the shutdown pin drops below 0.3V.

The V/I characteristics of the shutdown pin are shown in Figure 4. For voltages between 2.5V and ≈V_{IN}, a current of 10μA flows *out* of the shutdown pin. This current increases to ≈25μA as the shutdown pin moves through the 2.35V threshold. The current increases further to ≈ 30μA at the 0.3V threshold, then drops to ≈15μA as the shutdown voltage falls below 0.3V. The 10μA current source is included to pull the shutdown pin to its high or default state when left open. It also provides a convenient pullup for delayed start applications with a capacitor on the shutdown pin.

When activated, the typical collector current of Q1 in Figure 5, is ≈ 2mA. A soft start capacitor on the I_{LIM} pin will delay regulator shutdown in response to C1, by ≈(5V)(C_{LIM})/2mA. Soft start after full micropower shutdown is ensured by coupling C2 to Q1.

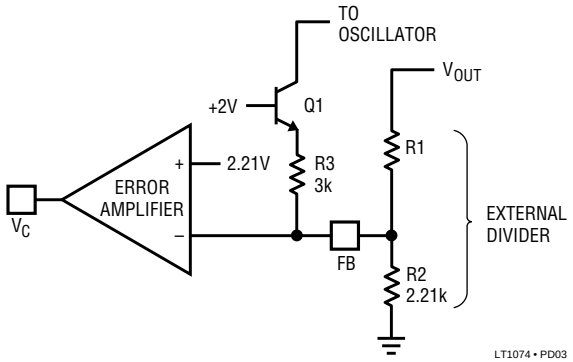

Figure 3. Frequency Shifting

PIN DESCRIPTIONS

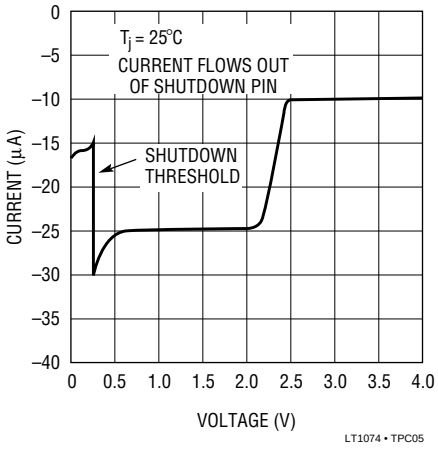

Figure 4. Shutdown Pin Characteristics

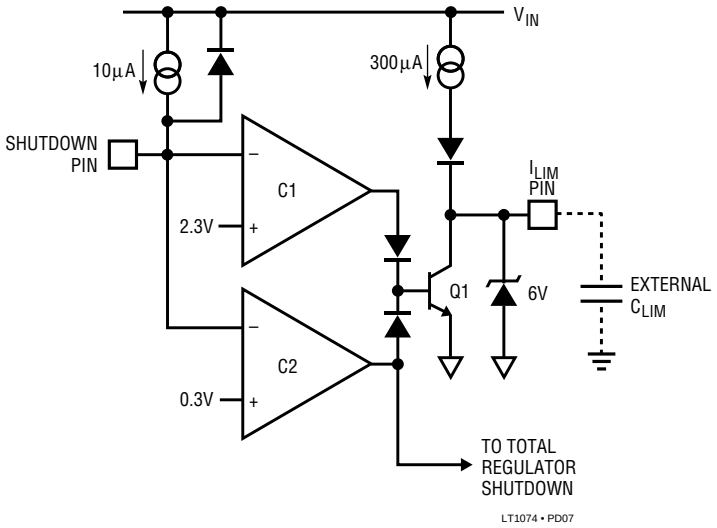

Figure 5. Shutdown Circuitry

Undervoltage Lockout

Undervoltage lockout point is set by R1 and R2 in Figure 6. To avoid errors due to the 10µA shutdown pin current, R2 is usually set at 5k, and R1 is found from:

$$R1 = R2\,\frac{(V_{TP} - V_{SH})}{V_{SH}}$$

V_{TP} = Desired undervoltage lockout voltage.
V_{SH} = Threshold for lockout on the shutdown pin = 2.45V.

If quiescent supply current is critical, R2 may be increased up to 15kΩ, but the denominator in the formula for R2 should replace V_{SH} with V_{SH} – (10µA)(R2).

Hysteresis in undervoltage lockout may be accomplished by connecting a resistor (R3) from the I_{LIM} pin to the shutdown pin as shown in Figure 7. D1 prevents the shutdown divider from altering current limit.

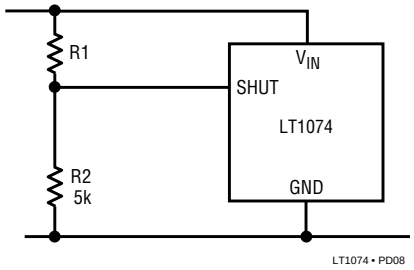

Figure 6. Undervoltage Lockout

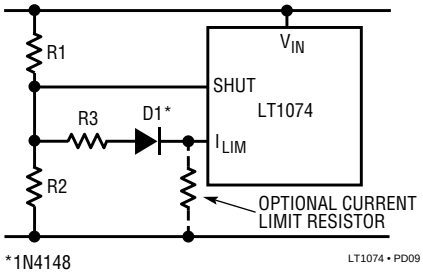

Figure 7. Adding Hysteresis

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$$\text{Trip Point} = V_{TP} = 2.35V\left(1+\frac{R1}{R2}\right)$$

If R3 is added, the lower trip point (V_{IN} descending) will be the same. The upper trip point (V_{UTP}) will be;

$$V_{UTP} = V_{SH}\left(1+\frac{R1}{R2}+\frac{R1}{R3}\right)-0.8V\left(\frac{R1}{R3}\right)$$

If R1 and R2 are chosen, R3 is given by

$$R3 = \frac{\left(V_{SH}-0.8V\right)\left(R1\right)}{V_{UTP}-V_{SH}\left(1+\frac{R1}{R2}\right)}$$

Example: An undervoltage lockout is required such that the output will not start until V_{IN} = 20V, but will continue to operate until V_{IN} drops to 15V. Let R2 = 2.32k.

$$R1 = \left(2.32k\right)\frac{\left(15V-2.35V\right)}{2.35V} = 12.5k$$

$$R3 = \frac{\left(2.35-0.8\right)\left(12.5\right)}{20-2.35\left(1+\frac{12.5}{2.32}\right)} = 3.9k$$

STATUS PIN (AVAILABLE ONLY ON LT1176 PARTS)

The status pin is the output of a voltage monitor "looking" at the feedback pin. It is low for a feedback voltage which is more than 5% above or below nominal. "Nominal" in this case means the internal reference voltage, so that the ±5% window tracks the reference voltage. A time delay of ≈ 10µs prevents short spikes from tripping the status low. Once it does go low, a second timer forces it to stay low for a minimum of ≈ 30µs.

The status pin is modeled in Figure 8 with a 130µA pullup to a 4.5V clamp level. The sinking drive is a saturated NPN with ≈100Ω resistance and a maximum sink current of approximately 5mA. An external pullup resistor can be added to increase output swing up to a maximum of 20V.

When the status pin is used to indicate "output OK," it becomes important to test for conditions which might create unwanted status states. These include output overshoot, large signal transient conditions, and excessive output ripple. "False" tripping of the status pin can usually be controlled by a pulse stretcher network as shown in Figure 8. A single capacitor (C1) will suffice to delay an output "OK" (status high) signal to avoid false "true" signals during start-up, etc. Delay time for status high will be approximately (2.3×10^4) (C1), or 23ms/µF. Status low delay will be much shorter, ≈ 600µs/µF.

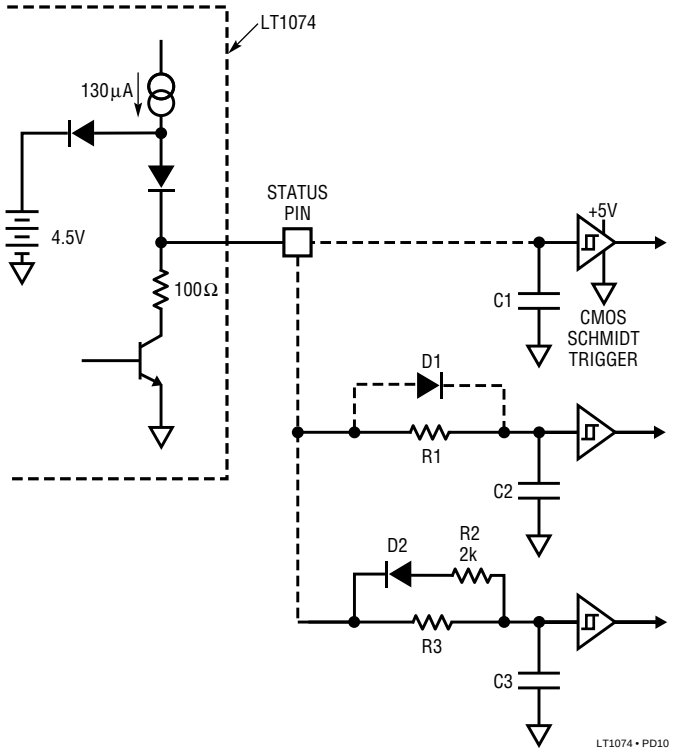

Figure 8. Adding Time Delays to Status Output

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If false tripping of status "low" could be a problem, R1 can be added. Delay of status high remains the same if R1 ≤ 10kΩ. Status low delay is extended by R1 to approximately R1 • C2 seconds. Select C2 for high delay and R1 for low delay.

Example: Delay status high for 10ms, and status low for 3ms.

$$C2 = \frac{10ms}{23ms/\mu F} = 0.47\mu F \left(\text{Use } 0.47\mu F\right)$$

$$R1 = \frac{3ms}{C2} = \frac{3ms}{0.47\mu F} = 6.4k\Omega$$

In this example D1 is not needed because R1 is small enough to not limit the charging of C2.

If very fast "low" tripping combined with long "high" delays is desired, use the D2, R2, R3, C3 configuration. C3 is chosen first to set "low" delay

$$C3 \approx \frac{t_{LOW}}{2k\Omega}$$

R3 is then selected for "high" delay

$$R3 \approx \frac{t_{HIGH}}{C3}$$

For t_{LOW} = 100μs and t_{HIGH} = 10ms, C3 = 0.05μF and R3 = 200kΩ.

I_{LIM} PIN

The I_{LIM} pin is used to reduce current limit below the preset value of 6.5A. The equivalent circuit for this pin is shown in Figure 9.

When I_{LIM} is left open, the voltage at Q1 base clamps at 5V through D2. Internal current limit is determined by the current through Q1. If an external resistor is connected between I_{LIM} and ground, the voltage at Q1 base can be reduced for lower current limit. The resistor will have a voltage across it equal to (320μA) (R), limited to ≈ 5V when clamped by D2. Resistance required for a given current limit is

$$R_{LIM} = I_{LIM}\ (2k\Omega) + 1k\Omega\ (LT1074)$$

$$R_{LIM} = I_{LIM}\ (5.5k\Omega) + 1k\Omega\ (LT1076)$$

As an example, a 3A current limit would require 3A (2k) + 1k = 7kΩ for the LT1074. The accuracy of these formulas is ±25% for 2A ≤ I_{LIM} ≤ 5A (LT1074) and 0.7A ≤ I_{LIM} ≤ 1.8A (LT1076), so I_{LIM} should be set at least 25% above the *peak* switch current required.

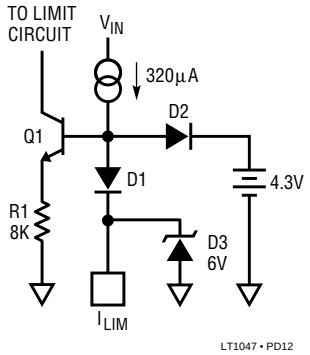

Figure 9. I_{LIM} Pin Circuit

Foldback current limiting can be easily implemented by adding a resistor from the output to the I_{LIM} pin as shown in Figure 10. This allows full desired current limit (with or without R_{LIM}) when the output is regulating, but reduces current limit under short circuit conditions. A typical value for R_{FB} is 5kΩ, but this may be adjusted up or down to set the amount of foldback. D2 prevents the output voltage from forcing current back into the I_{LIM} pin. To calculate a

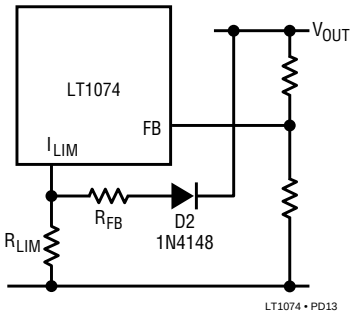

Figure 10. Foldback Current Limit

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value for R_{FB}, first calculate R_{LIM}, then R_{FB};

$$R_{FB} = \frac{(I_{SC} - 0.44^*)(R_L)}{0.5^*(R_L - 1k\Omega) - I_{SC}} = R_L \text{ in} k\Omega$$

*Change 0.44 to 0.16, and 0.5 to 0.18 for LT1076.

Example: I_{LIM} = 4A, I_{SC} = 1.5A, R_{LIM} = (4)(2k) + 1k = 9k

$$R_{FB} = \frac{(1.5 - 0.44)(9k\Omega)}{0.5(9k - 1k) - 1.5} = 3.8k\Omega$$

ERROR AMPLIFIER

The error amplifier in Figure 11 is a single stage design with added inverters to allow the output to swing above and below the common mode input voltage. One side of the amplifier is tied to a trimmed internal reference voltage of 2.21V. The other input is brought out as the FB (feedback) pin. This amplifier has a G_M (voltage "in" to current "out") transfer function of ≈5000μmho. Voltage gain is determined by multiplying G_M times the total equivalent output loading, consisting of the output resistance of Q4 and Q6 in parallel with the series RC external frequency compensation network. At DC, the external RC is ignored, and with a parallel output impedance for Q4 and Q6 of 400kΩ, voltage gain is ≈ 2000. At frequencies above a few hertz, voltage gain is determined by the external compensation, R_C and C_C.

$$A_V = \frac{G_m}{2\pi \bullet f \bullet C_C} \text{ at midfrequencies}$$

$$A_V = G_m \bullet R_C \text{ at high frequencies}$$

Phase shift from the FB pin to the V_C pin is 90° at mid-frequencies where the external C_C is controlling gain, then drops back to 0° (actually 180° since FB is an inverting input) when the reactance of C_C is small compared to R_C. The low frequency "pole" where the reactance of C_C is equal to the output impedance of Q4 and Q6 (r_O), is

$$f_{POLE} = \frac{1}{2\pi \bullet r_0 \bullet C} \quad r_0 \approx 400k\Omega$$

Although f_{POLE} varies as much as 3:1 due to r_O variations, mid-frequency gain is dependent only on G_M, which is specified much tighter on the data sheet. The higher frequency "zero" is determined solely by R_C and C_C.

$$f_{ZERO} = \frac{1}{2\pi \bullet R_C \bullet C_C}$$

The error amplifier has *asymmetrical* peak output current. Q3 and Q4 current mirrors are unity gain, but the Q6 mirror has a gain of 1.8 at output null and a gain of 8 when the FB pin is high (Q1 current = 0). This results in a maximum positive output current of 140μA and a maximum negative (sink) output current of ≅ 1.1mA. The asymmetry is deliberate — it results in much less regulator output overshoot during rapid startup or following the release of an output overload. Amplifier offset is kept low by area scaling Q1 and Q2 at 1.8:1.

Amplifier swing is limited by the internal 5.8V supply for positive outputs and by D1 and D2 when the output goes low. Low clamp voltage is approximately one diode drop (≈ 0.7V – 2mV/°C).

Note that both the FB pin and the V_C pin have other internal connections. Refer to the frequency shifting and sychronizing discussions.

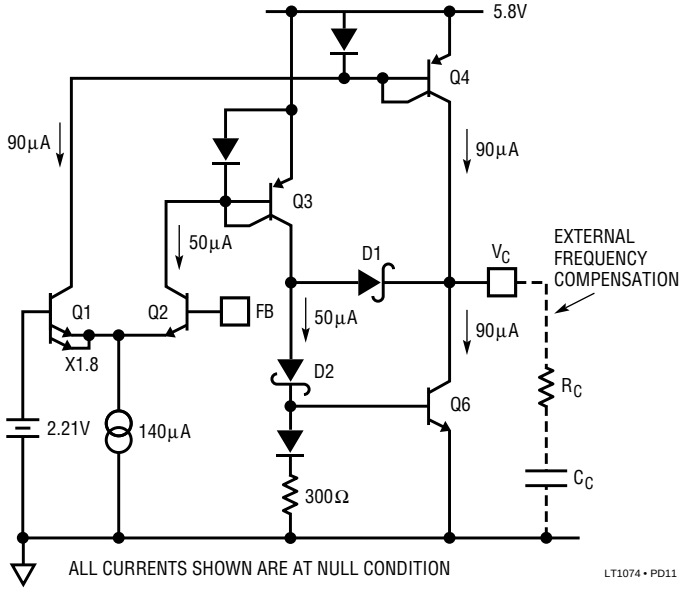


Figure 11. Error Amplifier

DEFINITION OF TERMS

V_{IN}: DC input voltage.

V_{IN}': DC input voltage minus switch voltage loss. V_{IN}' is 1.5 V to 2.3V less than V_{IN}, depending on switch current.

V_{OUT}: DC output voltage.

V_{OUT}': DC output voltage plus catch diode forward voltage. V_{OUT}' is typically 0.4V to 0.6V more than V_{OUT}.

f: Switching frequency.

I_M: Maximum specified switch current I_M = 5.5A for the LT1074 and 2A for the LT1076.

I_{SW}: Switch current during switch on time. The current typically jumps to a starting value, then ramps higher. I_{SW} is the *average* value during this period unless otherwise stated. It is *not* averaged over the whole switching period, which includes switch off time.

I_{OUT}: DC output current.

I_{LIM}: DC output current limit.

I_{DP}: Catch diode forward current. This is the peak current for discontinuous operation and the average value of the current *pulse* during switch off time for continuous mode.

I_{DA}: Catch diode forward current averaged over one complete switching cycle. I_{DA} is used to calculate diode heating.

ΔI: Peak-to-peak ripple current in the inductor, also equal to peak current in the discontinuous mode. ΔI is used to calculate output ripple voltage and inductor core losses.

Vp-p: Peak-to-peak output voltage ripple. This does not include "spikes" created by fast rising currents and capacitor parasitic inductance.

t_{SW}: This is not really an actual rise or fall time. Instead, it represents the *effective* overlap time of voltage and current in the switch. t_{SW} is used to calculate switch power dissipation.

L: Inductance, usually measured with low AC flux density, and zero DC current. Note that large AC flux density can increase L by up to 30%, and large DC currents can decrease L dramatically (core saturation).

B_{AC}: *Peak* AC flux density in the inductor core, equal to one-half peak-to-peak AC flux density. Peak value is used because nearly all core loss curves are plotted with peak flux density.

N: Tapped-inductor or transformer turns ratio. Note the exact definition of N for each application.

μ: Effective permeability of core material used in the inductor. μ is typically 25-150. Ferrite material is much higher, but is usually gapped to reduce the effective value to this range.

V_e: Effective core material volume (cm^3).

L_e: Effective core magnetic path length (cm).

A_e: Effective core cross sectional area (cm^2).

A_w: Effective core or bobbin winding area.

L_t: Average length of one turn on winding.

P_{CU}: Power dissipation caused by winding resistance. It does not include skin effect.

P_C: Power loss in the magnetic core. P_C depends only on *ripple current* in the inductor not DC current.

E: Overall regulator efficiency. It is simply output power divided by input power.

POSITIVE STEP-DOWN (BUCK) CONVERTER

The circuit in Figure 12 is used to convert a larger positive input voltage to a lower positive output. Typical waveforms are shown in Figure 13, with V_{IN} = 20V, V_{OUT} = 5V, L = 50µH, for both continuous mode (inductor current never drops to zero) with I_{OUT} = 3A and discontinuous mode, where inductor current drops to zero during a portion of the switching cycle (I_{OUT} = 0.17A). Continuous mode maximizes output power but requires larger inductors. *Maximum* output current in true discontinuous mode is only one-half of switch current rating. Note that when load current is reduced in a continuous mode design, eventually the circuit will enter discontinuous mode. The LT1074 operates equally well in either mode and there is no significant change in performance when load current reduction causes a shift to discontinuous mode.

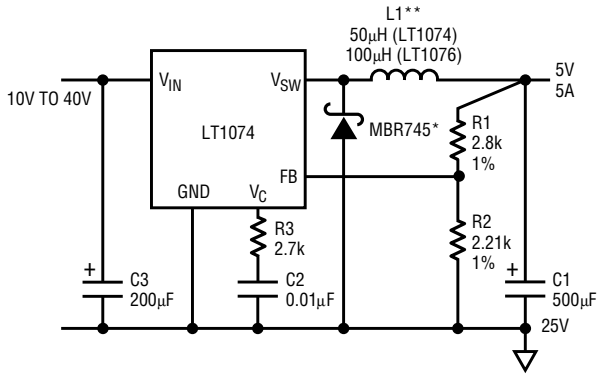


Figure 12. Basic Positive Buck Converter

Duty cycle of a buck converter in continuous mode is

$$DC = \frac{V_{OUT} + V_f}{V_{IN} - V_{SW}} = \frac{V_{OUT}'}{V_{IN}'} \quad (01)$$

V_f = Forward voltage of catch diode
V_{SW} = Voltage loss across "on" switch

Note that duty cycle does not vary with load current except to the extent that V_f and V_{SW} change slightly.

A buck converter will change from continuous to discontinuous mode (and duty cycle will begin to drop) at a load current equal to

$$I_{OUT(CRIT)} = \frac{\left(V_{OUT}'\right)\left(V_{IN}' - V_{OUT}'\right)}{2 \bullet V_{IN}' \bullet f \bullet L} \quad (02)$$

With the possible exception of load transient response, there is no reason to increase L to ensure continuous mode operation at light load.

Using the values from Figure 12, with V_{IN} = 25V, V_f = 0.5V, V_{SW} = 2V

$$DC = \frac{5 + 0.5}{25 - 2} = 24\% \quad (03)$$

$$I_{OUT(CRIT)} = \frac{(5.5)(23 - 5.5)}{2(23)\left(10^5\right)\left(50 \times 10^{-6}\right)} = 0.42A$$

The "ringing" which occurs at some point in the switch "off" cycle in discontinuous mode is simply the resonance created by the catch diode capacitance plus switch capacitance in parallel with the inductor. This ringing does no harm and any attempt to dampen it simply wastes efficiency. Ringing frequency is given by;

$$f_{RING} = \frac{1}{2\pi\sqrt{L \bullet \left(C_{SW} + C_{DIODE}\right)}} \quad (04)$$

$C_{SW} \approx 80pF$
C_{DIODE} = 200pF - 1000pF

No off state ringing occurs in continuous mode because the diode is always conducting during switch off time and effectively shorts the resonance.

A detailed look at the leading edge of the switch waveform may reveal a second "ringing" tendency, usually at frequencies around 20MHz-50MHz. This is the result of the inductance in the loop which includes the input capacitor, the LT1074 leads, and the diode leads, combined with the capacitance of the catch diode. A total lead length of 4 inches will create ≈0.1µH. This coupled with 500pF of diode capacitance will create a damped 25MHz oscillation superimposed on the fast rising switch voltage waveform. Again, no harm is created by this ringing and no attempt should be made to dampen it other than minimizing lead length. Certain board layouts combined with very short interconnects and high diode capacitance may create a tuned circuit which resonates with the switch output to

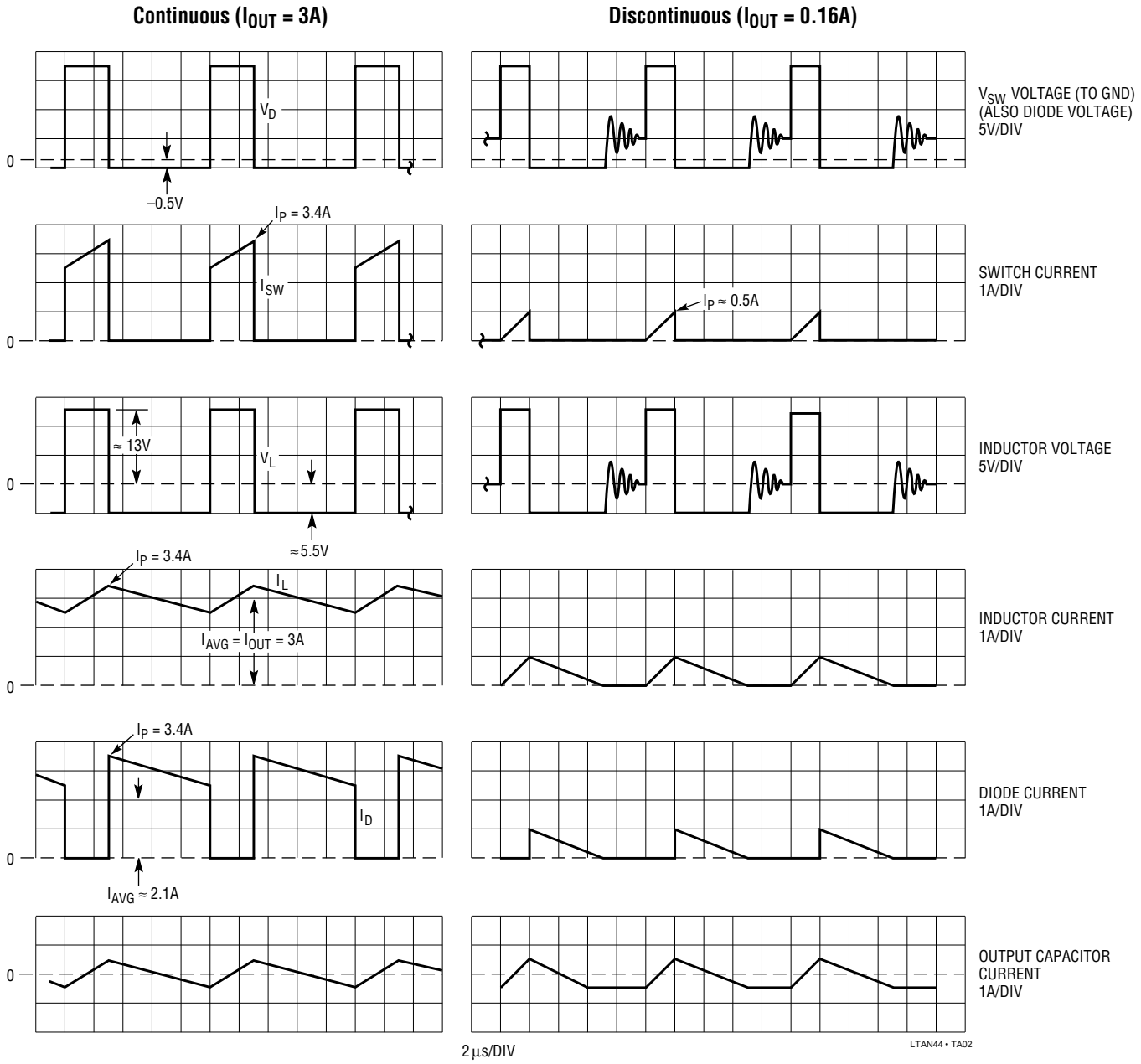


Figure 13. Buck Converter Waveforms with V_{IN} = 20V, L = 50µH

cause a low amplitude oscillation at the switch output during "on" time. This can be eliminated with a ferrite bead slipped over either diode lead during board assembly.

It is interesting to note that standard silicon fast recovery diodes create almost no ringing because of their lower capacitance and because they are effectively damped by their slower turn-off characteristics. This slower turn-off and the larger forward voltage represent additional power loss, so Schottky diodes are normally recommended.

Maximum output current of a buck converter is given by;

Continuous Mode (05)

$$I_{OUT(MAX)} = I_M - \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{2f \bullet V_{IN} \bullet L}$$

I_M = Maximum switch current (5.5A for LT1074)
V_{IN} = DC input voltage (maximum)
V_{OUT} = Output voltage
f = Switching frequency

For the example shown, with L = 50µH, and V_{IN} = 25V,

$$I_{OUT(MAX)} = 5.5 - \frac{5(25-5)}{2\left(10^5\right)(25)\left(50\times10^{-6}\right)} = 5.1A \qquad (06)$$

Note that increasing inductor size to 100µH would only increase maximum output current by 4%, but decreasing it to 20µH would drop maximum current to 4.5A. Low inductance can be used for lower output currents, but core loss will increase.

Inductor

The inductor used in a buck converter acts as both an energy storage element and a smoothing filter. There is a basic tradeoff between good filtering versus size and cost. Typical inductor values used with the LT1074 range from 5µH to 200µH, with the small values used for lower power, minimum size applications and the larger values used to maximize output power or minimize output ripple voltage. The inductor must be rated for currents at least equal to output current and there are restrictions on ripple current (expressed as volt • microsecond product at various frequencies) to avoid core heating. For details on selecting an inductor and calculating losses, see the "Inductor Selection" section.

Output Catch Diode

D1 is used to generate a current path for L1 current when the LT1074 switch turns off. The current through D1 in continuous mode is equal to output current with a duty cycle of $(V_{IN} - V_{OUT})/V_{IN}$. For low input voltages, D1 may operate at duty cycles of 50% or less, but one must be very careful of utilizing this fact to minimize diode heat sinking. First, an unexpected high input voltage will cause duty cycle to increase. More important however, is a shorted output condition. When V_{OUT} = 0, diode duty cycle is ≈1 for any input voltage. Also, in current limit, diode current is not load current, but is determined by LT1074 switch current limit. If continuous output shorts must be tolerated, D1 must be adequately rated and heat sunk. 7 and 11-pin versions of the LT1074 allow current limit to be reduced to limit diode dissipation. 5-pin versions can be accurately current limited using the technique shown in Figure 20.

Under normal conditions, D1 dissipation is given by;

$$P_{DI} = I_{OUT}\frac{(V_{IN} - V_{OUT})}{V_{IN}} \bullet V_f \qquad (07)$$

V_f is the forward voltage of D1 at I_{OUT} current. Schottky diode forward voltage is typically 0.6V at the diode's full rated current, so it is normal design practice to use a diode rated at 1.5 to 2 times output current to maintain efficiency and allow margin for short circuit conditions. This derating allows V_f to drop to approximately 0.5V

Example: $V_{IN(MAX)}$ = 25V, I_{OUT} = 3A, V_{OUT} = 5V, assume V_f = 0.5V;

Full Load (08)

$$P_{DI} = \frac{(3)(25-5)(0.5V)}{25} = 1.2W$$

Shorted Output

$$P_{DI} = (\approx 6A)(DC = 1)(0.6V) = 3.6W$$

The high diode dissipation under shorted output conditions may necessitate current limit adjustment if adequate heat sinking cannot be provided.

Diode switching losses have been neglected because the reverse recovery time is assumed to be short enough to ignore. If a standard silicon diode is used, switching losses cannot be ignored. They can be approximated by;

$$Pt_{rr} \approx (V_{IN})(f)(t_{rr})(I_{OUT}) \qquad (09)$$

t_{rr} = Diode reverse recovery time

Example: Same circuit with t_{rr} = 100ns

$$Pt_{rr} = (25)\left(10^5\right)\left(10^{-7}\right)(3) = 0.75W \qquad (10)$$

Diodes with abrupt turn-off characteristics will transfer most of this power to the LT1074 switch. Soft recovery diodes will dissipate much of the power within the diode itself.

LT1074 Power Dissipation

The LT1074 draws about 7.5mA quiescent current, independent of input voltage or load. It draws an additional 5mA during switch "on" time. The switch itself dissipates a power approximately proportional to load current. This power is due to pure conduction losses (switch "on" voltage times switch current) and dynamic switching losses due to finite switch current rise and fall times. Total LT1074 power dissipation can by calculated from

$$P = V_{IN}\left[7mA + 5mA \bullet DC + 2I_{OUT} \bullet t_{SW} \bullet f\right] + \quad (11)$$

$$DC\left[I_{OUT}\left(1.8V\right)^{*} + 0.1\Omega^{*}\left(I_{OUT}\right)^{2}\right]$$

$$DC = \text{Duty Cycle} \approx \frac{V_{OUT} + 0.5V}{V_{IN} - 2V}$$

t_{SW} = Effective overlap time of switch voltage and current

$\approx$ 50ns + (3ns/A) (I_{OUT}) (LT1074)
$\approx$ 60ns + (10ns/A) (I_{OUT}) (LT1076)

Example: V_{IN} = 25V, V_{OUT} = 5V, f = 100kHz, I_{OUT} = 3A

$$DC = \frac{5 + 0.5}{25 - 2} = 0.196 \quad (12)$$

$$t_{SW} = 50ns + \left(3ns/A\right)\left(3A\right) = 59ns$$

$$P = \quad (13)$$

$$25\left[\begin{array}{l}7mA + 5mA\ (0.196) + \\ (2)\ (3)\ (59ms)\ (10^5)\end{array}\right] + 0.196\left[3\ (1.8) + 0.1\ (3)^2\right]$$

$$= \underbrace{0.21W}_{\substack{\text{Supply}\\ \text{Current}\\ \text{Loss}}} + \underbrace{0.89W}_{\substack{\text{Dynamic}\\ \text{Switching}\\ \text{Loss}}} + \underbrace{1.24W}_{\substack{\text{Switch}\\ \text{Conduction}\\ \text{Loss}}} = 2.34W$$

*LT1076 = 1V, 0.3Ω

Input Capacitor (Buck Converter)

A local input bypass capacitor is normally required for buck converters because the input current is a square wave with fast rise and fall times. This capacitor is chosen by ripple current rating—the capacitor must be large enough to avoid overheating created by its ESR and the AC RMS value of converter input current. For continuous mode;

$$I_{AC,RMS} = I_{OUT}\sqrt{\frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{\left(V_{IN}\right)^2}} \quad (14)$$

Worst case is at $V_{IN} = 2V_{OUT}$.

Power loss in the input capacitor is not insignificant in high efficiency applications. It is simply RMS capacitor current squared times ESR.

$$P_{C3} = \left(I_{AC,RMS}\right)^2\left(ESR\right) \quad (15)$$

Example: V_{IN} = 20V-30V, I_{OUT} = 3A, V_{OUT} = 5V.

Worst case is at $V_{IN} = 2 \bullet V_{OUT}$ = 10V, so use the closest V_{IN} value of 20V;

$$I_{AC,RMS} = 3A\sqrt{\frac{5\left(20 - 5\right)}{\left(20\right)^2}} = 1.3A\ RMS \quad (16)$$

The input capacitor must be rated at a working voltage of 30V minimum and 1.3A ripple current. Ripple current ratings vary with maximum ambient temperature, so check data sheets carefully.

It is important to locate the input capacitor very close to the LT1074 and to use short leads (radial) when the DC input voltage is less than 12V. Spikes as high as 2V/inch of lead length will appear at the regulator input. If these spikes drop below ≈7V, the regulator will exhibit anomalous behavior. See "V_{IN} Pin" in the Pin Descriptions section.

You may be wondering why no mention has been made of capacitor value. That's because it doesn't really matter. Larger electrolytic capacitors are purely resistive (or inductive) at frequencies above 10kHz, so their bypassing impedance is resistive, and ESR is the controlling factor. For input capacitors used with the LT1074, a unit which meets ripple current ratings will provide adequate "bypassing" regardless of its capacitance value. Units with higher voltage rating will have lower capacitance for the same ripple current rating, but as a general rule, the *volume* required to meet a given ripple current/ESR is fixed over a wide range of capacitance/voltage rating. If the capacitor chosen for this application has 0.1Ω ESR, it will have a power loss of $(1.3A)^2$ (0.1Ω) = 0.17W.

Output Capacitor

In a buck converter, output ripple voltage is determined by both the inductor value and the output capacitor;

Continuous Mode (17)

$$Vp-p=\frac{(ESR)(V_{OUT})\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{(L1)(f)}$$

Discontinuous Mode

$$Vp-p=ESR\sqrt{\frac{(2I_{OUT})(V_{OUT})(V_{IN}-V_{OUT})}{L\bullet f\bullet V_{IN}}}$$

Note that only the ESR of the output capacitor is used in the formula. It is assumed that the capacitor is purely resistive at frequencies above 10kHz. If an inductor value has been chosen, the formula can be rearranged to solve for ESR to aid in selecting a capacitor.

Continuous Mode (18)

$$ESR(MAX)=\frac{(Vp-p)(L1)(f)}{V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}$$

Discontinuous Mode

$$ESR(MAX)=Vp-p\sqrt{\frac{L\bullet f\bullet V_{IN}}{2I_{OUT}(V_{OUT})(V_{IN}-V_{OUT})}}$$

Worst case output ripple is at highest input voltage. Ripple is independent of load for continuous mode and proportional to the square root of load current for discontinuous mode.

Example: Continuous mode with $V_{IN(MAX)}$ = 25V, V_{OUT} = 5V, I_{OUT} = 3A, L1 = 50µH, f = 100kHz. Required maximum peak-to-peak output ripple is 25mV.

$$ESR=\frac{(0.025)\left(50\times10^{-6}\right)\left(10^{5}\right)}{(5)\left(1-\frac{5}{25}\right)}=0.03\Omega \quad (19)$$

A 10V capacitor with this ESR would have to be several thousand microfarads, and therefore fairly large. Tradeoffs which could be made include;

A. Paralleling several capacitors if component height is more critical than board area.

B. Increasing inductance. This can be done at no increase in size if a more expensive core (molypermalloy, etc.) is used.

C. Adding an output filter. This is often the best solution because the additional components are fairly low cost and their additional space is minimized by being able to "size down" the main L and C. See the "Output Filter" section.

Although ripple current is not usually a problem with buck converter output capacitors because the current is prefiltered by the inductor, a quick check should be done before a final capacitor is chosen—especially if the capacitor has been "downsized" to take advantage of an additional output filter. RMS ripple current into the output capacitor is

Continuous Mode (20)

$$I_{RMS}=\frac{0.29(V_{OUT})\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{L1\bullet f}$$

From the previous example:

$$I_{RMS}=\frac{0.29(5)\left(1-\frac{5}{25}\right)}{\left(50\times10^{-6}\right)\left(10^{5}\right)}=0.23A\ RMS \quad (21)$$

This ripple current is low enough to not be a problem, but that could change if the inductor was reduced by two or three to one and the output capacitor was minimized by adding an output filter.

The calculations for discontinuous mode RMS ripple current were considered too complicated for this discussion, but a conservative value would be 1.5 to 2 times output current.

To minimize output ripple, the output terminals of the regulator should be connected directly to the capacitor leads so that the diode (D1) and inductor currents do not circulate in output leads.

Efficiency

All the losses except those created by the inductor and the output filter are covered in this buck regulator section. The example used was a 5V, 3A output with 25V input. Calculated losses were: switch, 1.24W; diode, 1.2W; switching times, 0.89W; supply current, 0.21W; and input capacitor, 0.17W. Output capacitor losses were negligible . The sum of all these losses is 3.71W. Inductor loss is covered in a special section of this Application Note. Assume for this application that inductor copper loss is 0.3W and core loss is 0.15W. Total regulator loss is 4.16W. Efficiency is

$$E = \frac{I_{OUT} \bullet V_{OUT}}{I_{OUT} \bullet V_{OUT} + \Sigma P_L} = \frac{(3A)(5V)}{(3A)(5V) + 4.16} = 78\% \quad (22)$$

When considering improvements or tradeoffs of particular loss terms, keep in mind that a change in any one term will be attenuated by efficiency *squared.* For instance, if switch loss were reduced by 0.3W, this is 2% of the 15W output power, but only a $2(0.8)^2$ = 1.28% improvement in efficiency.

Output Divider

R1 and R2 set DC output voltage. R2 is normally set at 2.21kΩ (a standard 1% value) to match the LT1074 reference voltage of 2.21V, giving a divider current of 1mA. R1 is then calculated from

$$R1 = \frac{R2\,(V_{OUT} - V_{REF})}{V_{REF}} \quad (23)$$

If R2 = 2.21kΩ, R1 = $(V_{OUT} - V_{REF})$ kΩ

R2 may be scaled in either direction to suit other needs, but an upper limit of 4kΩ is suggested to ensure that the frequency shifting action created by the FB pin voltage is maintained under shorted output conditions.

Output Overshoot

Switching regulators often exhibit startup overshoot because the 2-pole LC network requires a fairly low unity gain frequency for the feedback loop. The LT1074 has asymmetrical error amplifier slew rate to help reduce overshoot, but it can still be a problem with certain combinations of L1C1 and C2R3. Overshoot should be checked on all designs by allowing the output to slew from zero in a no-load condition with maximum input voltage. This can be done by stepping the input or by pulling the V_C pin low through a diode connected to a 0V-10V square wave.

Worst case overshoot can occur on recovery from an output short because the V_C pin must slew from its high clamp state down to ≈1.3V. This condition is best checked with the brute force method of shorting and releasing the output.

If excessive output overshoot is found, the procedure for reducing it to a tolerable level is to first try increasing the compensation resistor. The error amplifier output must slew negative rapidly to control overshoot and its slew rate is limited by the compensation capacitor. The compensation resistor, however, allows the amplifier output to "step" downward very rapidly before slewing limitations begin. The size of this step is ≈(1.1mA)(R_C). If R_C can be increased to 3kΩ, the V_C pin can respond very quickly to control output overshoot.

If loop stability cannot be maintained with R_C = 3kΩ, there are several other solutions. Increasing the size of the output capacitor will reduce short-circuit-recovery overshoot by limiting output rise time. Reducing current limit will also help for the same reason. Reducing the compensation capacitor below 0.05μF helps because the V_C pin can then slew an appreciable amount during the allowable overshoot time.

The "final solution" to output overshoot is to clamp the V_C pin so that it does not have to slew as far to shut off the output. The V_C pin voltage in normal operation is known fairly precisely because it is made independent of everything except output voltage by the internal multiplier;

$$V_C \text{ Voltage} \approx 2\phi + \frac{V_{OUT}}{24} \quad (24)$$

$\phi = V_{BE}$ of internal transistor = 0.65V – 2mV/°C

To allow for transient conditions and circuit tolerances, a slightly different expression is used to calculate clamp level for the V_C pin

$$V_{C(CLAMP)} = 2\phi + \frac{V_{OUT}}{20} + \frac{V_{IN(MAX)}}{50} + 0.2V \quad (25)$$

For a 5V output with $V_{IN(MAX)}$ = 30V,

$$V_{C(CLAMP)} = 2(0.65) + \frac{5}{20} + \frac{30}{50} + 0.2 = 2.35V \quad (26)$$

There are several ways to clamp the V_C pin as shown in Figure 14. The simplest way is to just add a clamp Zener (D3). The problem is finding a low voltage Zener which does not leak badly below the knee. Maximum Zener leakage over temperature should be 40µA @ $V_C = 2\phi + V_{OUT}/20V$. One solution is to use an LM385-2.5V micropower reference diode where the calculated clamp level does not exceed 2.5V.

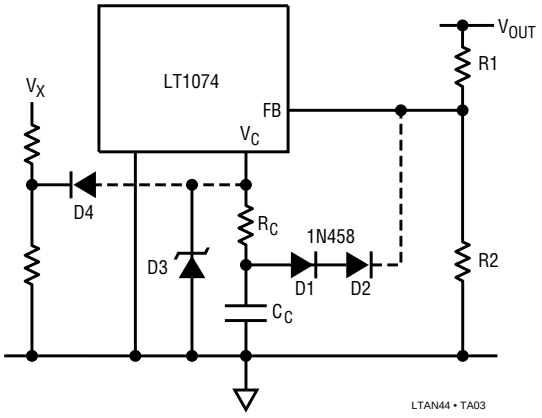


Figure 14. Clamping the V_C Pin

A second clamp scheme is to use a voltage divider and diode (D4). V_X must be some quasi-regulated source which does not collapse with regulator output voltage. A third technique can be used for outputs up to 20V. It clamps the V_C pin to the feedback pin with two diodes, D1 and D2. These are small signal nongold doped-diodes with a forward voltage that matches ϕ. The reason for this is start-up. V_C is essentially clamped to ground through the output divider when V_{OUT} = 0. It must be allowed to rise sufficiently to ensure start-up. The feedback pin will sit at about 0.5V with V_{OUT} = 0, because of the combined current from the feedback pin and V_C pin. The V_C voltage will be 2ϕ + 0.5V + (0.14mA) (R_C). With R_C = 1kΩ, V_C = 1.94. This is plenty to ensure start-up.

Overshoot Fixes that Don't Work

I know that these things don't work because I tried them. The first is soft start, created by allowing the output current or the V_C voltage to ramp up slowly. The first problem is that a slowly rising output allows more time for the V_C pin to ramp up well beyond its nominal control point so that it has to slew farther down to stop overshoot. If the V_C pin itself is ramped slowly, this can control input start-up overshoot, but it becomes very difficult to guarantee reset of the soft start for all conditions of input sequencing. In any case, these techniques do not address the problem of overshoot following overload of the output, because they do not get "reset" by the output.

Another common practice is to parallel the upper resistor in the output divider with a capacitor. This again works fine under limited conditions, but it is easily defeated by overload conditions which pull the output slightly below its regulated point long enough for the V_C pin to hit the positive limit (≈6V). The added capacitor remains charged and the V_C pin must slew almost 5V to control overshoot when the overload is released. The resulting overshoot is impressive—and often deadly.

TAPPED-INDUCTOR BUCK CONVERTER

Output current of a buck converter is normally limited to maximum switch current, but this restriction can be altered by tapping the inductor as shown in Figure 15. The ratio of "input" turns to "output" turns is "N" as shown in the schematic. The effect of the tap is to lengthen switch "on" time and therefore draw more power from the input without raising switch current. During switch "on" time, current delivered to the output through L1 is equal to switch current—5.5A maximum for the LT1074. When the switch turns off, inductor current flows only in the output section of L1, labeled "1," through D1 to the output. Energy conservation in the inductor requires that current increase by the ratio (N + 1):1. If N = 3, then maximum current delivered to the output during switch

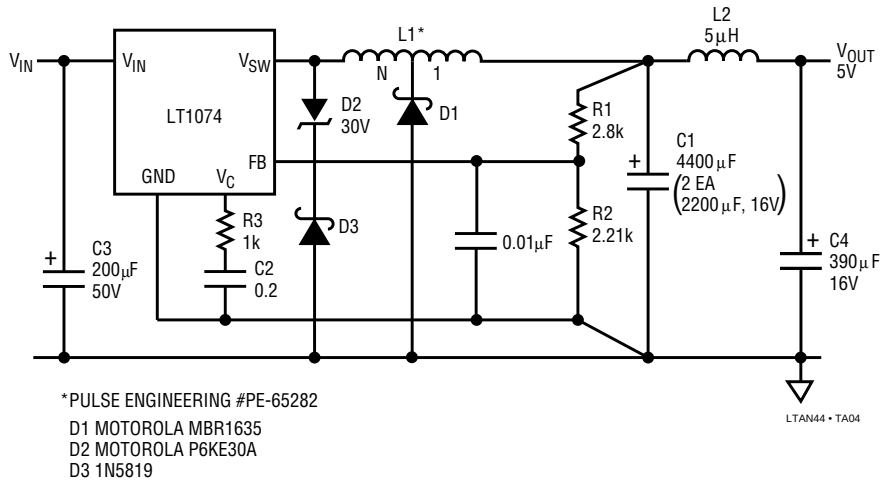


Figure 15. Tapped-Inductor Buck Converter

off time is (3 + 1)(5.5A) = 22A. Average load current is increased to the weighted average of the 5A and 22A currents. Maximum output current is given by;

$$I_{OUT(MAX)} = \quad (27)$$

$$0.95\left[I_{SW} - \frac{\left(V_{IN}' - V_{OUT}'\right)\left(1+N\right)}{2Lf\left(N + \frac{V_{IN}'}{V_{OUT}'}\right)}\right]\left[\frac{N+1}{1+\frac{N \bullet V_{OUT}'}{V_{IN}'}}\right]$$

L = Total Inductance

The last term, $(N + 1)/(1 + N \bullet V_{OUT}/V_{IN})$ is the basic switch current multiplier term. At high input voltages it approaches N + 1, and theoretical output current approaches 18A for N = 3. For lower input voltages the multiplier term approaches unity and no benefit is gained by tapping the inductor. Therefore, when calculating maximum load current capability, always use the worst case low input voltage. The 0.95 multiplier is thrown-in to account for second order effects of leakage inductance, etc.

Example: $V_{IN(MIN)}$ = 20V, N = 3, L =100µH, V_{OUT} = 5V, Diode V_f = 0.55V, f =100kHz. Let I_{SW} = Maximum for LT1074 = 5.5A, V_{OUT}' = 5V + 0.55V = 5.55V, V_{IN}' = 20V – 2V = 18V

$$I_{OUT(MAX)} = \quad (28)$$

$$0.95\left[5.5 - \frac{\left(18-5.55\right)\left(1+3\right)}{2\left(10^{-4}\right)\left(10^{5}\right)\left(3+\frac{18}{5.5}\right)}\right]\left[\frac{3+1}{1+\frac{3\left(5.55\right)}{18}}\right]$$

$$= 0.95\left[5.5-0.4\right]\left[2.08\right] = 10.08A$$

Duty cycle of the tapped-inductor converter is equal to;

$$DC = \frac{1+N}{N+\frac{V_{IN}'}{V_{OUT}'}} \quad (29)$$

Average and peak diode currents are

$$I_{D(AVG)} = \frac{I_{OUT}\left(V_{IN}' - V_{OUT}'\right)}{V_{IN}'} \quad (30)$$

$$\left(\text{Use Maximum } V_{IN}'\right)$$

$$I_{D(PEAK)} = \frac{I_{OUT}\left(N\,V_{OUT}' + V_{IN}'\right)}{V_{IN}'}$$

$$\left(\text{Use Minimum } V_{IN}'\right)$$

Average switch current *during switch on time is*

$$I_{SW(AVG)} = \frac{I_{OUT}\left(N \bullet V_{OUT}' + V_{IN}'\right)}{V_{IN}'\left(1+N\right)} \quad (31)$$

$$\left(\text{Use Minimum } V_{IN}'\right)$$

Diode peak reverse voltage is

$$V_{DI(PEAK)} = \frac{V_{IN} + N \bullet V_{OUT}}{1+N} \quad (32)$$

$$\left(\text{Use Maximum } V_{IN}\right)$$

Switch reverse voltage is

$$V_{SW} = V_{IN} + V_Z + V_{SPIKE} \quad (33)$$

$$\left(\text{Use Maximum } V_{IN}\right)$$

V_Z = Reverse breakdown of D2 (30V)
V_{SPIKE} = Narrow (<100ns) spike created by rapid switch turnoff and the stray wiring inductance of C3, D2, D3, and the LT1074 V_{IN} and switch pins. This voltage spike is approximately $I_{SW}/2$ *volts per inch* of total lead length.

Using parameters from the maximum output current example, with $V_{IN(MAX)}$ = 30V, I_{OUT} = 8A

$$DC @ V_{IN} = 20V = \frac{1+3}{3+\frac{18}{5.55}} = 64\% \quad (34)$$

$$I_{D(AVG)} = \frac{\left(8\right)\left(28-5.55\right)}{28} = 6.7A$$

$$I_{D(PEAK)} @ V_{IN} = 20V = \frac{\left(8\right)\left(3 \bullet 5.55 + 18\right)}{18} = 15.4A$$

$$I_{SW(AVG)} @ V_{IN} = 20V = \frac{\left(8\right)\left(3 \bullet 5.55 + 18\right)}{18\left(1+3\right)} = 3.85A$$

Note that this is the average switch current during "on" time. It must be multiplied by duty cycle and switch voltage drop to obtain switch power loss. Total loss also includes switch fall time (rise time losses are minimal due to leakage inductance in L1).

$$P_{SWITCH} = \left(I_{SW}\right)\left(DC\right)\left[1.8V + \left(0.1\right)\left(I_{SW}\right)\right] + \left(V_{IN}' + V_Z\right)\left(I_{SW}\right)\left(f\right)\left(t_{SW}\right) \quad (35)$$

$$t_{SW} = 50ns + 3ns \bullet I_{SW}$$

$$= \left(3.85\right)\left(0.64\right)\left[1.8 + \left(0.1\right)\left(3.85\right)\right] + \left(20+30\right)\left(3.85\right)\left(10^5\right)\left(62ns\right)$$

$$= 5.3W + 1.19W = 6.5W$$

$$V_{DI(PEAK)} = \frac{30+3.5}{1+3} = 11.25V \quad (36)$$

$$V_{SW} = 30 + 30 + \frac{3.85}{2}\left(2''\right)^* = 64V$$

* This assumes 2" of lead length

Snubber

The tapped-inductor converter requires a snubber (D2 and D3) to clip off negative switching spikes created by the leakage inductance of L1. This inductance (L_L) is the value measured between the tap and the switch (N) terminal with the tap shorted to the output terminal. Theoretically, the measured inductance will be zero because the shorted turns reflect "0" ohms back to any other terminals. In practice, even with bifilar winding techniques, there is ≥1% leakage inductance compared to total inductance. This is ≈1.2µH for the PE-65282. L_L is modeled as a separate inductance in series with the "N" section input, which does not couple to the rest of the inductor. This gives rise to a negative spike at the switch pin at switch turnoff. D2 and D3 clip this spike to prevent switch damage, but D2 dissipates a significant amount of power. This power is equal to the energy stored in L_L at switch turnoff, ($E = (I_{SW})^2 \bullet L_L/2$) multiplied by switching frequency and a multiplier term which is dependent on the *difference* between D2 voltage and the normal reverse voltage swing at the inductor input.

$$P_{D2} = \frac{\left(I_{SW}\right)^2 \bullet L_L}{2}\left(f\right)\left(\frac{V_Z}{V_Z - V_{OUT}' \bullet N}\right) \quad (37)$$

For this example;

$$P_{D2} = \frac{(3.85)^2\left(1.2\times10^{-6}\right)\left(10^5\right)}{2}\left(\frac{30}{30-5.55\bullet3}\right) = 2W \quad (38)$$

Output Ripple Voltage

Output ripple on a tapped-inductor converter is higher than a simple buck converter because a square wave of current is superimposed on the normal triangular current fed to the output. Peak-to-peak ripple current delivered to the output is:

$$Ip-p = \frac{I_{OUT}\left(N\bullet V_{OUT}+V_{IN}\right)(N)}{V_{IN}\left(1+N\right)} + \frac{\left(1+N\right)\left(V_{IN}-V_{OUT}\right)}{f\bullet L\left(N+\frac{V_{IN}}{V_{OUT}}\right)} \quad (39)$$

$$\left(\text{Use Minimum } V_{IN}\right)$$

A conservative approximation of RMS ripple current is one-half of peak-to-peak current.

Output ripple voltage is simply the ESR of the output capacitor multiplied times Ip-p. In this example, with ESR = 0.03Ω

$$Ip-p = \frac{(8)(3\bullet5+20)(3)}{20(1+3)} + \frac{(1+3)(20-5)}{\left(10^5\right)\left(10^{-4}\right)\left(3+\frac{20}{5}\right)} = 11.4A \quad (40)$$

$$I_{RMS} = 5.7A$$

$$Vp-p = (0.03)(11.4) = 340mV$$

This high value of ripple current and voltage requires some thought about the output capacitor. To avoid an excessively large capacitor, several smaller units are paralleled to achieve a combined 5.7A ripple current rating. The ripple voltage is still a problem for many applications. However, to reduce ripple voltage to 50mV would require an ESR of less than 0.005W—an impractical value. Instead, an output filter is added which attenuates ripple by more than 20:1.

Input Capacitor

The input bypass capacitor is selected by ripple current rating. It is assumed that all the converter input ripple current is supplied by the input capacitor. RMS input ripple current is approximately

$$I_{IN(RMS)} \approx \frac{\left(I_{OUT}\right)\left(V_{OUT}'\right)}{\left(V_{IN}'\right)\left(1+N\right)}\sqrt{\left(1+N\right)\left(\frac{V_{IN}'}{V_{OUT}'}-1\right)} \quad (41)$$

$$\left(\text{Use Minimum } V_{IN}\right)$$

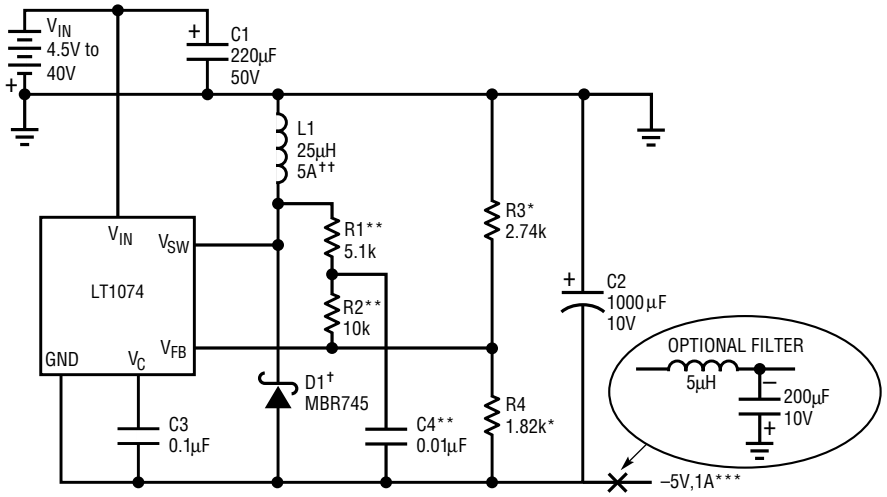
$$= \frac{(8)(5.5)}{(18)(1+3)}\sqrt{(1+3)\left(\frac{18}{5.5}-1\right)} = 1.84A \text{ RMS}$$

The input capacitor value in microfarads is not particularly important since it is purely resistive at 100kHz; but it must be rated at the required ripple current and maximum input voltage. Radial lead types should be used to minimize lead inductance.

POSITIVE TO NEGATIVE CONVERTER

The LT1074 can be used to convert positive voltages to negative if the *sum* of input and output voltage is greater than the 8V minimum supply voltage specification, and the minimum positive supply is 4.75V. Figure 16 shows the LT1074 used to generate negative 5V. The ground pin of the device is connected to the negative output. This allows the feedback divider, R3 and R4, to be connected in the normal fashion. If the ground pin were tied to ground, some sort of level shift and inversion would be required to generate the proper feedback signal.

Positive to negative converters have a “right half plane zero” in the transfer function which makes them particularly hard to frequency stabilize, especially with low input voltage. R1, R2, and C4 have been added to the basic design solely to guarantee loop stability at low input voltage. They may be omitted for $V_{IN} > 10V$, or $V_{IN}/V_{OUT} > 2$. R1 plus R2 is in parallel with R3 for DC output voltage calculations. Use the following guidelines for these resistors:



* = 1% FILM RESISTORS
D1 = MOTOROLA-MBR745
C1 = NICHICON-UPL1C221MRH6
C2 = NICHICON-UPL1A102MRH6
L1 = COILTRONICS-CTX25-5-52

† LOWER REVERSE VOLTAGE RATING MAY BE USED FOR LOWER INPUT VOLTAGES. LOWER CURRENT RATING IS ALLOWED FOR LOWER OUTPUT CURRENT.

†† LOWER CURRENT RATING MAY BE USED FOR LOWER OUTPUT CURRENT.

** R1, R2, AND C4 ARE USED FOR LOOP FREQUENCY COMPENSATION, BUT R1 AND R2 MUST BE INCLUDED IN THE CALCULATION FOR OUTPUT VOLTAGE DIVIDER VALUES. FOR HIGHER OUTPUT VOLTAGES, INCREASE R1, R2 AND R3 PROPORTIONATELY;
$R3 = V_{OUT} - 2.37\ (K\Omega)$
R1 = (R3) (1.86)
R2 = (R3) (3.65)

*** MAXIMUM OUTPUT CURRENT OF 1A IS DETERMINED BY MINIMUM INPUT VOLTAGE OF 4.5V. HIGHER MINIMUM INPUT VOLTAGE WILL ALLOW MUCH HIGHER OUTPUT CURRENTS.

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Figure 16. Positive to Negative Converter

R4 = 1.82k
$R3 = |V_{OUT}| - 2.37$ (In kΩ)
R1 = R3 (1.86)
R2 = R3 (3.65)

If R1 and R2 are omitted:

R4 = 2.21k
$R3 = |V_{OUT}| - 2.21$ (In kΩ)

A +12V to –5V converter would have R4 = 2.21k and R3 = 2.74k.

Recommended compensation components would be C3 = 0.005µF in parallel with a series RC of 0.1µF and 1kΩ.

The converter works by charging L1 through the input voltage when the LT1074 switch is "on." During switch "off" time, the inductor current is diverted through D1 to the negative output. For continuous mode operation, duty cycle of the switch is

$$DC = \frac{V_{OUT}'}{V_{IN}' + V_{OUT}} \quad (42)$$

$\left(\text{Use absolute value for } V_{OUT}\right)$

Peak switch current for continuous mode is

$$I_{SW(PEAK)} = \quad (43)$$

$$\frac{I_{OUT}\left(V_{IN}' + V_{OUT}'\right)}{V_{IN}'} + \frac{\left(V_{IN}'\right)\left(V_{OUT}'\right)}{2f \bullet L\left(V_{IN}' + V_{OUT}'\right)}$$

To calculate maximum output current for a given maximum switch current (I_M) this can be rearranged as;

$$I_{OUT(MAX)} = \quad (44)$$

$$\frac{V_{IN}' - \left(I_M\right)\left(R_L\right)}{V_{IN}' + V_{OUT}'}\left[I_M - \frac{\left(V_{IN}'\right)\left(V_{OUT}'\right)}{2f \bullet L\left(V_{IN}' + V_{OUT}'\right)}\right]$$

$\left(\text{Use Minim um } V_{IN}'\right)$

Note that an extra term ($I_M \bullet R_L$) has been added. This is to account for the series resistance (R_L) of the inductor, which may become a significant loss at low input voltages.

Maximum output current is dependent upon input *and* output voltage, unlike the buck converter which will supply essentially a constant output current. The circuit shown will supply over 4A at V_{IN} = 30V, but only 1.3A at V_{IN} = 5V. The $I_{OUT(MAX)}$ equation does not include second order loss terms such as capacitor ripple current, switch rise and fall time, core loss, and output filter. These factors may reduce maximum output current by up to 10% at low input and/or output voltages. Figure 17 shows $I_{OUT(MAX)}$ versus input voltage for various output voltages. It assumes a 25µH inductor for V_{OUT} = –5V, 50µH for V_{OUT} = –12V, and 100µH for V_{OUT} = –25V.

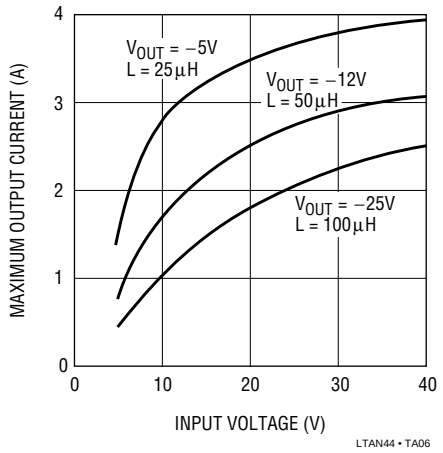

Figure 17. Maximum Output Current of Positive to Negative Converter

If absolute minimum circuit size is required and load currents are not too high, discontinuous mode can be used. Minimum inductance required for a specified load is;

Discontinuous Mode (45)

$$L_{MIN} = \frac{2I_{OUT}\left(V_{OUT}'\right)}{\left(I_M\right)^2 \bullet f}$$

There is a maximum load current that can be supplied in discontinuous mode. Above this current, the formula for L_{MIN} is invalid. Maximum load current in discontinuous mode is;

Discontinuous Mode (46)

$$I_{OUT(MAX)} = \left(\frac{V_{IN}'}{V_{IN}' + V_{OUT}'}\right)\left(\frac{I_M}{2}\right)$$

$\left(\text{Use Minimum } V_{IN}\right)$

Example: V_{OUT} = 5V, I_M = 5A, f = 100kHz, Load Current = 0.5A. Diode Forward Voltage = 0.5V, giving V_{OUT}' = 5.5V. V_{IN} = 4.7V to 5.3V. Assume $V_{IN}'_{(MIN)}$ = 4.7V – 2.3V = 2.4V.

$$I_{OUT(MAX)} = \left(\frac{2.4}{2.4 + 5.5}\right)\left(\frac{5}{2}\right) = 0.76A \quad (47)$$

The required load current of 0.5A is less than the maximum of 0.76A, so discontinuous can be used.

$$L_{MIN} = \frac{2\left(0.5\right)\left(5.5\right)}{\left(5\right)^2\left(10^5\right)} = 2.2\mu H \quad (48)$$

To ensure full load current with production variations of frequency and inductance, 3µH should be used.

The formula for minimum inductance assumes a high peak current in the inductor (≈5A). If the minimum inductance is used, the inductor must be specified to handle the high peak current without saturating. The high ripple current will also cause relatively high core loss and output ripple voltage, so some judgment must be used in minimizing the inductor size. See the "Inductor Selection" section for more details.

To calculate peak inductor and switch current in discontinuous mode, use

$$I_{PEAK} = \sqrt{\frac{2 \bullet I_{OUT} \bullet V_{OUT}'}{L \bullet f}} \quad (49)$$

Input Capacitor

C3 is used to absorb the large square wave switching currents drawn by positive to negative converters. It must have low ESR to handle the RMS ripple current and to avoid input voltage "dips" during switch on time, especially with 5V inputs. Capacitance value is not particularly important if ripple current and operating voltage requirements are met. RMS ripple current in the capacitor is

Continuous Mode (50)

$$I_{RMS} = I_{OUT}\sqrt{\frac{V_{OUT}'}{V_{IN}'}}$$

(Use Minimum V_{IN})

Discontinuous Mode* (51)

$$I_{RMS} = \frac{(I_{OUT})(V_{OUT}')}{V_{IN}'}\sqrt{\frac{1.35\left(1-\frac{m}{2}\right)^3}{m} + 0.17m^2 + 1 - m}$$

$$m = \frac{1}{V_{IN}'}\sqrt{2Lf\,I_{OUT}\,V_{OUT}'}$$

*This formula is a test for calculator students

Examples: A continuous mode design with V_{IN} = 12V, V_{OUT} = –5V, I_{OUT} = 1A, V_{OUT}' = 5.5V, and V_{IN}' = 10V.

$$I_{RMS} = (1)\sqrt{\frac{5.5}{10}} = 0.74A\ RMS \quad (52)$$

Now change to a discontinuous design with the same conditions and L = 5µH, f = 100kHz.

$$m = \frac{1}{10}\sqrt{(2)\left(10\times10^{-6}\right)(105)(1)(5.5)} = 0.33 \quad (53)$$

$$I_{RMS} = \frac{(1)(5.5)}{10}\sqrt{\frac{1.35\left(1-0.165\right)^3}{0.33} + 0.17\left(0.33\right)^2 + 1 - 0.33}$$

$$= 0.96A\ RMS$$

Notice that discontinuous mode saves on inductor size, but may require a a larger input capacitor to handle the ripple current increase. The 30% increases in ripple current generates 70% more heating in the capacitor ESR.

Output Capacitor

The inductor on a positive to negative converter does not operate as a filter. It simply acts as an energy storage device so that energy can be transferred from input to output. Therefore, all filtering is done by the output capacitor, and it must have adequate ripple current rating and low ESR. Output ripple voltage for continuous mode will contain three distinct components; a "spike" on switch transitions which is equal to the rate of rise/fall of switch current multiplied by the effective series inductance (ESL) of the output capacitor, a square wave proportional to load current and capacitor ESR, and a triangular component dependent on inductor value and ESR. The spikes are very narrow, typically less than 100ns, and often "disappear" in the parasitic filter created by the inductance of PC board traces between the converter and load combined with the load bypass capacitors. One must be extremely careful when looking at these spikes with an oscilloscope. The magnetic fields created by currents transitions in converter wiring will generate "spikes" on the screen even when they do not exist at the converter output. See the "Oscilloscope Techniques" section for details.

The peak-to-peak sum of square wave and triangular output ripple voltage is

$$Vp-p = ESR\left[\frac{I_{OUT}\left(V_{IN}' + V_{OUT}'\right)}{V_{IN}'} + \frac{\left(V_{OUT}'\right)\left(V_{IN}'\right)}{2\left(V_{OUT}+V_{IN}\right)(f)(L)}\right] \quad (54)$$

$\left(\text{Use Minimum } V_{IN}'\right)$

Example: V_{IN} = 5V, V_{OUT} = –5V, L = 25µH, $I_{OUT(MAX)}$ = 1A, f = 100kHz. Assume V_{IN}' = 2.8V, V_{OUT}' = 5.5V, and ESR = 0.05Ω.

$$Vp-p = 0.05\left[\frac{(1)(2.8+5.5)}{2.8} + \frac{(5.5)(2.8)}{2\left(5.5+2.8\right)\left(10^5\right)\left(25\times10^{-6}\right)}\right] \quad (55)$$

$$= 172mV$$

For some applications this rather high ripple voltage may be acceptable, but more commonly it will be necessary to reduce ripple voltage to 50mV or less. This may be impractical to achieve simply by reducing ESR, so an output filter (L2, C4) is shown, The filter components are relatively small and low cost, both of which are additionally offset by possible reduction in the size of the main output capacitor C1. See the "Output Filters" section for details.

C1 must be chosen for ripple current as well as ESR. Ripple current into the output capacitor is given by;

Continuous Mode (56)

$$I_{RMS} = I_{OUT}\sqrt{\frac{V_{OUT}'}{V_{IN}'}}$$

Discontinuous Mode (57)

$$I_{RMS} = I_{OUT}\sqrt{\frac{0.67\left(I_P - I_{OUT}\right)^3}{I_{OUT}\left(I_P\right)^2} + \frac{0.67\left(I_{OUT}\right)^2}{\left(I_P\right)^2} + 1 - \frac{2I_{OUT}}{I_P}}$$

Where I_P = Peak Inductor Current

$$= \sqrt{\frac{2I_{OUT}\left(V_{OUT}'\right)}{L \bullet f}}$$

For the Continuous Mode example

$$I_{RMS} = (1A)\sqrt{\frac{5.5}{2.8}} = 1.4A\ RMS \quad (58)$$

With Discontinuous Mode using a 3µA inductor, with I_{OUT} = 0.5A

$$I_P = \sqrt{\frac{(2)(0.5)(5.5)}{\left(3\times10^{-6}\right)\left(10^5\right)}} = 4.28A \quad (59)$$

$$I_{RMS} = (0.5)\sqrt{\frac{(0.67)(4.28-0.5)^3}{(0.5)(4.28)^2} + \frac{(0.67)(0.5)^2}{(4.28)^2} + 1 - \frac{2(0.5)}{4.28}}$$

$$= 1.09A\ RMS$$

Notice that output capacitor ripple current is over twice the DC output current in this discontinuous example. The smaller inductor size obtained by discontinuous mode may be somewhat offset by the larger capacitors required on input and output to meet ripple current conditions.

Efficiency

Efficiency for this positive to negative converter can be quite high for larger input and output voltages (>90%), but can be much lower for low input voltages. Losses are summarized below for a continuous mode design. Discontinuous losses are much more difficult to express analytically, but will typically be 1.2 to 1.3 times higher than in continuous mode.

Conduction loss in switch = P_{SW} (DC)

$$P_{SW}(DC) = \frac{\left(I_{OUT}\right)\left(V_{OUT}'\right)}{V_{IN}'}\left[1.8V + \frac{(0.1)\left(I_{OUT}\right)\left(V_{OUT}' + V_{IN}'\right)}{V_{IN}'}\right] \quad (60)$$

Transient switch loss = P_{SW} (AC)

$$P_{SW}(AC) = \frac{I_{OUT}\left(V_{OUT}' + V_{IN}'\right)^2 2\left(t_{SW}\right)(f)}{V_{IN}'} \quad (61)$$

Where t_{SW} = 50ns + 3ns $(V_{OUT}' + V_{IN}')/V_{IN}'$. The LT1074 quiescent current generates a loss called P_{SUPPLY}

$$P_{SUPPLY} = \left(V_{IN}' + V_{OUT}'\right)\left[\frac{7mA + 5mA\left(V_{OUT}'\right)}{\left(V_{OUT}' + V_{IN}'\right)}\right] \quad (62)$$

Catch diode loss = $P_{DI} = (I_{OUT})(V_f)$

Where V_f = Forward Voltage of D1 at a current equal to;

$I_{OUT}\ (V_{OUT}' + V_{IN}')/V_{IN}'$

Capacitor losses can be found by calculating RMS ripple current and multiplying by capacitor ESR. Inductor losses are the sum of copper (wire) loss and core loss

$$P_{L1} = R_L\left[\frac{\left(I_{OUT}\right)\left(V_{OUT}' + V_{IN}'\right)}{V_{IN}'}\right]^2 + P_{CORE} \quad (63)$$

R_L = Inductor Copper Resistance

P_{CORE} can be calculated if the inductor core material is known. See the "Inductor Selection" section.

Example: V_{IN} = 12V, V_{OUT} = –12V, I_{OUT} = 1.5A, f = 100kHz. Let L1= 50µH, with R_L = 0.04Ω. Assume ESR of input and output capacitor is 0.05Ω. V_{IN}' = 12V – 2V = 10V, V_{OUT}' = 12V + 0.5V = 12.5V.

$$P_{SW}(DC) = \frac{(1.5)(12.5)}{10}\left[1.8 + \frac{(0.1)(1.5)(12.5+10)}{10}\right] = 4W \quad (64)$$

$$P_{SW}(AC) = \frac{(1.5)(12.5+10.5)^2}{10}\left[2(50ns+3ns)\frac{(12.5+10)}{10}\right](10^5) = 0.86W$$

$$P_{SUPPLY} = (12+12)\left[7mA + \frac{5mA(12.5)}{12.5+10}\right] = 0.23W$$

$$P_{DI} = (1.5)(0.5) = 0.75W$$

$$I_{RMS(INPUT\ CAP)} = 1.5\sqrt{\frac{12.5}{10}} = 1.68A\ RMS$$

$$P_{C3} = (1.68)^2(0.05) = 0.14W$$

$$I_{RMS(OUTPUT\ CAP)} = I_{OUT}\sqrt{\frac{(12.5)^2 + (12.5)(10)}{(10)(12.5+10)}} = 1.68A\ RMS$$

$$P_{C1} = (1.68)^2(0.05) = 0.14W$$

$$P_{L1} = 0.04\left[\frac{(1.5)(12.5+10)}{10}\right]^2 = 0.46W$$

Assume $P_{CORE} = 0.2W$

$$Efficiency = \frac{I_{OUT}\ V_{OUT}}{I_{OUT}\ V_{OUT} + \Sigma P_{LOSS}}$$

$$\Sigma P_{LOSS} = 4 + 0.86 + 0.23 + 0.75 + 0.14 + 0.14 + 0.46 + 0.2 = 6.78W$$

$$Efficiency = \frac{(1.5)(12)}{(1.5)(12)+6.78} = 73\%$$

NEGATIVE BOOST CONVERTER

Note: *All equations in this section use the absolute value of V_{IN} and V_{OUT}.*

The LT1074 can be configured as a negative boost converter (Figure 18) by tying the ground pin to the negative output. This allows the regulator to operate from input voltages as low as 4.75V if the regulated output is at least 8V. R1 and R2 set the output voltage as in a conventional connection, with R1 selected from

$$R1 = \frac{V_{OUT} \bullet R2}{V_{REF}} - R2 \quad (65)$$

Boost converters have a "right half plane zero" in the forward part of the signal path and for this reason, L1 is kept to a low value to maximize the "zero" frequency. With larger values for L1, it becomes difficult to stabilize the regulator, especially at low input voltages. If V_{IN} >10V, L1 can be increased to 50µH.

There are two important characteristics of boost converters to keep in mind. First, the input voltage cannot exceed the output voltage, or D1 will simply pull the output unregulated high. Second, the output cannot be pulled below the input, or D1 will drag down the input supply. For this reason, boost converters are not normally considered short circuit protected unless some form of fusing is provided. Even with fuses, there is the possibility of damage to D1 if the input supply can deliver very large surge currents.

Boost converters require switch currents which can be much greater than output load current. Peak switch current is given by

$$I_{SW(PEAK)} = \frac{I_{OUT} \bullet V_{OUT}'}{V_{IN}'} + \frac{V_{IN}'(V_{OUT}' - V_{IN}')}{2L \bullet f \bullet V_{OUT}'} \quad (66)$$

For the circuit in Figure 18, with V_{IN} = 5V, (V_{IN}' ≈3V), V_{OUT}' ≈15.5V, with an output load of 0.5A;

$$I_{SW}(PEAK) = \frac{(0.5A)(15.5)}{3} + \frac{3(15.5-3)}{2(25\mu H)(10^5)(15.5)} = 3.07A \quad (67)$$

This formula can be rearranged to yield maximum load current for a given maximum switch current (I_M)

$$I_{OUT(MAX)} = \frac{I_M \bullet V_{IN}'}{V_{OUT}'} - \left(\frac{V_{IN}'}{V_{OUT}'}\right)^2 \frac{V_{OUT}' - V_{IN}'}{2L \bullet f} \quad (68)$$

For I_M = 5.5A, this equation yields 0.82A with V_{IN} = 4.5V, 1.8A with V_{IN} = 8V, and 3.1A for V_{IN} = 12V.

The explanation for switch current which is much higher than output current is that current is delivered to the

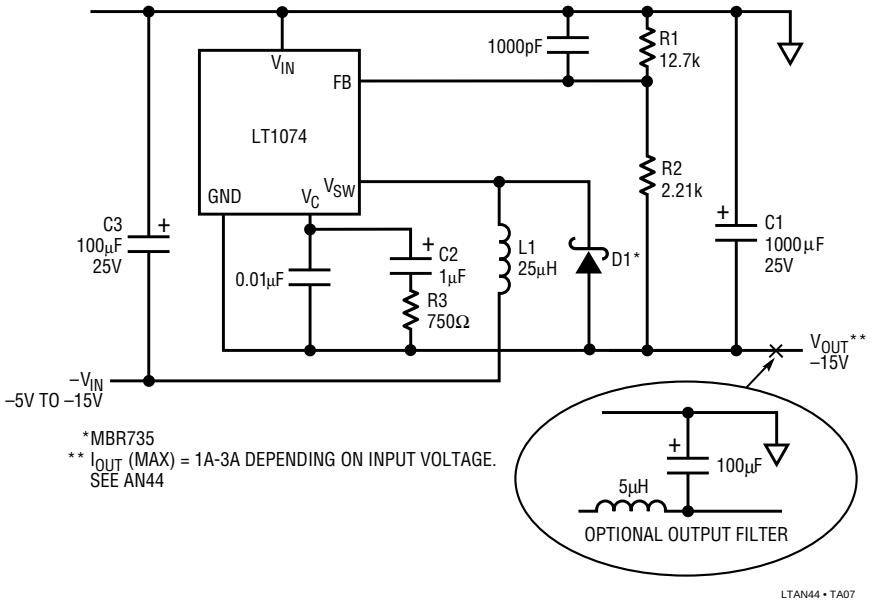

Figure 18. Negative Boost Converter

output only during switch "off" time. With low input voltages, the switch is "on" a high percentage of the total switching cycle and current is delivered to the output only a small percent of the time. Switch duty cycle is given by

$$DC = \frac{V_{OUT}' - V_{IN}'}{V_{OUT}'} \quad (69)$$

For V_{IN} = 5V, V_{OUT} = 15V, $V_{IN}' \approx 3V$, V_{OUT}' = 15.5V and;

$$DC = \frac{15.5 - 3}{15.5} = 81\% \quad (70)$$

Peak inductor current is equal to peak switch current. Average inductor current in continuous mode is equal to

$$I_{L(AVG)} = \frac{I_{OUT} \bullet V_{OUT}'}{V_{IN}'} \quad (71)$$

A 0.5A load requires 2.6A inductor current for V_{IN} = 5V.

Along with high switch currents, keep in mind that boost converters draw DC input currents *higher* than the output load current. Average input current to the converter is

$$I_{IN}(DC) \approx \frac{(I_{OUT})(V_{OUT}')}{V_{IN}'} \quad (72)$$

With I_{OUT} = 0.5A, and V_{IN} = 5V ($V_{IN}' \approx 3V$)

$$I_{IN}(DC) = \frac{(0.5)(15.5)}{3} = 2.6A \quad (73)$$

This formula does not take into account secondary loss terms such as the inductor, output capacitor, etc., so it is somewhat optimistic. Actual input current may be closer to 3A. *Be sure the input supply is capable of providing the required boost converter input current.*

Output Diode

The *average* current through D1 is equal to output current, but the peak pulse current is equal to peak switch current, which can be many times output current. D1 should be conservatively rated at 2 to 3 times output current.

Output Capacitor

The output capacitor of a boost converter has high RMS ripple current so this is often the deciding factor in the selection of C1. RMS ripple current is approximately

$$I_{RMS(C1)} \approx I_{OUT} \sqrt{\frac{V_{OUT}' - V_{IN}'}{V_{IN}'}} \quad (74)$$

For I_{OUT} = 0.5A, V_{IN} = 5V

$$I_{RMS} \approx 0.5 \sqrt{\frac{15.5 - 3}{3}} = 1A\ RMS \quad (75)$$

C1 must have a ripple current rating of 1A RMS. Its actual capacitance value is not critical. ESR of the capacitor will determine output ripple voltage.

Output Ripple

Boost converters tend to have high output ripple because of the high pulse currents delivered to the output capacitor.

$$Vp-p = ESR\left[\frac{I_{OUT}\bullet V_{OUT}'}{V_{IN}'}+\frac{V_{IN}'\left(V_{OUT}'-V_{IN}'\right)}{2L\bullet f\bullet V_{OUT}'}\right] \quad (76)$$

This formula assumes continuous mode operation, and it ignores the inductance of C1. In actual operation, C1 inductance will allow output "spikes" which should be removed with an output filter. The filter can be as simple as several inches of output wire or trace and a small solid tantalum capacitor if only the spikes need to be removed. A filter inductor is required if significant reduction of the fundamental is needed. See the "Output Filter" section.

For the circuit in Figure 18, with I_{OUT} = 0.5A, V_{IN} = 5V; and an output capacitor ESR of 0.05Ω

$$Vp-p = \quad (77)$$

$$0.05\left[\frac{(0.5)(15.5)}{3}+\frac{3\left(15.5-3\right)}{2\left(25\times10^{-6}\right)\left(10^{5}\right)(15.5)}\right]=153mV$$

Input Capacitor

Boost converters are more benign with respect to input current pulsing than buck or inverting converters. The input current is a DC level with a triangular ripple superimposed. RMS value of input current ripple is

$$I_{RMS(C3)}\approx\frac{V_{IN}'\left(V_{OUT}'-V_{IN}'\right)}{3L\bullet f\bullet V_{OUT}'} \quad (78)$$

Notice that ripple current is independent of load current assuming that load current is high enough to keep the converter in continuous mode. For the converter in Figure 18, with V_{IN} = 5V

$$I_{RMS}=\frac{3\left(15.5-3\right)}{3\left(25\times10^{-6}\right)\left(10^{5}\right)(15.5)}=0.32A\ RMS \quad (79)$$

C3 may be chosen on a ripple current basis to minimize size. Larger values will allow less conducted EMI back into the input supply.

INDUCTOR SELECTION

There are five main criteria in selecting an inductor for switching regulators. First, and most important, is the actual inductance value. If inductance is too low, output power will be restricted. Too much inductance results in large physical size and poor transient response. Second, the inductor must be capable of handling both RMS and peak currents which may be significantly higher than load current. Peak currents are limited by core saturation, with resultant loss of inductance. RMS currents are limited by heating effects in the winding. Also important is peak-to-peak current which determines heating effects in the core itself. Third, the physical size or weight of the inductor may be important in many applications. Fourth, power losses in the inductor can significantly affect regulator efficiency, especially at higher switching frequencies. Last, the price of inductors is very dependent on particular construction techniques and core materials, which impact overall size, efficiency, mountability, EMI, and form factor. There may be a significant cost penalty, for instance, if more expensive core materials are needed in "minimum size" applications.

The issues of price and size become particularly complicated at higher frequencies. High frequencies are used to reduce component size, and indeed, the inductance values required scale inversely with frequency. The problem with a scaled-down high frequency inductor is that total core loss increases slightly with frequency for constant ripple current, and this power is now dissipated in a smaller core, so temperature rise *and* efficiency can limit size reductions. Also, the smaller core has less room for wire, so wire losses may increase. The only solution to this problem is to find a better core material. Common low cost inductors use powdered iron cores, which are very low cost. These cores exhibit modest losses at 40kHz with a typical flux density of 300 gauss. At 100kHz, core losses can become unacceptably high at these flux densities. Reducing flux density requires a larger core, canceling part of the advantage gained in reducing inductance at the higher frequency.

Molypermalloy, "high flux," "Kool Mμ" (Magnetics, Inc.), and ferrite cores have considerably lower core loss, and can be used at 100kHz and above with higher flux density, but these cores are expensive. The basic lesson here is that attention to inductor selection is very important to minimize costs and achieve desired goals of size and efficiency.

A special equation has been developed in the following section which shows that for a given core material, total core loss is dependent almost totally on *frequency* and *inductance value*, not physical size or shape. The formula is arranged to solve for the inductance required to achieve a given core loss. It shows that, in a typical 100kHz buck converter, inductance has to be increased by a factor of three over the minimum required, if a low cost powdered iron core is used.

"Standard" switching regulator inductors are toroids. Although this shape is hardest to wind, it offers excellent utilization of the core, and more importantly, has low EMI fringing fields. Rod or drum shaped inductors have very high fringing fields and are not recommended except possibly for secondary output filters. Inductors made with "E-E" or "E-C" split cores are easy to wind on the separate bobbin, but tend to be much taller than toroids and more expensive. "Pot" cores reverse the position of winding and core—the core surrounds the winding. These cores offer the best EMI shielding, but tend to be bulky and more expensive. Also, temperature rise is higher because of the enclosed winding. Special low profile split cores (TDK "EPC," etc.) are now offered in a wide range of sizes. Although not as efficient as EC cores in terms of watts/volume, these cores are attractive for restricted height applications.

The best way to select an inductor is to first calculate the limitations on its minimum value. These limitations are imposed by a maximum allowed switch current, maximum allowable efficiency loss, and the necessity to operate in continuous versus discontinuous mode. (See discussion elsewhere of the consequences related to these two modes.) After the minimum value has been established, calculations are done to establish the operating conditions of the inductor; i.e., RMS current, peak-to-peak ripple current, and peak current. With this information, next select an "off the shelf" inductor which meets all the calculated requirements, or is reasonably close, Then ascertain the physical size and price of the selected inductor. If it fits in the allowed "budget" of space, height, and cost, you can then give some consideration to increasing the inductance to gain better efficiency, lower output ripple, lower input ripple, more output power, or some combination of these. If the selected inductor is physically too large, there are several possibilities; select a different core shape, a different core material, (which will require recalculating the minimum inductance based on efficiency loss), a higher operating frequency, or consider a custom wound inductor which is optimized for the application. Keep in mind when attempting to shoehorn an inductor into the smallest possible space that output overload conditions may cause currents to increase to the point of inductor failure. The major failure mode to consider is winding insulation failure due to high winding temperature. IC failure caused by loss of inductance due to core saturation or core temperature is not usually a problem because the LT1074 has pulse-by-pulse current limiting which is effective even with drastically lowered inductance.

The following equations solve for minimum inductance based on the assumption of limited peak switch current (I_M).

Minimum Inductance to Achieve a Required Output Power

$$\text{Buck Mode Discontinuous, } I_{OUT} \le \frac{I_M}{2}, \text{ Use Maximum } V_{IN} \qquad (80)$$

$$L_{MIN} = \frac{2 \bullet I_{OUT} \bullet V_{OUT} \left(V_{IN}' - V_{OUT} \right)}{f \left(I_M \right)^2 \left(V_{IN}' \right)}$$

$$\text{Buck Mode Continuous, } I_{OUT} \le I_M, \text{ Use Maximum } V_{IN} \qquad (81)$$

$$L_{MIN} = \frac{V_{OUT} \left(V_{IN}' - V_{OUT} \right)}{2 \bullet f \bullet V_{IN}' \left(I_M - I_{OUT} \right)}$$

$$\text{Inverting Mode Discontinuous, } I_{OUT} \le \frac{I_M \bullet V_{IN}'}{2 \left(V_{IN}' + V_{OUT}' \right)} \qquad (82)$$

$$L_{MIN} = \frac{2 \bullet I_{OUT} \bullet V_{OUT}'}{\left(I_M \right)^2 \bullet f}$$

$$\text{Inverting Mode Continuous, } I_{OUT} \le \frac{I_M \bullet V_{IN}'}{\left(V_{IN}' + V_{OUT}' \right)} \qquad (83)$$

$$L_{MIN} = \frac{\left(V_{IN}' \right)^2 \bullet V_{OUT}'}{2 \bullet f \left(V_{OUT}' + V_{IN}' \right)^2 \left(\frac{I_M \bullet V_{IN}'}{V_{IN}' + V_{OUT}'} - I_{OUT} \right)}$$

$$\text{Boost Mode Discontinuous, } I_{OUT} \le \frac{I_M \bullet V_{IN}'}{2 \bullet V_{OUT}'} \qquad (84)$$

$$L_{MIN} = \frac{2 \bullet I_{OUT} \left(V_{OUT}' - V_{IN}' \right)}{\left(I_M \right)^2 \bullet f}$$

$$\text{Boost Mode Continuous }, I_{OUT} \le \frac{I_M \bullet V_{IN}'}{V_{OUT}'} \quad (85)$$

$$L_{MIN} = \frac{\left(V_{IN}'\right)^2 \left(V_{OUT}' - V_{IN}'\right)}{2 \bullet f \left(V_{OUT}'\right)^2 \left(\frac{I_M \bullet V_{IN}'}{V_{OUT}'} - I_{OUT}\right)}$$

$$\text{Tapped Inductor Continuous }, I_{OUT} \le \frac{I_M \left(N+1\right)\left(V_{IN}'\right)}{V_{IN}' + N V_{OUT}'} \quad (86)$$

$$L_{MIN} = \frac{V_{IN} \bullet V_{OUT} \left(V_{IN} - V_{OUT}\right)\left(N+1\right)^2}{I_M \bullet 2f \bullet V_{IN} \left(N+1\right)\left(V_{IN} + N V_{OUT}\right) - I_{OUT} \left(V_{IN} + N V_{OUT}\right)^2 \left(2f\right)}$$

Minimum Inductance Required to Achieve a Desired Core Loss

Power loss in inductor core material is not intuitive at all. It is, to a first approximation, independent of the *size* of the core for a given inductance and operating frequency. Second, power loss *drops* as inductance increases, for constant frequency. Last, raising frequency with a given inductor will *decrease* core loss, even though manufacturer's curves show that core loss increases with frequency. These curves assume constant flux density, which is not true for a fixed inductance.

The general formula for core loss can be expressed as;

$$P_C = C \bullet B_{AC}^{\,p} \bullet f^{\,d} \bullet V_C \quad (87)$$

C, d, p = Constants (see Table 1)
B_{AC} = Peak AC Flux Density (1/2 peak-to-peak) (gauss)
f = Frequency
V_C = Core Volume (cm^3)

The exponent "p" falls in the range of 1.8-2.4 for powdered iron cores, ≈2.1 for molypermalloy, and 2.3-2.8 for ferrites. "d" is ≈1 for powdered iron and ≈1.3 for ferrite. A closed form expression can be generated which relates core loss to the basic requirements of a switching regulator; inductance, frequency, and input/output voltages. The general form is

$$\text{Continuous Mode } P_C = \frac{a \bullet b^{\,p}}{f^{\,p-d} \bullet L^{\,p/2}} \quad (88)$$

$$\text{Discontinuous Mode } P_C = a \bullet f^{\,d-1} \bullet e \quad (89)$$

a, d, p = Core Material Constants (see Table 1)
b, e = Constants Determined by Input and Output Voltages and Currents
L = Inductance

These formulas show that core material, inductance, and frequency are the only degrees of freedom to alter core loss in the continuous mode case. For discontinuous mode, even inductance disappears as a variable, leaving frequency and core material. Further, the constant "d" is close to unity for many core materials, yielding a discontinuous mode core loss independent of all user variables except core material!

The following specific formulas will allow calculation of the inductance to achieve a given core loss in continuous mode and will indicate actual core loss for the discontinuous mode.

When using these formulas, assume initially that the term $V_e^{\,p-2/p}$ can be ignored. It is close to unity for a relatively wide range of core volumes because the exponent (p–2)/2 is less than 0.1 for commonly used powdered iron and molypermalloy cores. After an inductor is chosen and V_e is known, the term $V_e^{\,p-2/p}$ can be calculated to double check its effect on the value for L_{MIN}, usually less than 20%.

$$\text{Continuous Mode} \quad (90)$$

$$L_{MIN}^{*} = \frac{a \bullet \mu_e \bullet V_L^2}{\left(P_C\right)^{2/p} \bullet f^{\left(2 - \frac{2d}{p}\right)} \bullet V_e^{\left(\frac{p-2}{p}\right)}}$$

$$\text{Buck Mode Discontinuous} \quad (91)$$

$$P_C = \frac{a \bullet \mu_e \left(0.4\pi\right) f^{\,d-1}}{10^{-8}} \left(V_L \bullet I_{OUT}\right)$$

*A strict derivation

a, d, p = Core loss constants. Use Table 1.
μ_e = Effective core permeability. For ungapped cores, use Table 1. For gapped cores, use manufacturer's specification, or calculate.
V_L = An equivalent "voltage," dependent on input voltage, output voltage, and topology. Use Table 2.
P_C = Total core loss in watts.
L = Inductance.
V_e = Effective core volume in cm^3.

Table 1. Core Constants

		C	a	d	p	μ	Loss at 100kHz, 500 Gauss (mW/cm3)
Micrometals							
Powdered Iron	# 8	4.30E-10	8.20E-05	1.13	2.41	35	617
	# 18	6.40E-10	1.20E-04	1.18	2.27	55	670
	# 26	7.00E-10	1.30E-04	1.36	2.03	75	1300
	# 52	9.10E-10	4.90E-04	1.26	2.11	75	890
Magnetics							
Kool Mμ	60	2.50E-11	3.20E-06	1.5	2	60	200
	75	2.50E-11	3.20E-06	1.5	2	75	200
	90	2.50E-11	3.20E-06	1.5	2	90	200
	125	2.50E-11	3.20E-06	1.5	2	125	200
Molypermalloy	– 60	7.00E-12	2.90E-05	1.41	2.24	60	87
	– 125	1.80E-11	1.60E-04	1.33	2.31	125	136
	– 200	3.20E-12	2.80E-05	1.58	2.29	200	390
	– 300	3.70E-12	2.10E-05	1.58	2.26	300	368
	– 550	4.30E-12	8.50E-05	1.59	2.36	550	890
High Flux	– 14	1.10E-10	6.50E-03	1.26	2.52	14	1330
	– 26	5.40E-11	4.90E-03	1.25	2.55	26	740
	– 60	2.60E-11	3.10E-03	1.23	2.56	60	290
	– 125	1.10E-11	2.10E-03	1.33	2.59	125	460
	– 160	3.70E-12	6.70E-04	1.41	2.56	160	1280
Ferrite	F	1.80E-14	1.20E-05	1.62	2.57	3000	20
	K	2.20E-18	5.90E-06	2	3.1	1500	5
	P	2.90E-17	4.20E-07	2.06	2.7	2500	11
	R	1.10E-16	4.80E-07	1.98	2.63	2300	11
Philips							
Ferrite	3C80	6.40E-12	7.30E-05	1.3	2.32	2000	37
	3C81	6.80E-14	1.50E-05	1.6	2.5	2700	38
	3C85	2.20E-14	8.70E-08	1.8	2.2	2000	18
	3F3	1.30E-16	9.80E-08	2	2.5	1800	7
TDK							
Ferrite	PC30	2.20E-14	1.70E-06	1.7	2.4	2500	21
	PC40	4.50E-14	1.10E-05	1.55	2.5	2300	14
Fair-Rite	77	1.70E-12	1.80E-05	1.5	2.3	1500	86

Table 2. Equivalent Inductor Voltage

TOPOLOGY	V_L
Buck Continuous	$V_{OUT}(V_{IN} - V_{OUT})/2V_{IN}$
Buck Discontinuous	
Inverting Continuous	$V_{IN}' \bullet V_{OUT}'/[2(V_{IN}' + V_{OUT}')]$
Inverting Discontinuous	
Boost Continuous	$V_{IN}'(V_{OUT}' - V_{IN}')/2V_{OUT}'$
Boost Discontinuous	
Tapped-inductor	$(V_{IN} - V_{OUT})(V_{OUT})(1+N)/2(V_{IN} + NV_{OUT})$

Example: Buck converter with V_{IN} = 20V-30V, V_{OUT} = 5V, I_{OUT} = 3A, f = 100kHz, maximum inductor loss = 0.8W.

3A is more than $I_M/2$, so continuous mode must be used. Maximum input voltage is used to calculate L_{MIN} from equation 81

$$L_{MIN} = \frac{5(30-5)}{2\left(10^5\right)(30)(5-3)} = 10.4\mu H \qquad (92)$$

Now calculate minimum inductance to achieve desired core loss. Assume 1/2 total inductor loss in winding and 1/2 loss in the core (P_C = 0.4 W). Try Micrometals #26 core material. V_L (from Table 2) = 5(30 – 5)/(2 • 30) = 2.08

$$L_{MIN} = \frac{\left(1.3 \times 10^{-4}\right)(75)(2.08)^2}{(0.4)^{0.985} \bullet \left(10^5\right)^{2-1.34}} = 52\mu H \qquad (93)$$

The inductance must be five times the minimum to achieve desired core loss. Let's assume that 52µH is too large for our space requirements and try a better core material, #52, which is only slightly more expensive.

$$L_{MIN} = \frac{\left(4.9 \times 10^{-4}\right)(75)(2.08)^2}{(0.4)^{\frac{2}{2.11}} \bullet \left(10^5\right)^{\frac{2-2(1.26)}{2.11}}} = 35\mu H \qquad (94)$$

To see if an off-the-shelf inductor is suitable, calculate inductor currents and V • t product using Table 3.

$$I_{RMS} = I_{OUT} = 3A \qquad (95)$$

$$I_P = 3 + \frac{5(30-5)}{2\left(35 \times 10^{-6}\right)\left(10^5\right)(30)} = 3.6A$$

$$V \bullet t = \frac{5(30-5)}{\left(10^5\right)(30)} = 42V \bullet \mu s$$

Table 3. Inductor Operating Conditions

	I_{AVG}	I_{PEAK}	Ip-p	V•µs
Buck Converter (Continuous)	I_O	$I_O + \frac{V_O(V_I - V_O)}{2 \bullet L \bullet f \bullet V_I}$	$\frac{V_O(V_I - V_O)}{L \bullet f \bullet V_I}$	$\frac{V_O(V_I - V_O) \bullet 10^6}{f \bullet V_I}$
Positive to Negative (Continuous)	$\frac{I_O(V_I + V_O)}{V_I}$	$\frac{I_O(V_O + V_I)}{V_I} + \frac{V_I \bullet V_O}{2 \bullet L \bullet f(V_I + V_O)}$	$\frac{V_I \bullet V_O}{L \bullet f(V_I + V_O)}$	$\frac{V_I \bullet V_O \bullet 10^6}{f(V_I + V_O)}$
Negative Boost (Continuous)	$\frac{I_O \bullet V_O}{V_I}$	$\frac{I_O \bullet V_O}{V_I} + \frac{V_I(V_O - V_I)}{2L \bullet f \bullet V_O}$	$\frac{V_I(V_O - V_I)}{L \bullet f \bullet V_O}$	$\frac{V_I(V_O - V_I) \bullet 10^6}{f \bullet V_O}$
Tapped-Inductor*	$\frac{I_O(N \bullet V_O + V_I)}{V_I(1+N)}, \frac{I_O(N \bullet V_O + V_I)}{V_I}$ *	$\frac{I_O(N \bullet V_O + V_I)}{V_I(1+N)} + \frac{(V_I - V_O)(1+N)(V_O)}{2L \bullet f(N \bullet V_O + V_I)}$ *	$\frac{(V_I - V_O)(1+N)(V_O)}{L \bullet f(N \bullet V_O + V_I)}$ *	$\frac{10^6(V_I - V_O)(1+N)(V_O)}{f(N \bullet V_O + V_I)}$
Buck Converter (Discontinuous)	$1/4\sqrt{\frac{(I_O)^3 \bullet V_O(V_I - V_O)}{f \bullet L \bullet V_I}}$	$\sqrt{\frac{2I_O \bullet V_O(V_I - V_O)}{L \bullet f \bullet V_I}}$		$10^6\sqrt{\frac{2 \bullet L \bullet I_O \bullet V_O(V_I - V_O)}{f \bullet V_I}}$
Positive to Negative (Discontinuous)	$1/4\sqrt{\frac{I_O^3(V_I + V_O)^2}{V_I \bullet f \bullet L}}$	$\sqrt{\frac{2I_O \bullet V_O}{f \bullet L}}$		$10^6\sqrt{\frac{2I_O \bullet V_O \bullet L}{f}}$
Negative Boost (Discontinuous)	$1/4\sqrt{\frac{I_O^3 \bullet V_O^2(V_O + V_I)}{V_I^2 \bullet L \bullet f}}$	$\sqrt{\frac{2I_O(V_O - V_I)}{L \bullet f}}$		$10^6\sqrt{\frac{2I_O \bullet L(V_O - V_I)}{L \bullet f}}$

* Values given for tapped-inductor I_{AVG} are average current through entire inductor during switch "on" time (first term), and average current through output section during switch "off" time (second term). To calculate heating, these currents must be multiplied by the appropriate winding resistance and factored by duty cycle.

I_{PEAK} is used to ensure the core does not saturate and should be used with the entire inductance.

Peak-to-peak current is used with the entire inductance to calculate core heating losses. It is the equivalent value if the inductor is not tapped.

This inductor must be at least 35µH, rated at 3A and ≥ 42V • µs @ 100kHz. It must not saturate at a peak current of 3.6A.

Example: Inverting mode with V_{IN} = 4.7-5.3V, V_{OUT} = –5V, I_{OUT} = 1A, f = 100kHz, maximum inductor loss = 0.3W. Let V_{IN}' = 2.7V, V_{OUT}' = 5.5V. Maximum output current for discontinuous mode (equation 82) is 0.82A, so use continuous mode.

$$L_{MIN} = \frac{(2.7)^2 (5.5)}{2 \times 10^5 (5.5 + 2.7)^2 \left(\frac{5 \bullet 2.7}{5.5 + 2.7} - 1\right)} = 4.6\mu H \quad (96)$$

Now calculate minimum inductance from core loss. Assume core loss is 1/2 of total inductor loss, (P_C = 0.15W).

$$V_L(\text{From Table 2}) = \frac{(2.7)(5.5)}{2(2.7 + 5.5)} = 0.905 \quad (97)$$

Assuming Micrometals type #26 material,

$$L_{MIN} = \frac{\left(1.3 \times 10^{-4}\right)(75)(0.905)^2}{(0.15)^{\frac{2}{2.03}} \bullet \left(10^5\right)^{2 - \frac{2.72}{2.03}}} = 26\mu H \quad (98)$$

This value is over five times the minimum of 4.6µH Perhaps a higher core loss is acceptable. Here's how to do a quick check. If we assume total efficiency is ≈60% (+ to – conversion with a 5V input is inefficient due to switch loss), then input power is equal to output power divided by 0.6 = 8.33W. If we double core loss from 0.15W to 0.3W, efficiency will be 5W/(8.33 + 0.15) = 59%. This is only a 1% drop in efficiency. A core loss of 0.3W allows inductance to drop to 12µH, assuming that the 12µH inductor will tolerate the core loss plus winding loss without overheating. Inductor currents are

$$I_{RMS}(\text{From Table 3}) = \frac{(1A)(2.7 + 5.5)}{2.7} = 3A \quad (99)$$

$$I_P = \frac{(1A)(2.7 + 5.5)}{2.7} + \frac{(2.7)(5.5)}{2\left(12 \times 10^{-6}\right)\left(10^5\right)(2.7 + 5.5)} = 3.8A$$

$$V \bullet t = \frac{(2.7)(5.5)}{\left(10^5\right)(2.7 + 5.5)} = 18\ V \bullet \mu s\ @\ 100kHz$$

MICROPOWER SHUTDOWN

The LT1074 will go into a micropower shutdown mode, with $I_{SUPPLY} \approx 150\mu A$, when the shutdown pin is held below 0.3V. This can be accomplished with an open collector TTL gate, a CMOS gate, or a discrete NPN or NMOS device, as shown in Figure 19.

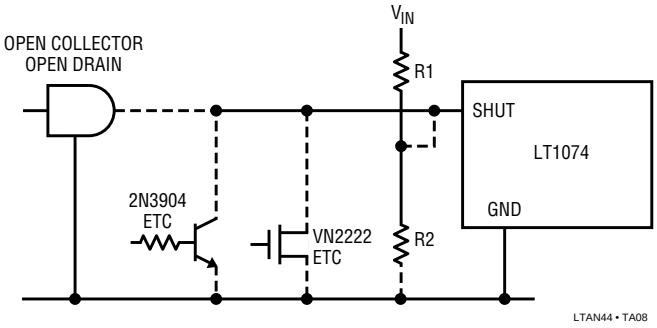

Figure 19. Shutdown

The basic requirement is that the pull down device can sink 50µA of current at a worst case threshold of 0.1V. This requirement is easily met with any open collector TTL gate (not Schottky clamped), a CMOS gate, or discrete device.

The sink requirements are more stringent if R1 and R2 are added for under voltage lockout. Sink capability must be 50µA + V_{IN}/R1 at the worst case threshold of 0.1V. The suggested value for R2 is 5kΩ to minimize the effect of shutdown pin bias current. This sets the current through R1 and R2 at ≈ 500µA at the undervoltage lockout point. At an input voltage of twice the lockout point, R1 current will be slightly over 1mA, so the pull down device must sink this current down to 0.1V. A VN2222 or equivalent is suggested for these conditions.

Start-Up Time Delay

Adding a capacitor to the shutdown pin will generate a delayed start-up. The internal current averages to about 25µA during the delay period, so delay time will be =(2.45V)/(C • 25µA), ±50%. If more accurate time out is required, R1 can be added to swamp out the effects of the internal current, but a larger capacitor is needed, and time out is dependent on input voltage.

Some thought must be given to reset of the timing capacitor. If a resistor to ground is used, it must be large enough to not drastically affect timing, so reset time is typically ten times longer than time delay. A diode to V_{IN}

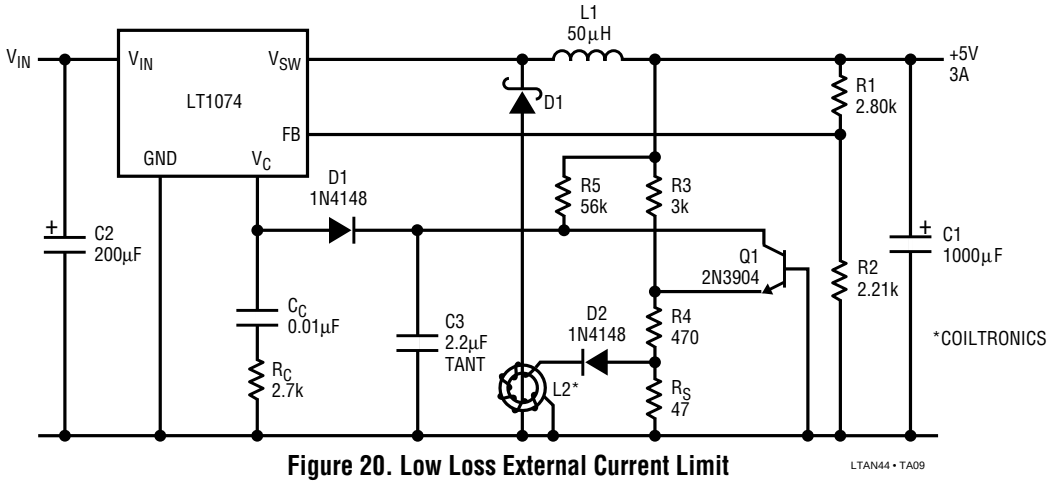

Figure 20. Low Loss External Current Limit

resets quickly, but if V_{IN} does not drop to near zero, time delay will be shortened when power is recycled immediately.

5-PIN CURRENT LIMIT

Sometimes it may be desirable to current limit the 5-pin version of the LT1074. This is particularly helpful where maximum load current is significantly less than the 6.5A internal current limit, and the inductor and/or catch diode are minimum size to save space. Short circuit conditions put maximum stress on these components.

The circuit in Figure 20 uses a small toroidal inductor slipped over one lead of the catch diode to sense diode current. Diode current during switch "off" time is almost directly proportional to output current, and L2 can generate an accurate limit signal without affecting regulator efficiency. Total power lost in the limit circuitry is less than 0.1W.

L2 has 100 turns. It therefore delivers 1/100 times diode current to R_S when D1 conducts. The voltage across R_S required to current limit the LT1074 is equal to the voltage across R4 plus the forward biased emitter base voltage Q1 (≈600mV@25°C). The voltage across R4 is set at 1.1V by R3, which is connected to the output. Current limit is set by selecting R_S;

$$R_S = \frac{R_4 I_X + V_{BE}}{\frac{I_{LIM}}{100} - I_X} \qquad (100)$$

$$I_X = \frac{V_{OUT} + V_{BE}}{R_3} + 0.4mA$$

V_{BE} = Forward biased emitter base voltage of Q1 @ I_C = 500µA (≈600mV).

N = Turns on L2.

I_{LIM} = Desired output current limit. I_{LIM} should be set ≈1.25 times maximum load current to allow for variations in V_{BE} and component tolerances.

The circuit in Figure 20 is intended to supply 3A maximum load current, so I_{LIM} was set at 3.75A. Nominal V_{IN} is 25V, giving

$$I_X = \frac{5 + 0.6}{3000} + 0.4 \times 10^{-3} = 2.27 \times 10^{-3} \qquad (101)$$

$$R_S = \frac{(470)\left(2.27 \times 10^{-3}\right) + 0.6}{3.75/100 - 2.27 \times 10^{-3}} = 47\Omega$$

This circuit has "foldback" current limit, meaning that short circuit current is lower than the current limit at full output voltage. This is the result of using the output voltage to generate part of the current limit trip level. Short circuit current will be approximately 45% of peak current limit, minimizing temperature rise in D1.

R5, C3, and D3 allow separate frequency compensation of the current limit loop. D3 is reversed biased during normal operation. For higher output voltages, scale R3 and R5 to provide approximately the same currents.

SOFT START

Soft start is a means for ramping switch currents during the turn on of a switching regulator. The reasons for doing this include surge protection for the input supply, protection of switching elements, and prevention of output

overshoot. Linear Technology switching regulators have built-in switch protection that eliminates concern over device failure, but some input supplies may not tolerate the inrush current of a switching regulator. The problem occurs with current limited input supplies or those with relatively high source resistance. These supplies can "latch" in a low voltage state where the current drawn by the switching regulator in much higher than the normal input current. This is shown by the general formula for switching regulator input current and input resistance;

$$I_{IN} = \frac{(V_{OUT})(I_{OUT})}{(V_{IN})(E)} = \frac{P_{OUT}}{(V_{IN})(E)} \quad (102)$$

$$R_{IN} = \frac{-(V_{IN})^2(E)}{(V_{OUT})(I_{OUT})} = \frac{-(V_{IN})^2(E)}{P_{OUT}} \text{ (note negative sign)}$$

E = Efficiency (≈ 0.7-0.9)

These formulas show that input current is proportional to the reciprocal of input voltage, so that if input voltage drops by 3:1, input current increases by 3:1. An input supply which rises slowly will "see" a much heavier current load during its low voltage state. This can activate current limit in the input supply and "latch" it permanently in a low voltage condition. By instituting a soft start in the switching regulator which is *slower* than the input supply rise time, regulator input current is held low until the input supply has a chance to reach full voltage.

The formula for regulator input resistance shows that it is negative and decreases as the square of input voltage. The maximum allowed positive source resistance to avoid latch-up is given by;

$$R_{SOURCE(MAX)} = \frac{(V_{IN})^2(E)}{4(V_{OUT})(I_{OUT})} \quad (103)$$

The formula shows that a +12V to –12V converter with 80% efficiency and 1A load must have a source resistance less than 2.4Ω. This may sound like much ado about nothing, because an input supply designed to deliver 1A would not normally have such a high source resistance, but a sudden output load surge or a dip in the source voltage might trigger a permanent overload condition. Low V_{IN} and high output load require lower source resistance.

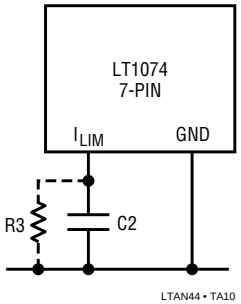

Figure 21. Soft Start Using I_{LIM} Pin

In Figure 21, C2 generates a soft start of switching current by forcing the I_{LIM} pin to ramp up slowly. Current out of the I_{LIM} pin is ≈ 300μA, so the time for the LT1074 to reach full switch current (V_{LIM} ≈ 5V) is ≈ (1.6×10^4)(C). To ensure low switch current until V_{IN} has reached full value, an approximate value for C2 is

$$C2 \approx \left(10^{-4}\right)(T) \quad (104)$$

T = Time for input voltage to rise to within 10% of final value.

C2 must be reset to zero volts whenever the input voltage goes low. An internal reset is provided when the shutdown pin is used to generate undervoltage lockout. The "undervoltage" state resets C2. If lockout is not used, R3 should be added to reset C2. For full current limit, R3 should be 30kΩ. If reduced current limit is desired, R3's value is set by desired current limit. See the "Current Limit" section.

If the only reason for adding soft start is to prevent input supply latchup, a better alternative may be undervoltage lockout (UVLO). This prevents the regulator from drawing input current until the input voltage reaches a preset voltage. The advantage of UVLO is that it is a true DC function and cannot be defeated by a slow rising input, short reset times, momentary output shorts, etc.

OUTPUT FILTERS

When converter output ripple voltage must be less than ≈2% of output voltage, it is usually better to add an output filter (Figure 22) than to simply "brute force" the ripple by using very large output capacitors. The output filter consists of a small inductor (≈2μH-10μH) and a second output capacitor, usually 50μF-200μF. The inductor must

be rated at full load current. Its core material is not important (core loss is negligible) except that core material will determine the size and shape of the inductor. Series resistance should be low enough to avoid unwanted efficiency loss. This can be estimated from;

$$R_L = \frac{(\Delta E)(V_{OUT})}{(I_{OUT})(E)^2} \quad (105)$$

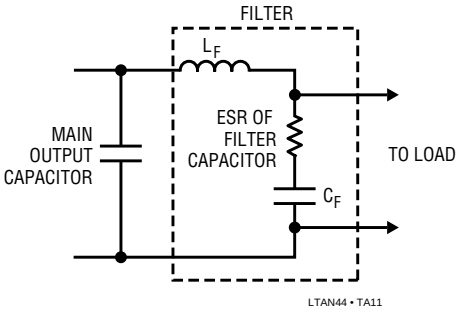

Figure 22. Output Filter

"E" is overall efficiency and ΔE is the loss in efficiency allocated to the filter. Both are expressed as a ratio, i.e., 2% $\Delta E = 0.02$, and 80% $E = 0.8$.

To obtain the required component values for the filter, one must assume a value for inductance or capacitor ESR, then calculate the remaining value. Actual capacitance in microfarads is of secondary importance because it is assumed that the capacitor will be basically resistive at ripple frequencies. One consideration on filter capacitor value is the load transient response of the converter. A small output filter capacitor (high ESR) will allow the output to "bounce" excessively if large amplitude load transients occur. When these load transients are expected, the size of the output filter capacitor must be increased to meet transient requirements rather than just ripple limits. In this situation, the main output capacitor can be reduced to simply meet ripple current requirements. The complete design should be checked for transient response with full expected load change.

If the capacitor is selected first, the inductor value can be found from ripple attenuation requirements.

Buck converter with triangular ripple into filter

$$L_f = \frac{(ESR)(ATTN)}{8f} \quad (106)$$

All other converters with essentially rectangular ripple into filter

$$L_f = \frac{(ESR)(ATTN)(DC)(1-DC)}{f} \quad (107)$$

ESR = Filter capacitor series resistance.
ATTN = Ripple attenuation required, as a ratio of peak-to-peak ripple IN to peak-to-peak ripple OUT.
DC = Duty cycle of converter. (If unknown, use worst case of 0.5).

Example: A 100kHz buck converter with 150mVp-p ripple which must be reduced to 20mV. ATTN = 150/20 = 7.5. Assume a filter capacitor with ESR = 0.3Ω

$$L = \frac{(0.3)(7.5)}{8\left(10^5\right)} = 2.8\mu H \quad (108)$$

Example: A 100kHz positive to negative converter with output ripple of 250mVp-p which must be reduced to 30mV. Assume duty cycle has been calculated at 30% = 0.3, and ESR of filter capacitor is 0.2Ω

$$L = \frac{(0.2)(250/30)(0.3)(1-0.3)}{10^5} = 3.5\mu H \quad (109)$$

If the inductor is known, the equations can be rearranged to solve for capacitor ESR.

Buck Converter; (110)

$$ESR = \frac{8f(L)}{ATTN}$$

Square Wave Ripple In;

$$ESR = \frac{f \bullet L}{(ATTN)(DC)(1-DC)}$$

The output filter will affect load regulation if it is "outside" the regulator feedback loop. Series resistance of the filter inductor will add directly to the closed loop output resistance of the converter. This closed loop resistance is typically in the range of 0.002Ω- 0.01Ω, so a filter inductor resistance of 0.02Ω may represent a significant loss in load regulation. One solution is to move the filter "inside" the feedback loop by moving the sense points to the output of the filter. This should be avoided if possible because the

added phase shift of the filter can cause difficulties in stabilizing the converter. Buck converters will tolerate an output filter inside the feedback loop by simply reducing the loop unity gain frequency. Positive to negative converters and boost converters have a "right half plane zero" which makes them very sensitive to additional phase shift. To avoid stability problems, one should first determine if the load regulation degradation caused by a filter is really a problem. Most digital and analog "chips" in use today tolerate modest changes in supply voltage with little or no effect on performance.

When the sense resistor is tied to the output of the filter, a "fix" for stability problems is to connect a capacitor from the input of the filter to a tap on the feedback divider as shown in Figure 23. This acts as a "feedforward" path around the filter. The minimum size of C_X will be determined by the filter response, but should be in the range of 0.1μF-1μF.

C_X could theoretically be connected directly to the FB pin, but this should be done only if the peak-to-peak ripple on the main output capacitor is less than 75mVp-p.

A word about "measured" filter output ripple. The true ripple voltage should contain only the fundamental of the switching frequency because higher harmonics and "spikes" are very heavily attenuated. If the ripple as measured on an oscilloscope is abnormally high or contains high frequencies, the measurement technique is probably at fault. See the "Oscilloscope Techniques" section.

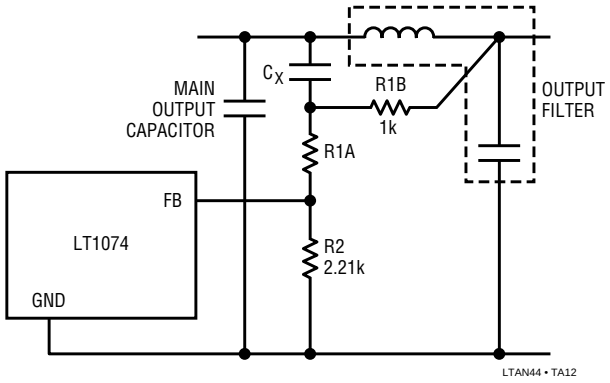

Figure 23. Feedforward when Output Filter is Inside Feedback Loop

INPUT FILTERS

Most switching regulators draw power from the input supply with rectangular or triangular current pulses. (The exception is a boost converter where the inductor acts as a filter for input current). These current pulses are absorbed primarily by the input bypass capacitor which is located right at the regulator input. Significant ripple current can still flow in the input lines, however, if the impedance of the source, including the inductance of supply lines, is low. This ripple current may cause unwanted ripple voltage on the input supply or may cause EMI in the form of magnetic radiation from supply lines. In these cases, an input filter may be required. The filter consists of an inductor in series with the input supply combined with the input capacitor of the converter, as shown in Figure 24.

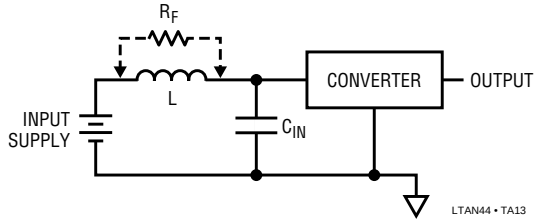

Figure 24. Input Filter

To calculate a value for L requires knowledge of what ripple current is allowed in the supply line. This is normally an unknown parameter, so much hand waving may go on in search of a value. Assuming that a value *has* been arrived at, L is found from;

$$L = \frac{ESR\left(DC\right)\left(1-DC\right)}{f\left(\frac{I_{SUP}}{I_{CON}} - \frac{ESR}{Rf}\right)} \qquad (111)$$

ESR = Effective series resistance of input capacitor.

DC = Converter duty cycle. If unknown, use 0.5 as worst case.

I_{CON} = Peak-to-peak ripple current drawn by the converter, assuming continuous mode. For buck converters, $I_{CON} \approx I_{OUT}$. Positive to negative converters have $I_{CON} = I_{OUT}\ (V_{OUT}' + V_{IN}')/V_{IN}'$. Tapped-inductor $I_{CON} = I_{OUT}\ (N \bullet V_{OUT}' + V_{IN}')/[V_{IN}'(1+N)]$.

I_{SUP} = Peak-to-peak ripple allowed in supply lines.

R_f = "Damping" resistor which may be required to prevent instabilities in the converter.

Example: A 100kHz buck converter with V_{OUT} = 5V, I_{OUT} = 4A, V_{IN} = 20V, (DC = 0.25). Input capacitor ESR is 0.05Ω. It is desired to reduce supply line ripple current to 100mA(p-p). Assume R_f is not needed (= ∞).

$$L = \frac{(0.05)(0.25)(1-0.25)}{10^5\left(\frac{0.1}{4}-0\right)} = 3.75\mu H \qquad (112)$$

For further details on input filters, including the possible need for a damping resistor (R_f), see the "Input Filters" section in Application Note 19.

The current rating of the input inductor must be a minimum of;

$$I_L = \frac{(V_{OUT})(I_{OUT})}{(V_{IN})(E)} \text{ Amps} \qquad (113)$$

$$(\text{Use Minimum } V_{IN})$$

For this example;

$$I_L = \frac{(5)(4)}{(20)(E \approx 0.8)} = 1.25A$$

Efficiency or overload considerations may dictate an inductor with higher current rating to minimize copper losses. Core losses will usually be negligible.

OSCILLOSCOPE TECHNIQUES

Switching regulators are a perfect test bed for poor oscilloscope techniques. A "scope" can lie in many ways and they all show up in a switching regulator because of the combination of fast and slow signals, coupled with both large and very small amplitudes. The following Rogue's Gallery will hopefully help the reader avoid many hours of frustration (and eliminate some embarrassing phone calls to the author).

Ground Loops

Good safety practice requires most instruments to have their "ground" system tied to a "third" (green) wire in the power cord. This unfortunately results in current flow through oscilloscope probe ground leads (shield) when other instruments source or sink current to the device under test. Figure 25 details this effect.

A generator is driving a 5V signal into 50Ω on the breadboard, resulting in a 100mA current. The return path for this current divides between the ground from the signal generator (typically the shield on a BNC cable) and the secondary ground "loop" created by the oscilloscope probe ground clip (shield), and the two "third wire" connections on the signal generator and oscilloscope. In

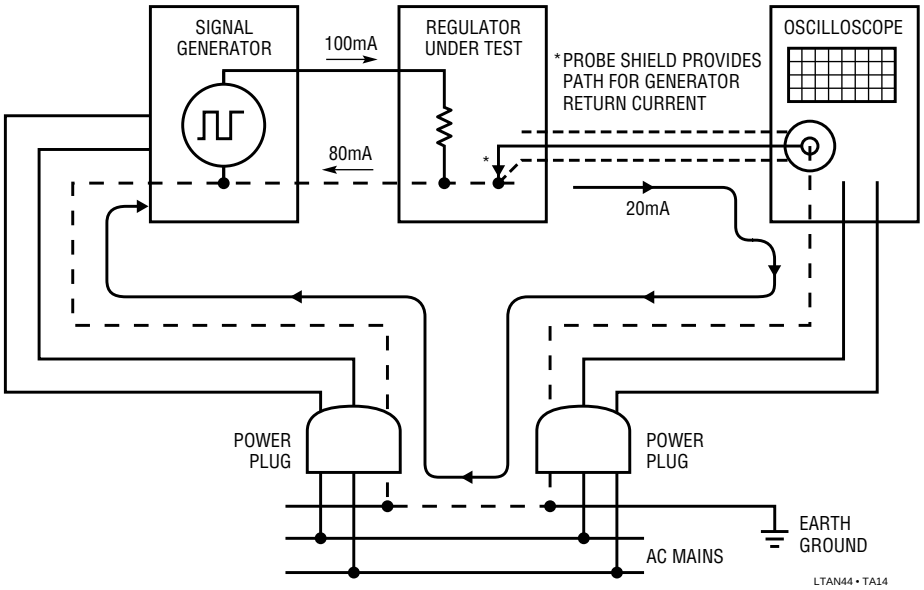

Figure 25. Ground Loop Errors

this case, it was assumed that 20mA flows in the parasitic ground loop. If the oscilloscope ground lead has a resistance of 0.2Ω, the screen will show a 4mV "bogus" signal. The problem gets much worse for higher currents, and fast signal edges where the inductance of the scope probe shield is important.

DC ground loops can be eliminated by disconnecting the third wire on the oscilloscope (its called a cheater plug, and my lawyers will *not* let me recommend it!) or by the use of an isolation transformer in the oscilloscope power connection.

Another source of circulating current in the probe shield wire is a second connection between a signal source and the scope. A typical example is a trigger signal connection between the generator trigger output and the scope external trigger input. This is most often a BNC cable *with its own grounded shield connection.* This forms a second path for signal ground return current, with the scope probe shield completing the path. My solution is to use a BNC cable which has had its shield intentionally broken. The trigger signal may be less than perfect, but the scope will not care. Mark the cable to prevent normal use!

Rule #1: *Before making any low level measurements, touch the scope probe "tip" to the probe ground clip with the clip connected to the desired breadboard ground.* The "scope" should indicate flatline. Any signal displayed is a ground loop lie.

Miscompensated Scope Probe

10X scope probes must be "compensated" to adjust AC attenuation so it precisely matches the 10:1 DC attenuation of the probe. If this is not done correctly, low frequency signals will be distorted and high frequency signals will have the wrong amplitude. In switching regulator applications, a "miscompensated" probe may show "impossible" waveforms. A typical example is the switching node of an LT1074 buck converter. This node swings positive to a level 1.5V-2V *below* the input voltage, and negative to one diode drop below ground. A 10X probe with too little AC attenuation could show the node swinging *above* the supply, and so far negative that the diode forward voltage appears to be many volts instead of the expected 0.5V. Remember that at these frequencies (100kHz), the wave *shape* looks right because the probe acts purely capacitive, so the wrong amplitude may not be immediately obvious.

Rule #2: Check 10X scope probe compensation *before* being embarrassed by a savvy tech.

Ground "Clip" Pickup

Oscilloscope probes are most often used with a short ground "lead" with an alligator clip on the end. This ground wire is a remarkably good antenna. It picks up local magnetic fields and displays them in full color on the oscilloscope screen. Switching regulators generate lots of magnetic fields. Switch wires, diodes, capacitor and inductor leads, even "DC" supply lines can radiate significant magnetic fields because of the high currents and fast rise/fall times encountered. The test for ground clip problems is to touch the probe tip to the alligator clip, with the clip connected to the regulator ground point. Any trace seen on the screen is caused either by circulating currents in a ground loop, or by antenna action of the ground clip.

The fix for ground clip "pickup" is to throw the clip wire away and replace it with a special soldered-in probe terminator which can be obtained from the probe manufacturer. The plastic probe tip cover is pulled off to reveal the naked coaxial metal tube shield which extends to the small needle tip. This tube slips into the terminator to complete the ground connection. This technique will allow you to measure millivolts of output ripple on a switching regulator even in the presence of high magnetic fields.

Rule #3: *Don't make any low level measurements on a switching regulator using a standard ground clip lead.* If an official terminator is not available, solder a solid bare hookup wire to the desired ground point and wrap it around the exposed probe coaxial tube with absolute minimum distance between the ground point and the tube. Position the ground point so that the probe needle tip can touch the desired test point.

Wires Are Not Shorts

A common error in probing switching regulators is to assume that the voltage anywhere on a wire path is the same. A typical example is the ripple voltage measured at the output of a switching regulator. If the regulator delivers square waves of current to the output capacitor, a positive

to negative converter for instance, the current rise/fall time will be approximately 10^8A/sec. This dI/dt will generate *≈2V per inch* "spikes" in the lead inductance of the output capacitor. The output (load) traces of the regulator should connect directly to the through-hole points where the radial-lead output capacitor leads are soldered in. The oscilloscope probe tip terminator (no ground clips, please) must be tied in directly at the base of the capacitor also.

The 2V/in. number can cause significant measurement errors even at high level points. When the input voltage to a switching regulator is measured across the input bypass capacitor, the spikes seen may be only a few tenths of a volt. If that capacitor is several inches away from the LT1074 though, the spikes "seen" by the regulator may be many volts. This can cause problems, especially at a low input voltage. Probing the "wrong" point on the input wire might mask these spikes.

Rule #4: If you want to know what the voltage is *on a high AC current signal path, define exactly which component voltage you are measuring* and connect the probe terminator directly across that component. As an example, if your circuit has a snubber to protect against switch overvoltage, connect the probe terminator *directly* to the IC switch terminals. Inductance in the leads connecting the switch to the snubber may cause the switch voltage to be many volts higher than the snubber voltage.

EMI SUPPRESSION

Electromagnetic interference (EMI) is a fact of life with switching regulators. Consideration of its effects should occur early in the design so that the electrical, physical, and monetary implications of any required filtering or shielding are understood and accounted for. EMI takes two basic forms; "conducted," which travels down input and output wiring, and "radiated," which takes the form of electric and magnetic fields.

Conducted EMI occurs on input lines because switching regulators draw current from their input supply in pulses, either square wave, or triangular, or a combination of these. This pulsating current can create bothersome ripple voltage on the input supply and it can radiate from input lines to surrounding lines or circuitry.

Conducted EMI on the output of a switching regulator is usually limited to the voltage ripple on the output nodes. Ripple frequencies from buck regulators consist almost entirely of the fundamental switching frequency, whereas boost and inverting regulator outputs contain much higher frequency harmonics if no additional filtering is used.

Electric fields are generated by the fast rise and fall times of the switch node in the regulator. EMI from this source is usually of secondary concern and can be minimized by keeping all connections to this node as short as possible and by keeping this node "internal" to the switching regulator circuitry so that surrounding components act as shields.

The primary source of electric field problems *within* the regulator itself is coupling between the switching node and the feedback pin. The switching node has a typical slew rate of 0.8×10^9V/sec., and the impedance at the feedback pin is typically 1.2kΩ. Just 1PF coupling between these pins will generate 1V spikes at the feedback pin, creating erratic switching waveforms. Avoid long traces on the feedback pin by locating the feedback resistors immediately adjacent to the pin. When coupling to switching node cannot be avoided, a 1000pF capacitor from the LT1074 ground pin to the feedback pin will prevent most pickup problems.

Magnetic fields are more troublesome because they are generated by a variety of components, including the input and output capacitors, catch diode, snubber networks, the inductor, the LT1074 itself, and many of the wires connecting these components. While these fields do not usually cause regulator problems, they can create problems for surrounding circuitry, especially with low level signals such as disc drives, data acquisition, communication, or video processing. The following guidelines will be helpful in minimizing magnetic field problems.

1. Use inductors or transformers with good EMI characteristics such as toroids or pot cores. The worst offenders from an EMI standpoint are "rod" inductors. Think of them as cannon barrels firing magnetic flux lines in every direction. Their only application in switchers should be in the output filter where ripple current is very low.

2. Route all traces carrying high ripple current over a ground plane to minimize radiated fields. This includes the catch diode leads, input and output capacitor leads, snubber leads, inductor leads, LT1074 input and switch pin leads, and input power leads. Keep these leads short and the components close to the ground plane.

3. Keep sensitive low level circuitry as far away as possible, and use field-cancelling tricks such as twisted-pair differential lines.

4. In critical applications, add a "spike killer" bead on the catch diode to suppress high harmonics. These beads will prevent very high dI/dt signals, but will also make the diode appear to turn "on" slowly. This can create higher transient switch voltages at switch turn-off, so switch waveforms should be checked carefully.

5. Add an input filter if radiation from input lines could be a problem. Just a few μH in the input line will allow the regulator input capacitor to swallow nearly all the ripple current created at the regulator input.

TROUBLESHOOTING HINTS

Low Efficiency

The major contributors here are switch and diode loss. These are readily calculable. If efficiency is abnormally low after factoring in these effects, zero in on the inductor. Core or copper loss may be the problem. Remember that inductor current may be much higher than output current in some topologies. A very handy substitution tool is a 500μH inductor wound with heavy wire on a large molypermalloy core. 100μH and 200μH taps are helpful. This inductor can be substituted for suspect units when inductor losses are suspected. If you read this App Note, you will know that a large core is used not to reduce core loss, but to allow enough room for large wire that eliminates copper loss.

If inductor losses are not the problem, check all the nickel and dime effects such as quiescent current and capacitor loss to see if the sum is no longer negligible.

Alternating Switch Timing

Switch "on" time may alternate from cycle to cycle if excess switching frequency ripple appears on the V_C pin. This can occur naturally because of high ESR in the output capacitor or because of pickup on the FB pin or the V_C pin. A simple check is to put a 3000pF capacitor from V_C pin to the ground pin close to the IC. If the erratic switching improves or is cured, excess V_C pin ripple is the problem. Isolate it by connecting the capacitor from FB to ground pin. If this also makes the problem disappear, V_C pin pickup is eliminated, and FB pickup is the likely culprit. The feedback resistors should be located close to the IC so that connections to the FB pin are short and routed away from switching nodes. A 500pF capacitor from FB to ground pin will usually be sufficient if pickup cannot be eliminated. Occasionally, excess output ripple is the problem. This can be checked by paralleling the output capacitor with a second unit. A 1000pF-3000pF capacitor on V_C can often be used to stop erratic switching caused by high output ripple, but be sure the ripple current rating of the output capacitor is adequate!

Input Supply Won't Come Up

Switching regulators have negative input resistance at DC. Therefore, they draw high current at low V_{IN}. This can latch input supplies low. See "Soft Start" section for details.

Switching Frequency is Low in Current Limit

This is normal. See "Frequency Shifting at the Feedback Pin" in the Pin Description section.

IC Blows Up!

Like the LT1070 before it, the only thing that can destroy the LT1074 or LT1076 is excess switch voltage. (I am ignoring obvious stuff like voltage reversal or wiring errors).

Start-up surges can sometimes cause momentary large switch voltages, so check voltages carefully with an oscilloscope. Read the section on oscilloscope techniques.

IC Runs Hot

A common mistake is to assume that heat sinks are no longer needed with a switching design. This is often true for small load currents, but as load current climbs above 1A, switch loss may increase to the point where a heat sink is needed. A TO-220 package has a thermal resistance of 50°C/W with no heat sink. A 5V, 3A output (15W) with 10% switch loss, will dissipate over 1.5W in the IC. This means a 75°C temperature rise, or 100°C case temperature at room ambient. This is normally referred to as hot! A small heat sink solves the problem. Simply soldering the TO-220 tab to an enlarged copper pad on the PC board will reduce thermal resistance to ≈25°C/W.

High Output Ripple or Noise Spikes

First read "Oscilloscope Techniques" section to avoid possible embarrassment, then check ESR of the output capacitor. Remember that fast (<100ns) spikes will be greatly attenuated by parasitic supply line inductance and load capacitance even if supply lines are only a few inches long.

Poor Load or Line Regulation

Check in this order:

1. Secondary output filter DC resistance if it is outside the loop.
2. Ground loop error in oscilloscope.
3. Improper connection of output divider resistors to current carrying lines.
4. Excess output ripple. The LT1074 can peak detect ripple voltages on the FB pin if they exceed 50mVp-p.

See "Reference Shift with Ripple Voltage" graph in Typical Performance Characteristics section.

500kHz-5MHz Oscillations, Especially at Light Load

This is discontinuous mode ringing and is quite normal and harmless. See buck converter waveform description for more details.

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