SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

DESIGNING WITH THE L296 MONOLITHIC POWER SWITCHING REGULATOR

A cost-effective replacement for costly hybrids, the L296 Power Switching Regulator delivers 4A at an output voltage of 5.1V to 40V and includes many popular supply features. This comprehensive application guide explains how the device operates and how it is used. Typical application circuits are also presented.

The SGS THOMSON L296 is the first monolithic switching regulator in plastic package which includes the power section. Moreover, the circuit includes all the functions which make it specially suited for microprocessor supply.

Before the introduction of L296, which realizes the step down configuration, this function was implemented with discrete power components driven be integrated PWM regulator circuits (giving a maximum output current of 300 to 400mA) or with hybrid circuits. Both of these solutions are characterized by a low efficiency of the power transistor. For this reason it is generally necessary to operate at frequencies in the 20kHz to 40kHz range. Of the two alternatives discrete solutions are usually less expensive because they do not include as many functions as the L296.

With the new L296 regulator the driving problem of the power control stage has been eliminated. Besides a higher overall efficiency, it is therefore also possible to operate directly at frequencies as high as 100kHz. At 200kHz the device still operates (further reducing the cost of the L and C external components) when a reduction of a few percent in efficiency is acceptable.

The device delivers a maximum current of 4 A to the load, at an output voltage adjustable from 5.1 to 40V ; the maximum operating input voltage is 46V. The high voltage and the high current capabilities of the device are a result of the special technology used and the special care taken in designing the power transistor. Essential requirements for a good power transistor are high gain and high current levels, low saturation voltage and good second breakdown robustness. To achieve high gain at high current levels, the power transistor has to be designed to maximize the emitter's perimeter/area ratio.

In the L296 power transistor, realized with a high voltage (50V) process, current densities in the magnitude order of 10mA/Mil^2 are achieved.

In its most complete configuration, in which all the available functions are being used, a significant reduction of the external component count is achieved compared with discrete component solution.

The L296 is mounted in a MULTIWATT® plastic package with 15 pins, minimizing the cost per watt and allowing a low thermal resistance of 3°C/W between junction and package and of 35°C/W between junction and ambient. This thermal resistance (inclucing the contact resistance) is comparable to that of the more costly metal TO-3 packages.

THE STEP-DOWN CONFIGURATION

Fig. 1 shows the simplified block diagram of the circuit realizing the step-down configuration. This circuit operates as follows : Q1 acts as a switch at the frequency f and the ON and OFF times are suitably controlled by the pulse width modulator circuit. When Q1 is saturated, energy is absorbed from the input which is transferred to the output through L. The emitter voltage of Q1, V_E, is Vi-Vsat when Q is ON and $-V_F$ (with V_F the forward voltage across the D diode as indicated) when Q1 is OFF. During this second phase the current circulates again through L and D. Consequently a rectangular shaped voltage appears on the emitter of Q1 and this is then filtered by the L-C-D network and converted into a continuous mean value across the capacitor C and therefore across the load. The current through L consists of a continuous component, I_{LOAD}, and a triangular-shaped component super-imposed on it, ΔI_L, due to the voltage across L.

Figure 1 : The Basic Step-down Switching Regulator Configuration.

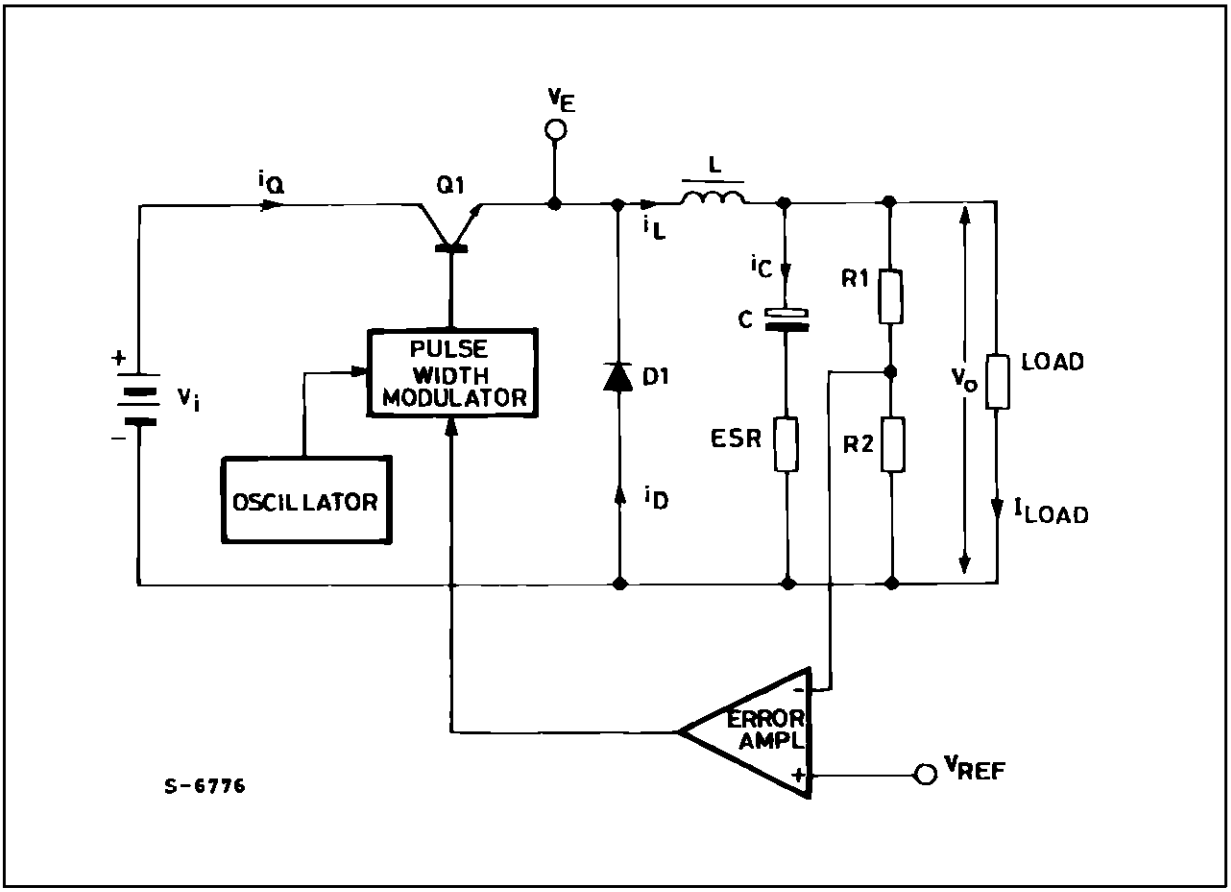


Figure 2 : Principal Circuit Waveforms of the figure 1 Circuit.

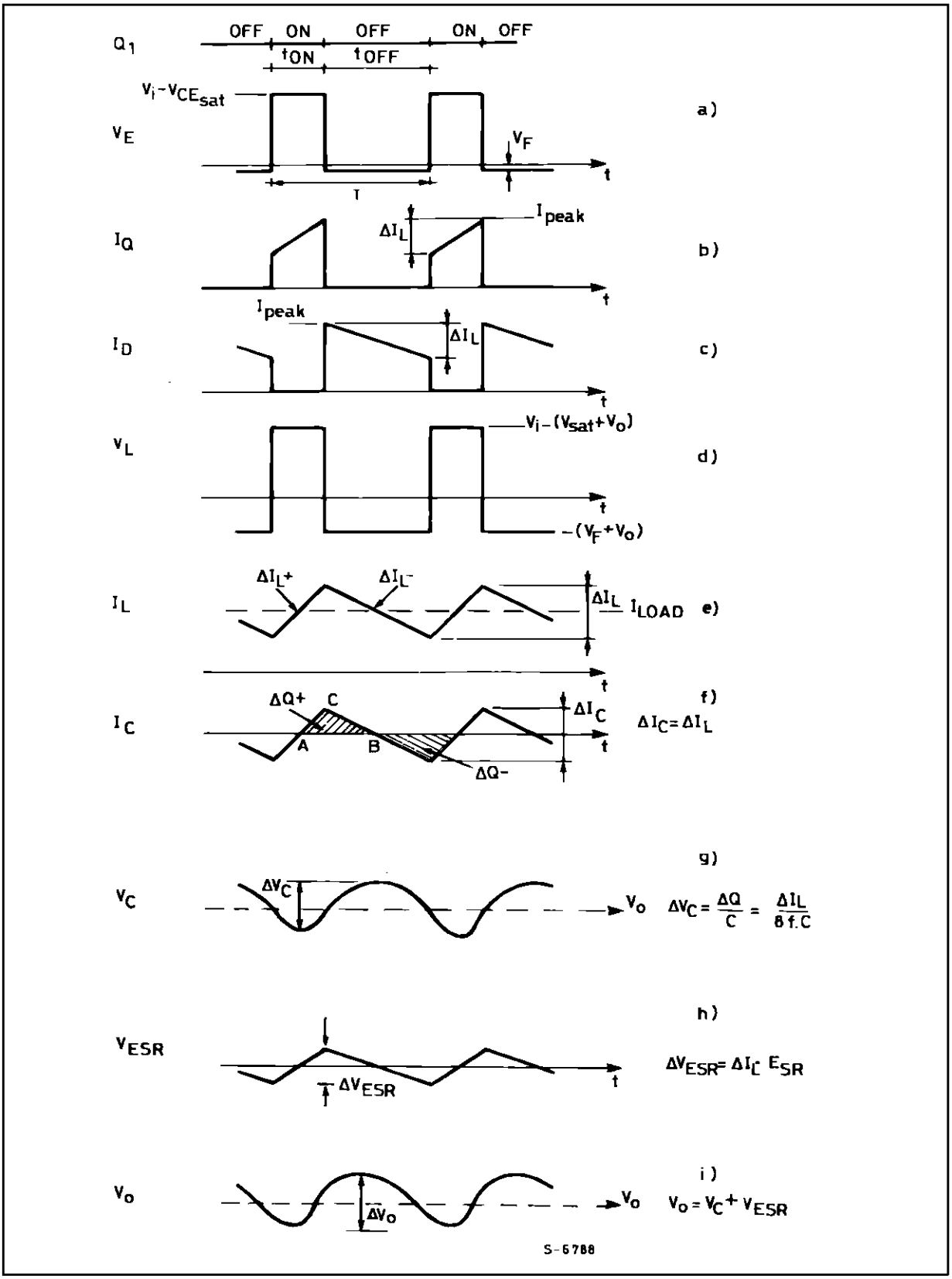


Fig. 2 shows the behaviour of the most significant waveforms, in different points of the circuit, which help to understand better the operation of the power section of the switching regulator. For the sake of simplicity, the series resistance of the coil has been neglected. Fig. 2a shows the behaviour of the emitter voltage (which is practically the voltage across the recirculation diode), where the power saturation and the forward V_F drop across the diode era taken into account.

The ON and OFF times are established by the following expression :

$$V_o = (V_i - V_{sat}) \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

Fig. 2b shows the current across the switching transistor. The current shape is trapezoidal and the operation is in continuous mode. At this stage, the phenomenadue to the catch diode, that we consider as dynamically ideal, are neglected. Fig. 2c shows the current circulating in the recirculation diode. The sum of the currents circulating in the power and in the diode is the current circulating in the coil as shown in fig. 2e. In balanced conditions the ΔI_L^+ current increase occuring during T_{ON} has to be equal to the ΔI_L^- decrease occurring during T_{OFF}. The mean value of I_L corresponds to the charge current.

The current ripple is given by the following formula :

$$\Delta I_L^+ = \Delta I_L^- = \frac{(V_i - V_{sat}) - V}{L} T_{ON} = \frac{V_o + V_F}{L} T_{OFF}$$

It is a good rule to respect to $I_{OMIN} \geq I_L/2$ relationship, that implies good operation in continuous mode. When this is not done, the regulator starts operating in discontinuous mode. This operation is still safe but variations of the switching frequency may occur and the output regulation decreases.

Fig. 2d shows the behaviour of the voltage across coil L. In balanced conditions, the mean value of the voltage across the coil is zero. Fig. 2f shows the current flowing through the capacitor, which is the difference between I_L and I_{LOAD}.

In balanced conditions, the mean current is equal to zero, and $\Delta I_C = \Delta I_L$. The current I_C through the capacitor gives rise to the voltage ripple.
This ripple consists of two components: a capacitive component, ΔV_C, and a resistive component, ΔV_{ESR}, due to the ESR equivalent series resistance of the capacitor. Fig. 2g shows the capacitive component ΔV_C of the voltage ripple, which is the integral of a triangular-shaped current as a function of time. Moreover, it should be observed that v_C (t) is in quadrature with i_C(t) and therefore with the voltage V_{ESR}. The quantity of charge ΔQ^+ supplied to the capacitor is given by the area enclosed by the ABC triangle in fig. 2f :

$$\Delta Q = \frac{1}{2} \cdot \frac{T}{2} \cdot \frac{\Delta I_L}{2}$$

which therefore gives :

$$\Delta V_C = \frac{Q}{C} = \frac{\Delta I_L}{8fc}$$

Fig. 2h shows the voltage ripple V_{ESR} due to the resistive component of the capacitor. This component is V_{ESR} (t) = i_C (t) · ESR. Fig. 2i shows the overall ripple V_o, which is the sum of the two previous components. As the frequency increases (> 20kHz), which is required to reduce both the cost and the sizes of L and C, the V_{ESR} component becomes dominant. Often it is necessary to use capacitors with greater capacitance (or more capacitors connected in parallel to limit the value of ESR within the required level.

We will now examine the stepdown configuration in more detail, referring to fig. 1 and taking the behaviour shown in fig. 2 into account.

Starting from the initial conditions, where Q = ON, $v_C = V_o$ and $i_L = i_D = 0$, using Kirckoff second principle we may write the following expression :

$V_i = v_L + v_C$ (V_{sat} is neglected against V_i).

$$V_i = L \frac{di_L}{dt} + v_C = L \frac{di_L}{dt} + V_o \quad (1)$$

which gives :

$$\frac{di_L}{dt} = \frac{(V_i - V_o)}{L} \quad (2)$$

The current through the inductance is given by :

$$I_L = \frac{(V_i - V_o)}{L} t \quad (3)$$

When V_i, V_o, and L are constant, I_L varies linearly with t. Therefore, it follows that :

$$\Delta I_L^+ = \frac{(V_i - V_o)\, T_{ON}}{L} \quad (4)$$

When Q is OFF the current through the coil has reached its maximum value, I_{peak} and because it cannot very instantaneously, the voltage across the coil is inverted and the diode D becomes forward biased to allow the recirculation of the current through the load.

When Q switches OFF, the following situation is present :

$v_C(t) = V_o$, $i_L(t) = i_D(t) = I_{peak}$

And the equation associated to the following loop may be written :

$$V_F + L \frac{di_L}{dt} + v_C = 0 \quad (5)$$

where :

$v_C = V_o$

$$\frac{dI_L}{dt} = -(V_F + V_o)/L \quad (6)$$

It follows therefore that :

$$i_L(t) = -\frac{V_F + V_o}{L} t \quad (7)$$

The negative sign may be interpretated with the fact that the current is now decreasing. Assuming that V_F may be neglected against V_o, during the OFF time the following behaviour occurs :

$$I_L = \frac{V_o}{L} t \quad (8)$$

therefore :

$$\Delta I_L^- = \frac{V_o}{L} T_{OFF} \quad (9)$$

But, because

$\Delta I_L^+ = \Delta I_L^-$ if follows that :

$$\frac{(V_i - V_o) T_{ON}}{L} = \frac{V_o T_{OFF}}{L}$$

which allows us to calculate V_o :

$$V_o = V_i \frac{T_{ON}}{T_{ON} + T_{OFF}} = V_i \frac{T_{ON}}{T} \quad (10)$$

where T is the switching period.

Expression (10) links the output voltage V_o to the input voltage V_i and to the duty cycle. The relation-ship between the currents is the following :

$$I_{iDC} = Io_{DC} \cdot \frac{T_{ON}}{T}$$

EFFICIENCY

The system efficiency is expressed by the following formula :

$$\eta\ \% = \frac{P_o}{P_i} 100$$

where $P_o = V_o I_o$ (with $I_o = I_{LOAD}$)

is the output power to the load and P_i is the input power absorbed by the system. P_i is given by P_o, plus all the other system losses. The expression of the efficiency becomes therefore the following :

$$\eta = \frac{P_o}{P_o + P_{sat} + P_D + P_L + P_q + p_{sw}} \quad (12)$$

DC LOSSES

P_{sat} : saturation losses of the power transistor Q. These losses increase as V_i decreases.

$$P_{sat} = V_{sat} \cdot I_o \frac{T_{ON}}{T} = V_{sat} I_o \frac{V_o}{V_i} \quad (13)$$

where $\frac{T_{ON}}{T} = \frac{V_o}{V_i}$ and V_{sat} is the power transistor saturation at current Io.

P_D : losses due to the recirculation diode. These losses increase as V_i increases, as in this case the ON time of the diode is greater.

$$P_D = V_F I_o \frac{V_i - V_o}{V_i} = V_F I_o \left(1 - \frac{V_o}{V_i}\right) \quad (14)$$

where V_F is the forward voltage of the recirculation diode at current I_o.

P_L : losses due to the series resistance R_S of the coil

$$P_L = R_S I_o^2 \quad (15)$$

P_q : losses due to the stand-by current and to the power driving current :

$$P_q = V_i I'_{3q} + V_i I''_{3q} \frac{T_{ON}}{T} \quad (16)$$

where being :

$\frac{T_{ON}}{T} = \frac{V_o}{V_i}$ it follows that :

$P_q = V_i I'_{3q} + V_o I''_{3q}$ in which :

$I'_{3q} = I_{3q}$ at 0 % duty cycle

$I''_{3q} = I_{3q(100\ \%\ d.c.)} - I_{3q\ (0\ \%\ d.c.)}$

SWITCHING LOSSES

P_{sw} : switching losses of the power transistor :

$$P_{sw} = V_i I_o \frac{t_r + t_f}{2T}$$

The switching losses of the recirculation diode are neglected (which are anyway negligible) as it is assumed that diode is used with recovery time much smaller than the rise time of the power transistor.

We can neglect losses in the coil (it is assumed that ΔI_L is very small compared to I_o) and in the output capacitor, which is assumed to show a low ESR.

Calculation of the inductance value, L

Calculation T_{ON} and T_{OFF} through (4) and (9) respectively it follows that :

$$T_{ON} = \frac{\Delta I_L^{+} \cdot L}{V_i - V_o} \qquad T_{OFF} \quad \frac{\Delta I_L^{-} \cdot L}{V_o}$$

But because :

$T_{ON} + T_{OFF} = T$ and $\Delta I_L^{+} = \Delta I_L^{-} = \Delta I_L$,

it follows that :

$$\frac{\Delta I_L \cdot L}{V_i - V_o} + \frac{\Delta I_L \cdot L}{V_o} = T$$

Calculating L, the previous relation becomes :

$$L = \frac{(V_i - V_o)\, V_o}{V_i\, \Delta I_L}\, T \qquad (18)$$

Fixing the current ripple in the coil required by the design (for instance 30% of I_o), and introducing the frequency instead of the period, it follows that :

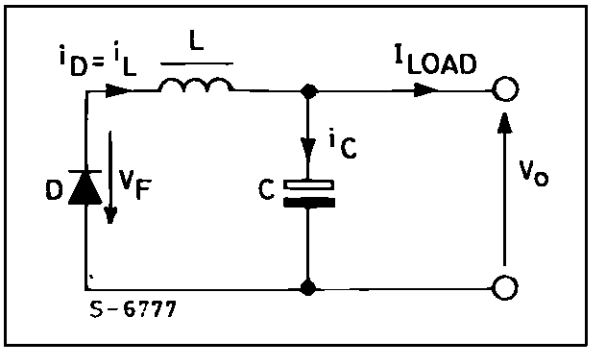
$$L = \frac{(V_i - V_o)\, V_o}{V_i \cdot 0.3 \cdot I_o \cdot f}$$ where L is in Henry and f in Hz

Calculation of the output capacitor C

From the output node in fig. 3 it may be seen that the current through the output capacitor is given by :

$i_c(t) = i_L(t) - I_o$

Figure 3 : Equivalent Circuit Showing Recirculation when Q1 is Turned Off.



From the behaviour shown in fig. 2 it may be calculated that the charge current of the output capacitor, within a period, is $\Delta I_L/4$, which is supplied for a time T/2. It follows therefore that :

$$\Delta V_C = \frac{\Delta I_L}{4C}\,\frac{T}{2} = \frac{\Delta I_L\, T}{8C} = \frac{\Delta I_L}{8fC} \qquad (19)$$

but, remembering expression (4) :

$$\Delta I_L^{+} = \frac{(V_i - V_o)\, T_{ON}}{L} \quad \text{and} \quad T_{ON} = \frac{V_o}{V_i}\, T$$

therefore equation (19) becomes :

$$\Delta V_C = \frac{(V_i - V_o)\, V_o}{8\, V_i f^2\, L\, C}$$

Finally, calculating C it follows that :

$$C = \frac{(V_i - V_o)\, V_o}{8\, V_i\, \Delta V_C\, f^2\, L} \qquad (20)$$

where : L is in Henrys
C is in Farads
f is in Hz

Finally, the following expression should be true :

$$ESR_{max} = \frac{\Delta V_{Cmax}}{\Delta I_L} \qquad (21)$$

It may happen that to satisfy relation (21) a capacitance value much greater than the value calculated through (20) must be used.

TRANSIENT RESPONSE

Sudden variations of the load current give rise to overvoltages and undervoltages on the output voltage. Since $i_c = C\,(dv_c/dt)$ (22), where $dv_c = \Delta V_o$, the instantaneous variation of the load current ΔI_o is supplied during the transient by the output capacitor. During the transient, also current through the coil tends to change its value.
Moreover, the following is true :

$$v_L = L\,\frac{di_L}{dt} \qquad (23) \qquad \text{where } di_L = \Delta I_o.$$

$v_L = V_i - V_o$ for a load increase

$v_L = V_o$ for a load decrease

Calculating dt from (22) and (23) and equalizing, it follows that :

$$L\,\frac{di_L}{v_L} = C\,\frac{dv_c}{i_c}$$

Calculating dv_c and equalizing it to ΔV_o, it follows that :

$$\Delta V_o = \frac{L \Delta I_o^2}{C(V_i - V_o)} \qquad (24) \qquad \text{for } +\Delta I_o$$

$$\Delta Vo = \frac{L \Delta I_o^2}{C V_o} \qquad (25) \qquad \text{for } -\Delta I_o$$

From these two expressions the dependence of overshoots and undershoots on the L and C values may be observed. To minimize ΔV_o it is therefore necessary to reduce the inductance value L and to increase the capacitance value C. Should other auxiliary functions be required in the circuit like reset or crowbar protections and very variable loads may be present, it is worthwhile to take special care for minimizing these overshoots, which could cause spurious operation of the crowbar, and the undershoot, which could trigger the reset function.

DEVICE DESCRIPTION

Fig. 4 shows the package in which the device is mounted and the pin function assignments.

The internal structure of the device is shown in fig. 5. Each block will now be examined.

Power supply

The device is provided with an internal stabilized power supply that, besides supplying the reference voltage of 5.1V for the whole system, also supplied the internal analog blocks.

Special features of the voltage reference are its accuracy, temperature stability and high line rejection. Through zenze-zap trimming, the voltage is within ± 2% limits.

Figure 4 : Pin Assignments of the L296.

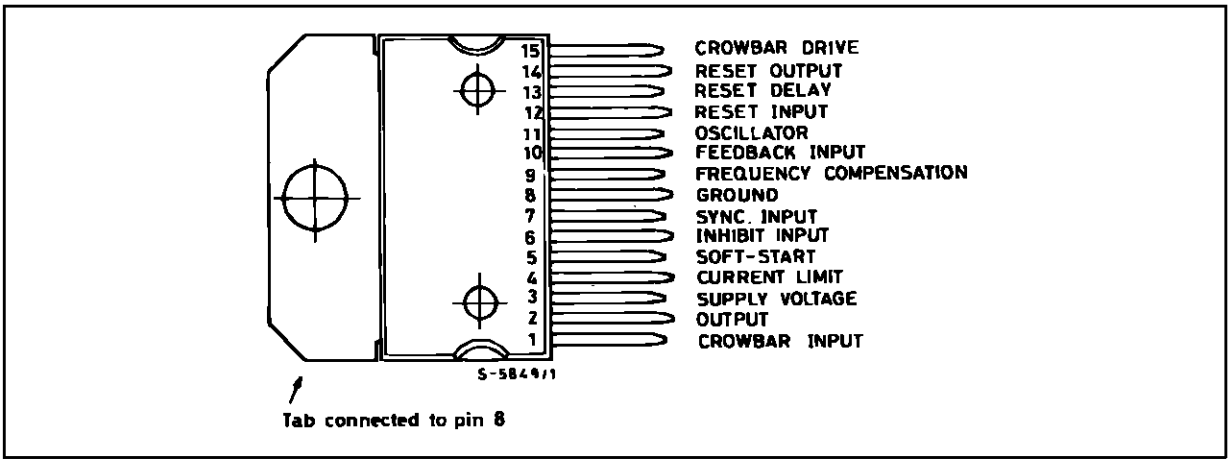
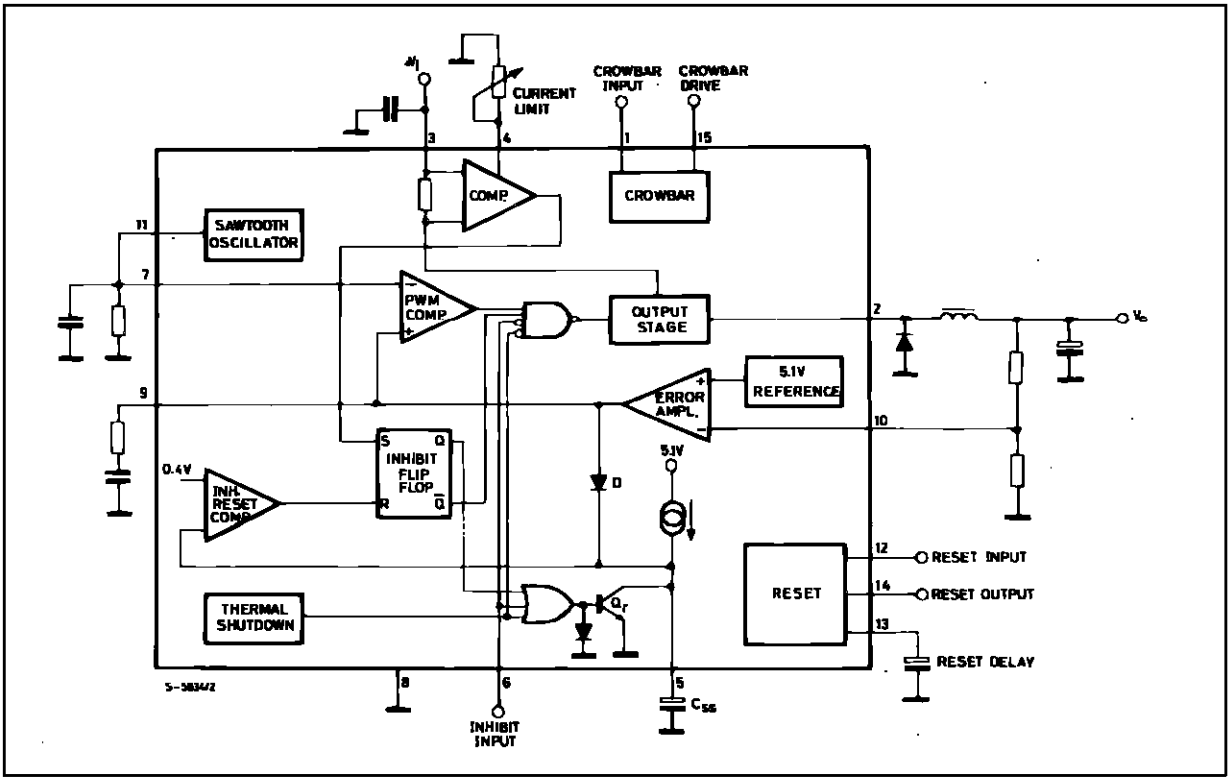


Figure 5 : Block Diagram of the L296. In Addition to the Basic Regulation Loop the Device includes Functions such as Reset, Crowbar and Current Limiting.



OSCILLATOR

The oscillator block generates the saw-tooth waveform that sets the switching frequency of the system. This signal, compared with the output voltage of the error amplifier, generates the PWM signal to be sent to the power output stage. The saw-tooth, whose amplitude is between 1.2V and 3.2V, is generated by charging rapidly the C_{osc} capacitor which then discharges across the R_{osc} resistance. As shown in fig. 6, the oscillator is realized by a comparator (with grounded compatible input) with hysteresis whose thresholds are 1.2V and 3.2V respectively. The C_{osc} capacitor and the R_{osc} resis-tance are connected to the non-inverting input of the comparator which set the oscillating frequency is fixed. When the voltage on pin 11 is less than 3.2V, the switch S_1 is closed and the current generator charges the C_{osc} capacitor rapidly ; in this phase S_2 is also closed. As soon as 3.2V is reached the comparator output drives S_2 open (therefore opening S_1, too) ; the inverting input voltage is reduced to about 1.2V and the capacitor starts to discharge itself across the R_{osc} resistor (the I_{bias} effect is neglected). When the voltage reaches 1.2V, S_2 and S_1 close again and a new cycle starts. The generated waveform is shown in fig. 7.

To achieve a good accuracy of the switching frequency it is essential to have a charging time of the capacitor which is much smaller than the discharging time. In this way, the oscillation frequency only depend son the external components C_{osc} and R_{osc}. For this reason the capacitor charging current (when S_1 is ON) is typically around 10mA. For example, with a 2.2nF capacitor to switch from 1.2V to 3.2V about 400ns is required, which is negligible compared to the 10µs period that occurs when the operation is performed at 100kHz. The diagrams shown in fig. 8 allow the calculation of the R_{osc} value (R_1 in fig. 8) with C_{osc} as a parameter (C_3 in fig. 8) when the oscillation frequency required for operation has been previously fixed.

Figure 6 : Internal Schematic of the Oscillator.

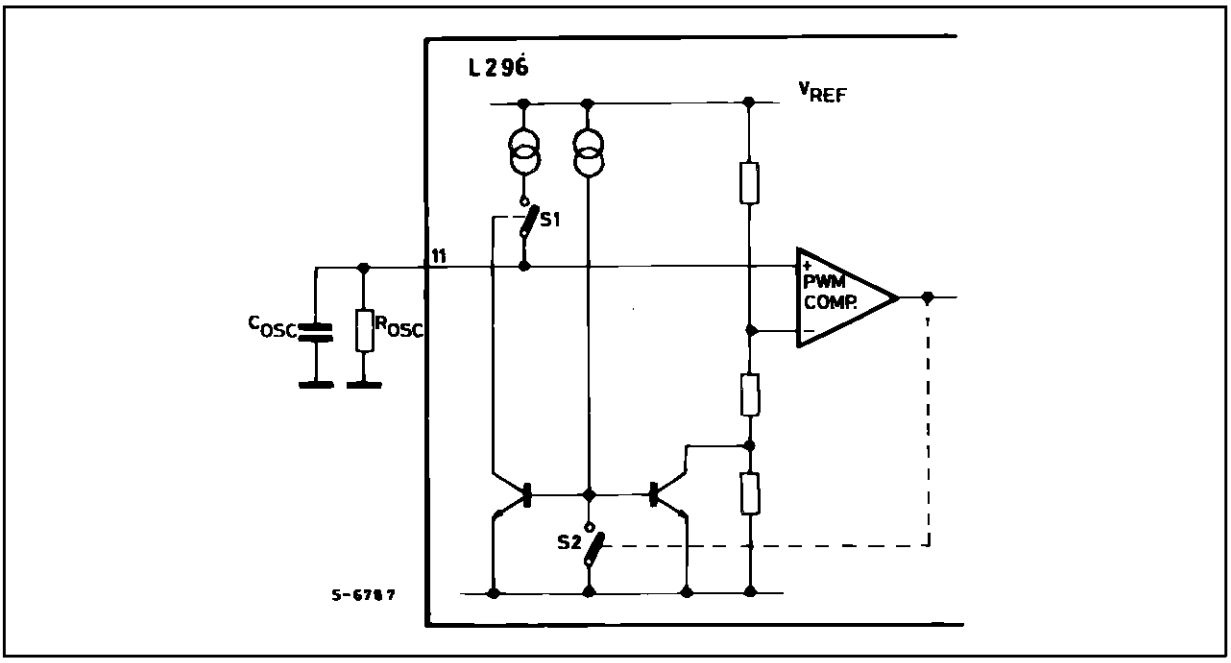


Figure 7a : Oscillator Waveform at Pin 11 with f = 100Khz (R_{osc} = 4.3KΩ, C_{osc} = 2.2nF).

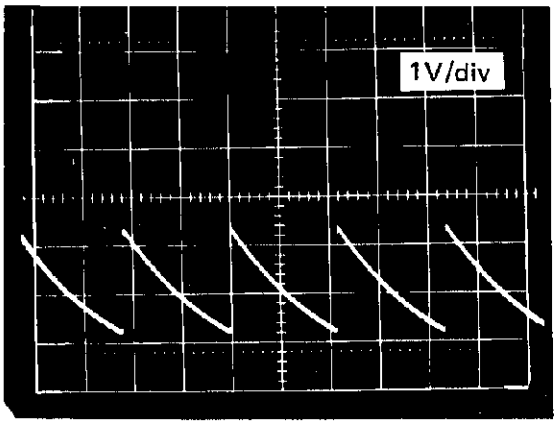


Figure 7b : Oscillator Waveform at Pin 11 with f = 50Khz (R_{osc} = 9.1KΩ, C_{osc} = 2.2nF).

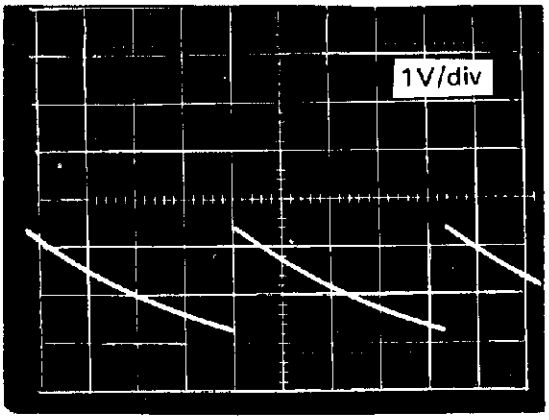


Figure 8 : Nomogram for the Choice of Oscillator Components.

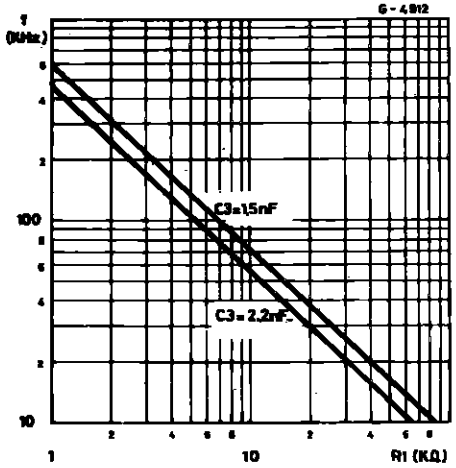


Fig. 8 shows two suggested values for the C_{osc} capacitance. Excessively low capacitance value may give rise to an inaccuracy of the upper threshold due to the switching delays of the comparator. This inaccuracy in caused by an excessively short rise time of the voltage. A capacitance value too high gives rise to a charging time which is too compared to the discharging time. An additional inaccuracy cause would be therefore present for the switching frequency, now due to spread of the charge current.

The oscillation frequency is given by the following formula :

$$f_{osc} = \frac{1}{R_{osc}\, C_{osc}} \qquad (26)$$

PWM (see fig. 9)

The PWM signal is generated on the comparator output ; the triangular-shaped waveform and the continuous signal coming from the output of the transconductance error amplifier are sent to its inputs. The PWM signal is then transferred to the driving stage of the output power transistor.

SOFT START (see fig. 9)

Soft start is an essential function for correct start-up, to prevent stresses and possible breakdown from occurring in the power transistor and to obtain a monotonically increasing output voltage.
In particular, the L296, as it does not have any duty cycle limitation and due to the type of current limitation does not allow the output to be forced to a steady state without the aid of the soft-start facility. Soft-start operates at the start-up of the system, after the inhibit has been activated, after an intervention of the current limitation and after the intervention of the thermal protection.

The soft-start function is realized through a capacitor connected to pin 5 which is charged at constant current (≅ 100μA) up to a value of about V_{REF}. During the charging time, through PNP transistor Q58, the voltage on pin 9 is forced to increase with the same rising speed as on pin 5. Starting from the discharged capacitor condition (pin 5 voltage = 0V) the power transistor is in the OFF condition, as the voltage on pin 9 is smaller than the minimum level of the ramp voltage. As the capacitor is charged, the PWM signal begins to be generated as soon as the error amplifier output voltage crosses the ramp ; the power stage starts to switch with steadily increasing duty cycle. This behaviour is shown in fig. 10. As soon as the steady condition is reached the duty cycle sets itself to the right value due to the effect of the feedback network while the soft-start capacitor completes its charging to a value very close to V_{REF}.

The soft-start effect is determined, apart from the switch-on time, when the current limitation operates, due to either an overload or a short circuit, to keep the mean value of the current absorbed by the power supply low.

Moreover from fig. 11 it may be observed that since the voltage on pin 9 can decrease under the minimum ramp level and increase over the maximum level no limitations have been provided on the duty cycle, which therefore may vary between 0 and 100%.

Figure 9 : Partial Internal Schematic Showing PWM and Soft Start Blocks.

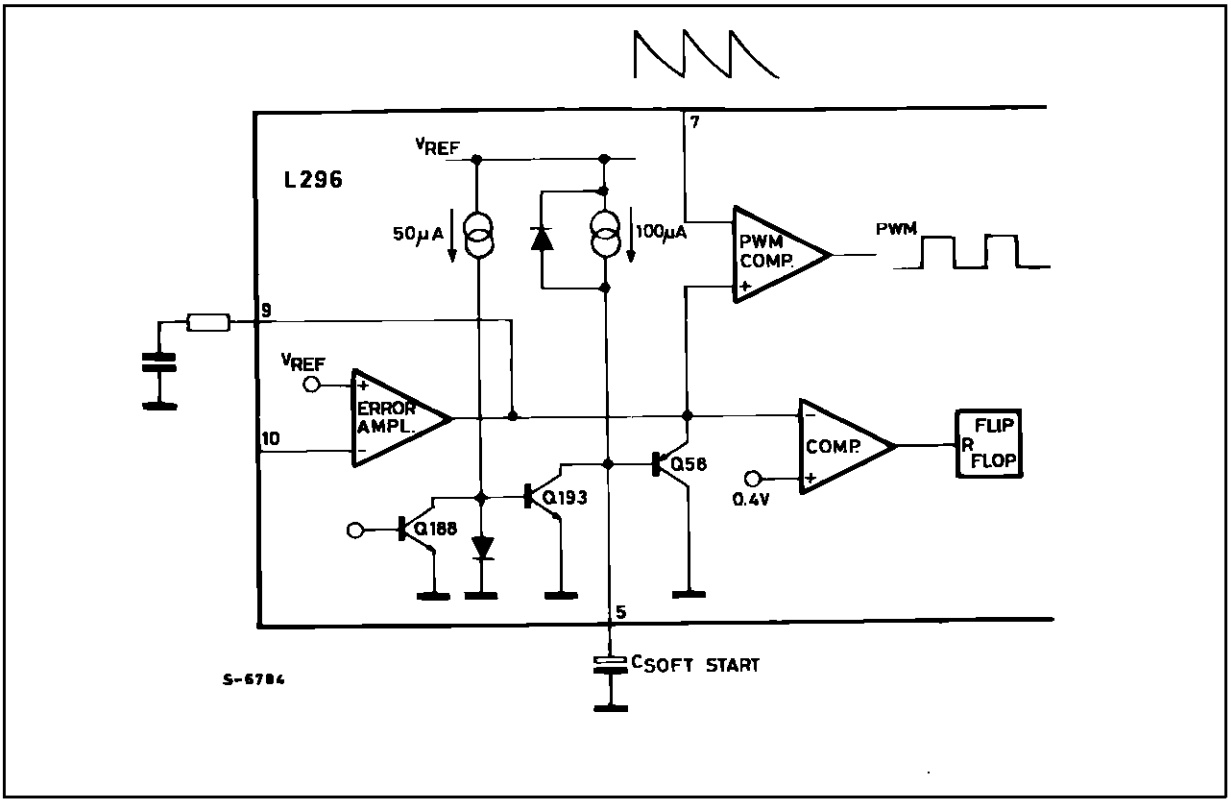


Figure 10 : Soft Start Waveforms. When power is applied, or after an inhibit, the L296's output current rises slowly under control of the soft start circuit.

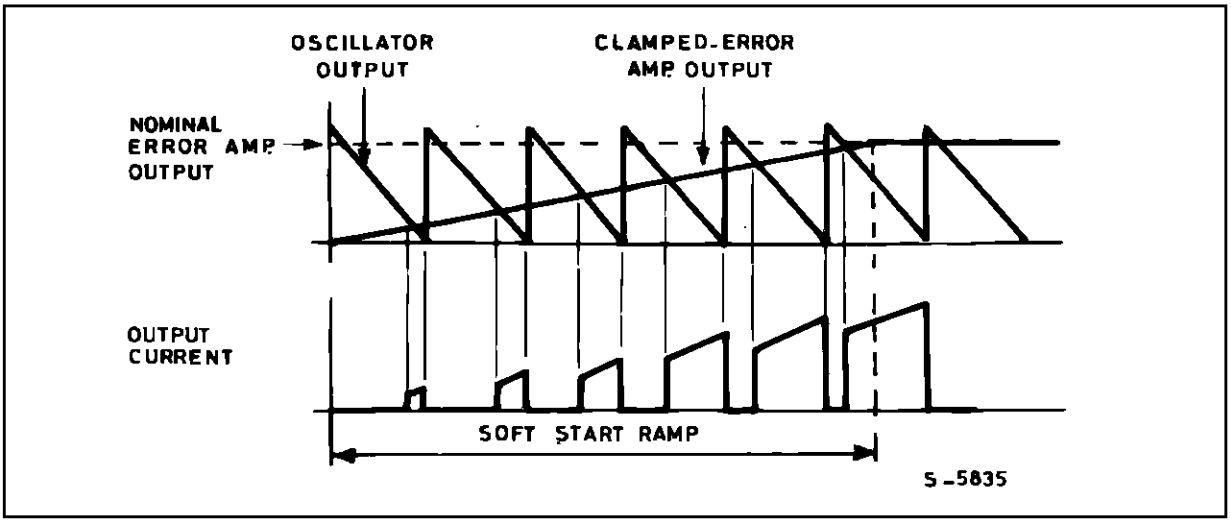
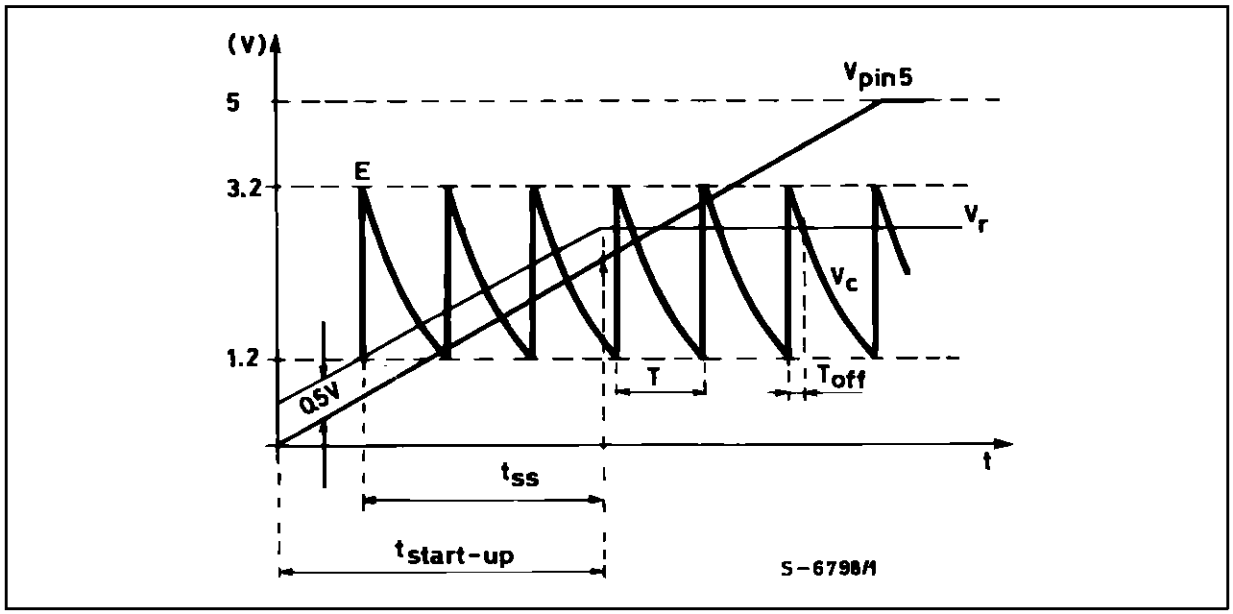


Figure 11 : Waveform for Calculation of Duty Cycle and Soft Start Time.



CALCULATING THE DUTY CYCLE AND SOFT-START TIME

Assume, for simplicity, that the rising edge of the ramp is instantaneous; V_r is the output voltage of the error amplifier and V_c the ramp voltage (see fig. 11). The PWM comparator block switches when $V_r = V_c$; therefore :

$$V_r = V_c = E\, e^{-\frac{t}{R_{osc}\, C_{osc}}}$$

Consequently :

$$t = R_{osc}\, C_{osc}\, \ln\frac{E}{V_r}$$

The time obtained from this expression is the T_{OFF} time of the power transistor. The duty cycle d is given by :

$$d = \frac{T_{ON}}{T} = \frac{T - R_{osc}\, C_{osc}\, \ln\frac{E}{V_r}}{T} = \\ = 1 - \ln\frac{E}{V_r} = \frac{Vo}{V_i} \qquad (27)$$

Consequently, starting with the capacitor discharged, the output of the regulator will be at the nominal level when the voltage at the terminal of the capacitor (which is charged by a constant current) has reached $V_r - 0.5V$.

$$t_{start\text{-}up} = \frac{C_{ss}\,(V_r - 0.5V)}{I_{5so}}$$

where C_{ss} is the soft-start capacitor and I_{5so} is the charging current.

Considering as the soft-start time the time required for the soft-start capacitor to charge from (1.2 V – 0.5V) to $V_r - 0.5V$, gives :

$$t_{ss} = \frac{C_{ss}\,(V_r - 1.2)}{I_{sso}}$$

substituting V_r from (27) gives :

$$V_r = E\, e^{-\left(1 - \frac{V_o}{V_i}\right)}$$

substituting into (28) gives :

$$t_{ss} = \frac{C_{ss}}{I_{sso}}\,(E\, e^{\left(\frac{V_o}{V_i} - 1\right)} - 1.2)$$

SYNCHRONIZATION

The synchronization function is available on pin 7, this function allows the device to be switched at an externally generated frequency (leaving pin 11 open), or to mutually synchronize several devices, using one of them as master and the others as slave (fig. 12).

This allows several devices to be operated at the same frequency, avoiding undesirable intermodulation phenomena. The number if mutually synchronizable devices is obviously much greater than the three devices shown in the figure. It is anyway diffi-

cult to establish an exact maximum number of devices, as it depends on different conditions.

The first consideration concerns the accuracy which must be achieved and maintained on the oscillation frequency. Since the bias current on pin 7 is an output current, the sum of all the bias currents must be much smaller than the capacitor discharge current in close proximity to the lower discharge threshold. Therefore, assuming C_{osc} = 2.2nF and R_{osc} = 4.3KΩ, it follows that :

$$\frac{1.2V}{4.3K\Omega} = 280\mu A$$

Assuming that a 10% variation may be accepted, it follows therefore that the number of synchronizable devices is given by :

$$N = \frac{28\mu A}{I_{bias\,max}}$$

This means that if the overall I_{bias} is too high it may modify the discharging time of the capacitor.

The second consideration concerns the layout design.

In the presence of a great number of devices to be synchronized, the lenght of the paths may become significant and therefore the distributed inductance introduced along the paths may begin to modify the triangular shaped waveform, particularly the rising edge which is very steep. This effect would affect the devices that are physically located more distant from the master device.

The amplitude of the saw-tooth to be externally connected must be with in 0.5V and 3.5V, values also representing the maximum swing of the error amplifier output.

CURRENT LIMITATION

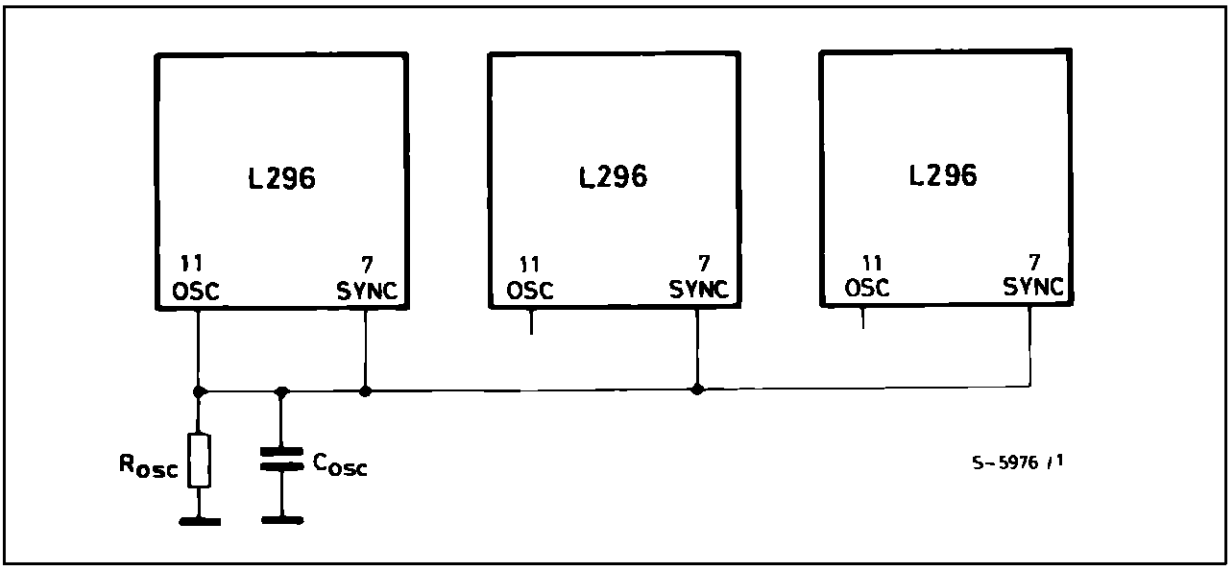
The current limitation function has been realized in a rather innovative way to avoid overload condition during the short circuit operation. In fact, while for all the other devices a constant current limitation is implemented by acting on the duty cycle (therefore, in short circuit conditions an output current is equal to the maximum limitation current), the new control approach allows operation in short circuit conditions with a mean current much smaller than the allowed 4A value. Operation of the current limiter will now be described.

Refer to the block diagram, fig. 13.

The current which is delivered from the output transistor to the load flows through the current sensing resistor R_S. When the voltage drop on R_S is equal to the offset voltage of the current comparator, the comparator generates a set pulse for the flip-flop, with a delay of about 1µsec. The purpose of this delay is to avoid triggering of the protection circuit on the current peak that occurs during the recirculation phase. Therefore, the output $\overline{Q}$ goes low and the power stage is immediately switched off, while the output $\overline{Q}$ goes high and acts directly on the soft-start capacitor dischargng the soft-start capacitor at a constant current (about 50µA).

When the voltage on pin 5 reaches 0.4V the comparator triggers, supplying a reset pulse to the flip-flop ; from now on, the power stage is enable and the soft-start phase starts again. When the limitation cause, either overload or short circuit, is still present the cycle repeats again. The waveform of the output current on pin 2 is shown in fig. 14.

Figure 12 : In multiple supplies several l296's can be synchronized as shown here.



From fig. 14 it may be observed how this current limitation technique allows the short circuit operation with a very low output current value.

It is possible to reduce the maximum current value by acting on pin 4. On this pin a voltage of about 3.3V is present ; by connecting a resistance a constant current, given by 3.3/R, is sent to ground. This current reduces the offset voltage of the current comparator, therefore anticipating its triggering threshold.

Figure 13 : Partial Schematic Showing the Current Limiter Circuit.

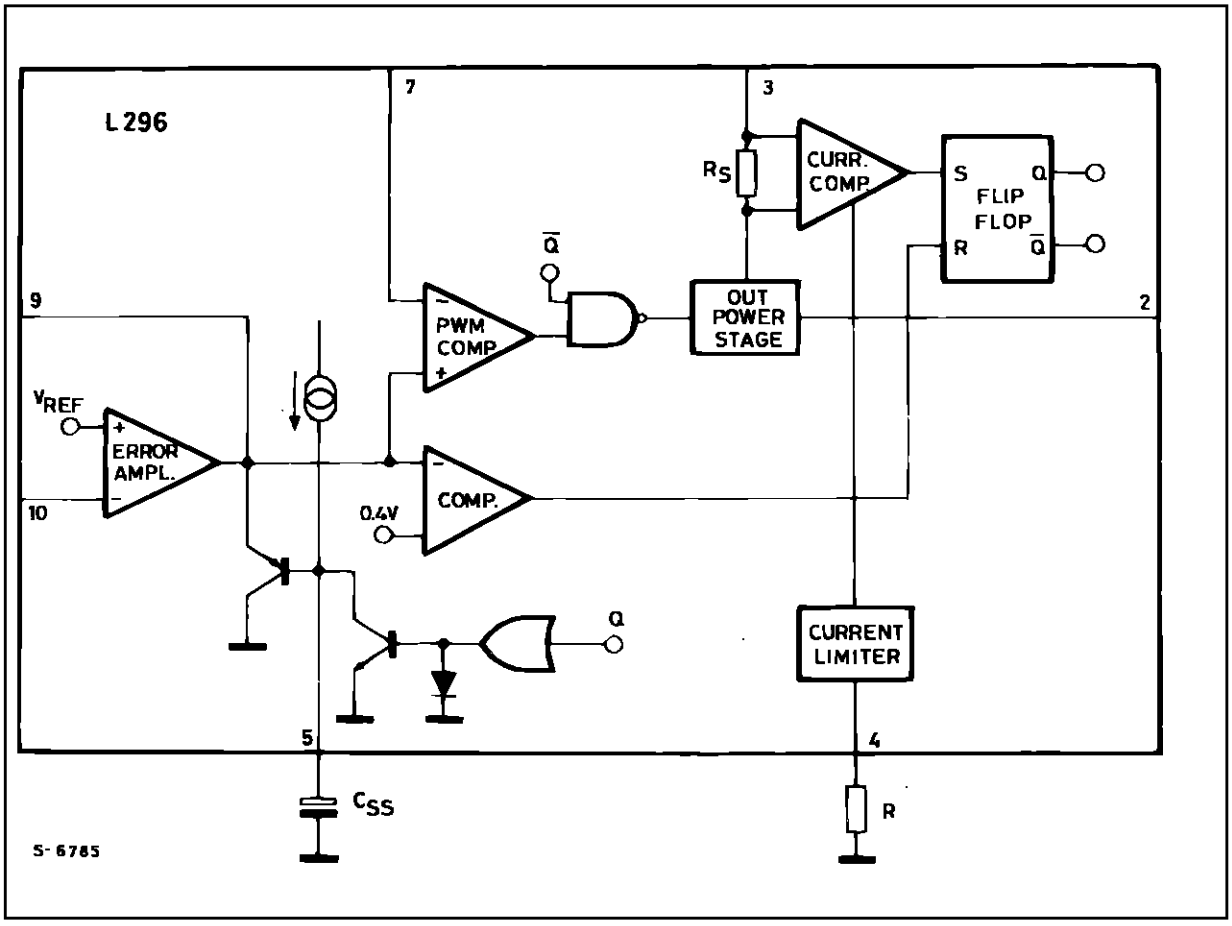


Figure 14a : Current Limiter Waveforms.

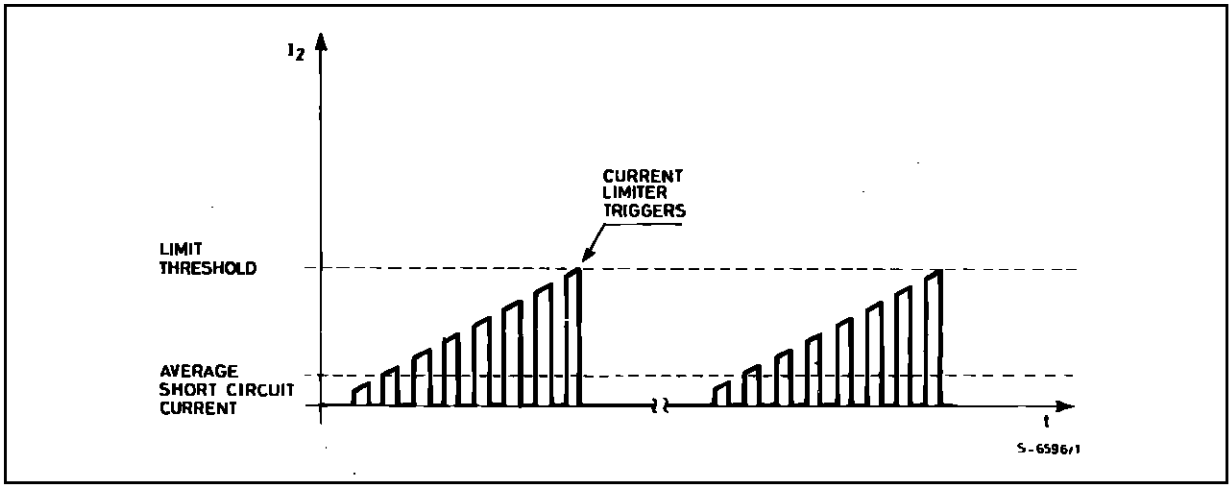


Figure 14b : Load Current in Short Circuit Conditions (V_i = 40V, L = 300µH, f = 100KΩ).

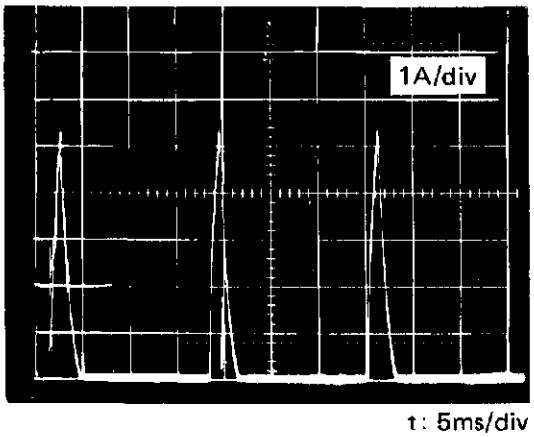
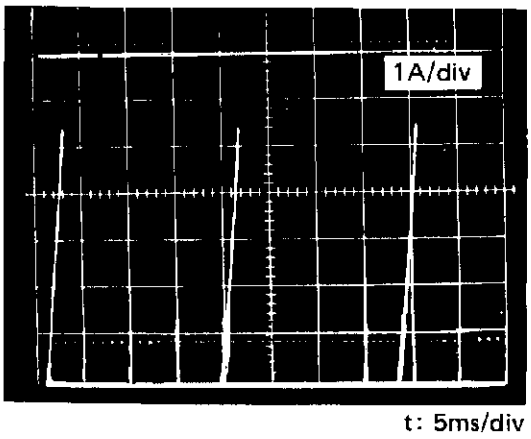


Figure 14c : Current at Pin 2 when the Output is Short Circuited.



RESET

The reset function is of great importance when the device is used to supply microprocessors, logic devices, and so on. This function differentiates the L296 device from all previous devices. The block diagram of the function is shown in fig. 15. A reset signal is generated when the output voltage is within the limits required to supply the microprocessor correctly.

The reset function is realized through the use of 3 pins : the reset input pin 12, the reset delay pin 13 and the reset output pin 14. When the voltage on pin 12 is smaller than 5V the comparator output is high and the reset capacitor is not charged because the transistor Q is saturated and the voltage on pin 14 is at low level, since Q2 is saturated, too. When the voltage on pin 12 goes above 5V, the transistor Q switches OFF and the capacitor can start to charge through a current generator of about 100µA. When the voltage on pin 13 goes above 4.5V the output of the related comparator switches low and the pin 14 goes high. As the output consists of an open collector transistor, a pull-up external resis-tance is required. In contrast, when the reset input voltage goes below 5V, less a hysteresis voltage of about 100mV, the comparator triggers again and instantaneously sets the voltage on pin 14 low, therefore forcing to saturation the Q1 transistor, that starts the rapid discharge of the capacitor. Obviously, the reset delay is again present when the voltage on pin 13 is allowed to go under 4.5V.

To achieve switching operations without uncertainties the two comparators have been provided with an hysteresis of about 100mV. In every operating condition the reset switching is guaranteed with a minimum reset input of 4.75V, the value required for correct operation of the microprocessor even in the presence of the minimum V_{REF} value.

Normally pin 12 is used connected to pin 10. When it is connected to the output, the function may be more properly called "reset" ; on the other hand, when it is connected through resistive divider, to the input voltage, the function is called "power fail". Fig. 16 and fig. 17 show the two possible usages.

The "power-fail" function is used to predict, with a given advance, the drop of the regulator output voltage, due to main failures, which is enough to save the data being processed into protected memory areas. Fig. 18 summarizes the reset function operation.

Figure 15 : Partial Schematic Showing Reset Circuit.

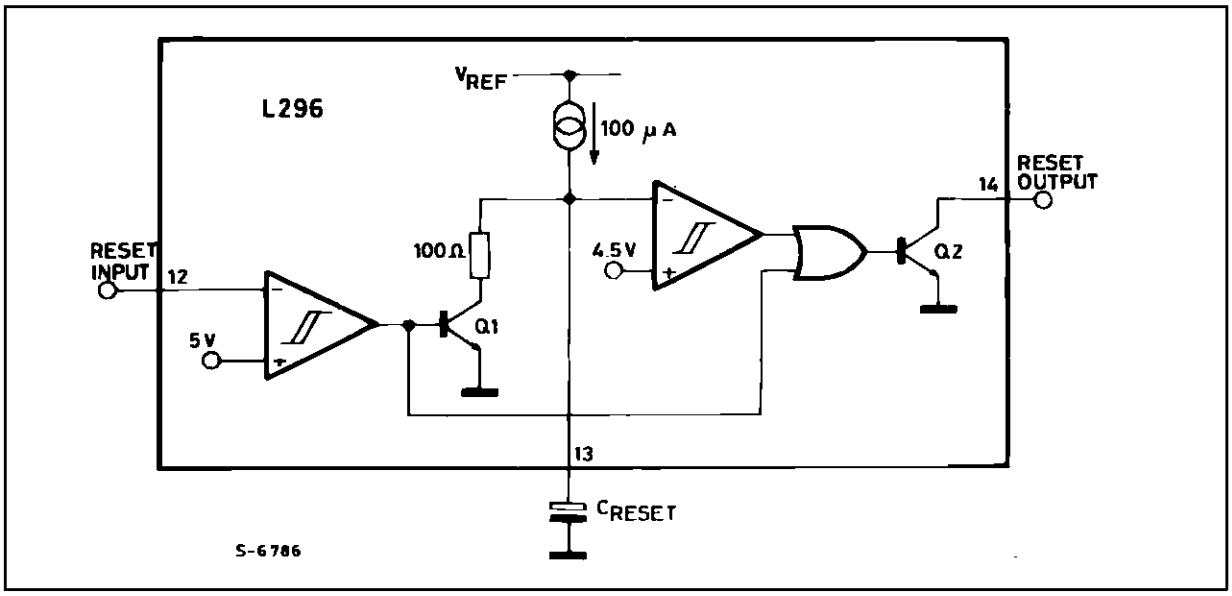


Figure 16 : For Power - On reset the reset block is connected as shown here.

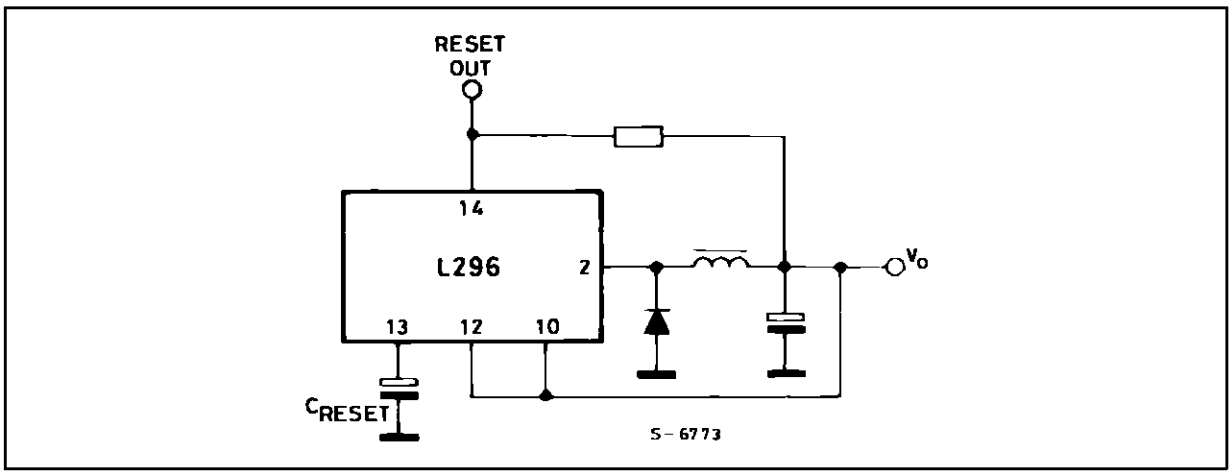


Figure 17 : To obtain a power fail signal, the reset block is connected like this.

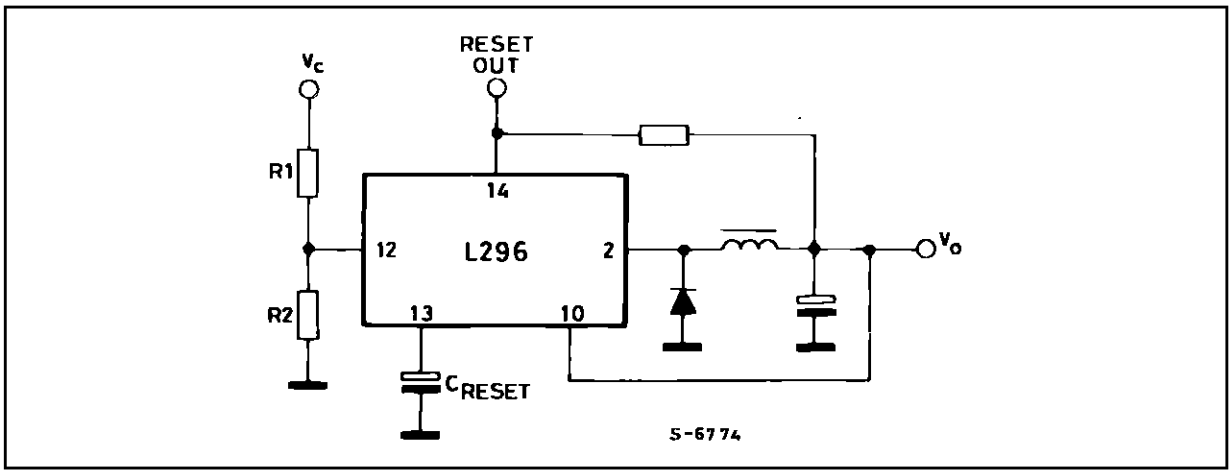
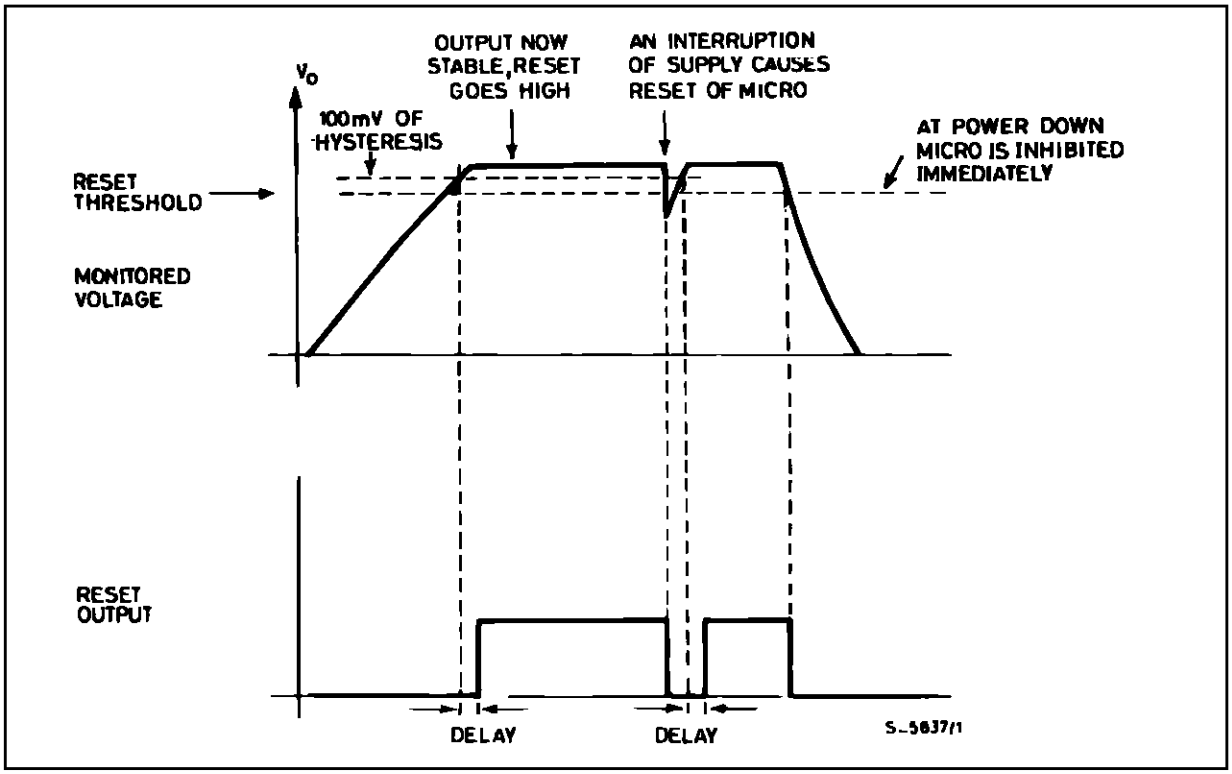


Figure 18 : Waveform of the Reset Circuit.



CROWBAR

This protection function is realized by a completely independent block, using pin 1 as input and pin 15 as output. It is used to prevent dangerous over voltages from occurring when the output exceeds 20% of rated value. Pin 15 is able to output a 100mA current to be sent to the gate of a SCR which, triggering, short circuits either output or the input. When connected to the input, as the SCR is triggered a fuse in series connected to power supply is blown and to bring the system back to operation manual intervention is requested. Figs. 19, 20 and 21 show the different configurations.

When the voltage on pin 1 exceeds by about 20% the V_{REF} value the output stage is activated, which sends a current to the SCR gate, after a delay of about 5µsec to make the system insensitive to low duration spikes. When activated, the output stage delivers about 100mA ; when not activated, it drains about 5mA and shows a low impedance to the SCR gate to avoid incorrect triggering due to random noise. If the crowbar function is not used connect pin 1 to ground.

Figure 19 : Connection of Crowbar Circuit at Output for 5.1V Output Applications.

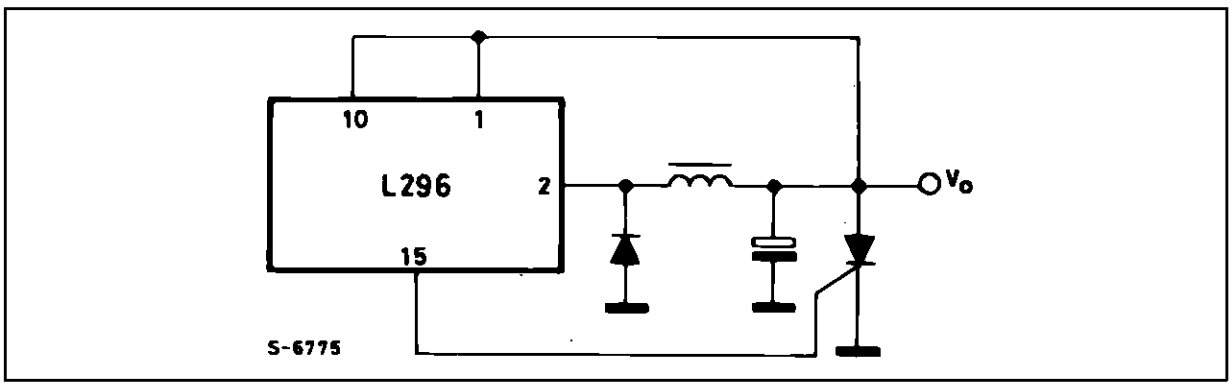


Figure 20 : Connection of Crowbar Circuit at Output for Output Voltages above 5.1V.

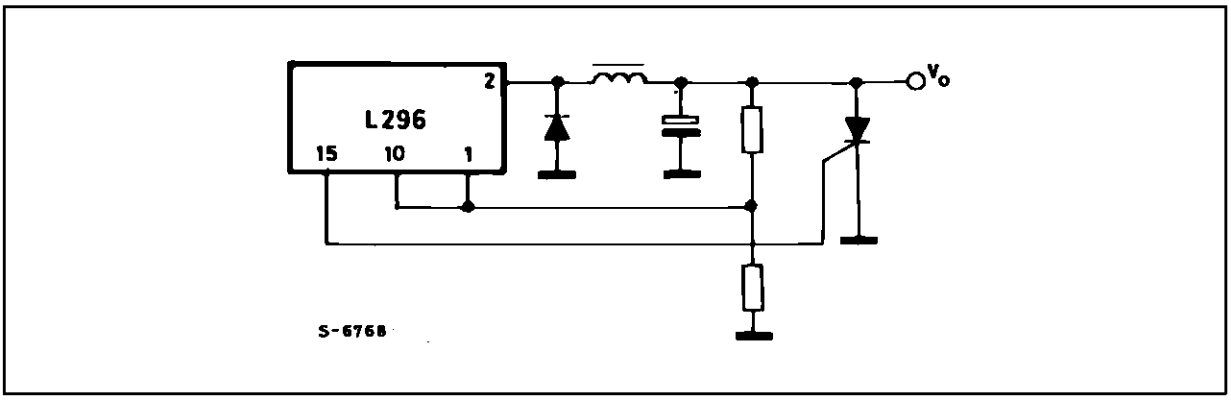
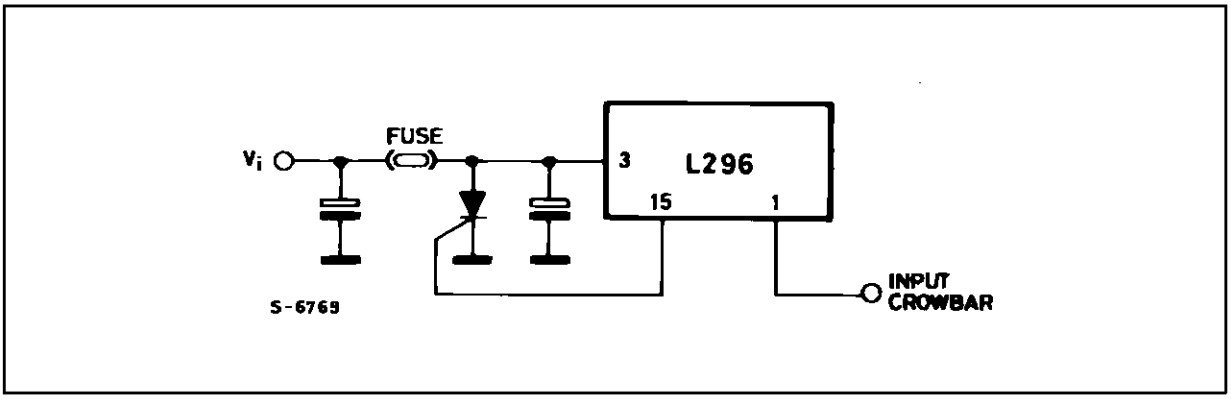


Figure 21 : Connection of Crowbar Circuit to Protect Input. When triggered, the scr blows the fuse.



INHIBIT

The inhibit input (pin 6) is TTL compatible and is activated when the voltage exceeds 2V and deactivated when the voltage goes under 0.8V. As may be seen in the block diagram, the inhibit acts on the power transistor, instantaneously switching it off and also acts on the soft-start, discharging its capacitor. When the function is unused, pin 6 must be grounded.

THERMAL PROTECTION

The thermal protection function operates when the junction temperature reaches 150°C ; it acts directly on the power stage, immediately switching it off, and on the soft-start capacitor, discharging it. The thermal protection is provided with hysteresis and, therefore, after an intervention has occurred, it is necessary to wait for the junction temperature to decrease of about 30°C below the intervention threshold.

APPLICATIONS

Though the L296 is designed for step-down regulator configurations it may be used in a variety of other applications. We will now examine these possibilities and show how the capabilities of the device may be extended.

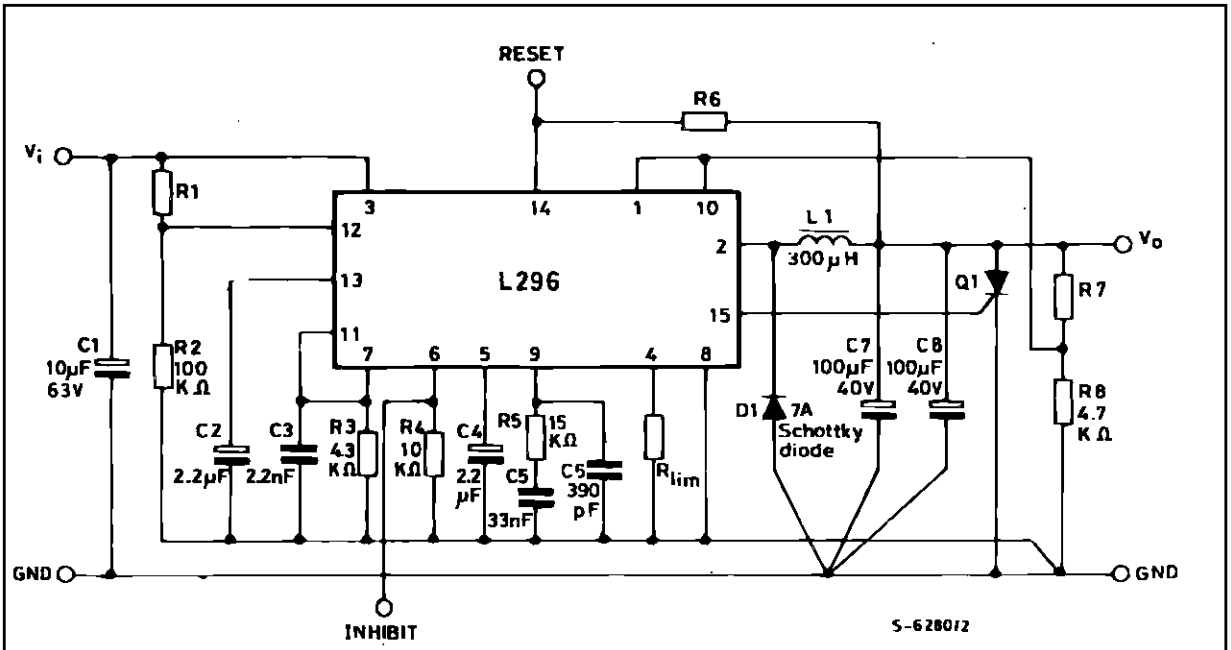
In fig. 22 the complete typical application is shown, where all the functions available on the device are being used. This circuit delivers to the load a maximum current of 4A and a voltage which is established by the voltage divider constituted by R_7 and R_8 resistances. The following table is helpful for a quick calculation of some standard output voltages :

Resistor Value for Standard Output Voltages

V_o	R_8	R_7
12 V	4.7 kΩ	6.2 kΩ
15 V	4.7 kΩ	9.1 kΩ
18 V	4.7 kΩ	12 kΩ
24 V	4.7 kΩ	18 kΩ

To obtain $V_o = V_{REF}$ the pin 10 is directly connected to the output, therefore eliminating both R_7 and R_8. The switching frequency is 100kHz.

Figure 22 : Schematic, PCB Layout and Suggested Component Values for the Evaluation Circuit used to characterize the L296. This is a typical stepdown application which exercises all the device's functions.



C7, C8 : EKR (ROE)

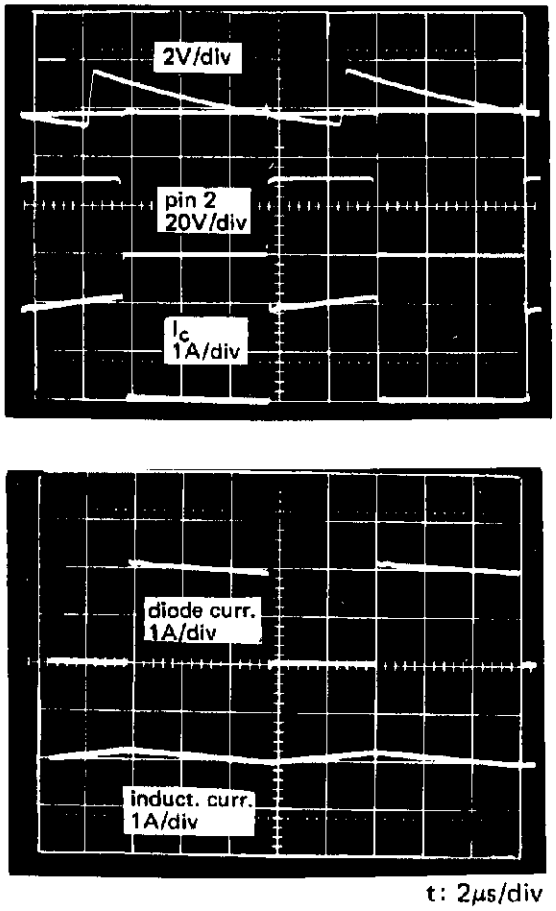
SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 - A2MPP	43	1.0 mm.	
Thomson GUP 20 x 16 x 7	65	0.8 mm.	1 mm.

SUGGESTED INDUCTOR (L1) (continued)

Core Type	No Turns	Wire Gauge
Siemens EC 35/17/10 (B6633 & - G0500 - x 127)	40	2 x 0.8 mm.
VOGT 250 µH Toroidal Coil, Part Number 5730501800		

Figure 23 : Oscilloscope Photographs Showing Main Waveform of the Figure 22 Circuit.



The oscilloscope photographs of the main waveforms are shown in fig. 23. The output voltage ripple ΔV_O depends on the current ripple in the coil and on the performance of the output capacitor at the switching frequency (100kHz). A capacitor suitable for this kind of application must have a low ESR and be able to accept a high current ripple, at the working frequency. For this application the Roederstein EKR series capacitors have been selected, desi-gned for high frequency applications (> 200kHz) and manufactured to show low ESR value and to accept high current ripples. To minimize the effects of ESR, two 100μF/40V capacitors have been connected in parallel. The behaviour of the impedance as a function of frequency is shown in fig. 24.

Also the selection of the catch diode requires special care. The best choice is a Schottky diode which minimizes the losses because of its smaller forward voltage drop and greater switching frequency rate. A possible limitation comes from the backward voltage, that generally reaches 40V max.

When the full input voltage range of the device is required in this application it is possible to use superfast siodes with 35 to 50ns rated recovery time, where no more problems on the backward voltage occur (on the other hand, they show a greater forward voltage). The use of slower diodes, with trr = 100ns or more is not recommended ; The photographs in fig. 25 show the effects on the power current and on the voltage on pin 2, due to the diodes showing different speeds. Diodes showing trr greater than 35-50ns will reduce the overall efficiency of the system, increasing the power dissipated by the device.

The third component requiring care is the inductor. Fig. 22a shows the part numbers of some types used for testing. Besides having the required inductance value, the coil has to show a very high saturation current.

Therefore, a correct dimensioning requires a saturation current above the maximum value of I_{2L}, the current limit threshold.

To achieve high saturation with ferrite cores an air gap between the two core halves must be provided ; the air gap causes a leakage flux which is radiated in the surrounding space. To better limit this phenomenon "pot cores" may be used, whose geometry is such to better limit the flux radiated to the outside.

Using toroidal cores, for instance of Magnetic 58930-A2 moly-permalloy kind, both the requirements of high saturation and low leakage flux are satisfied. The saturation is softer that the saturation shown by the ferrite materials. The air gap is not concentrated in one area, but is finely distributed along the whole core ; this gives the low leakage flux value.

Careful selection of the external components therefore allows the realization of a power supply system whose benefits are significant when compared to a system with the same performance but realized with the linear technique.

Figure 24 : Typical Impedance/Frequency curves for EKR Capacitors.

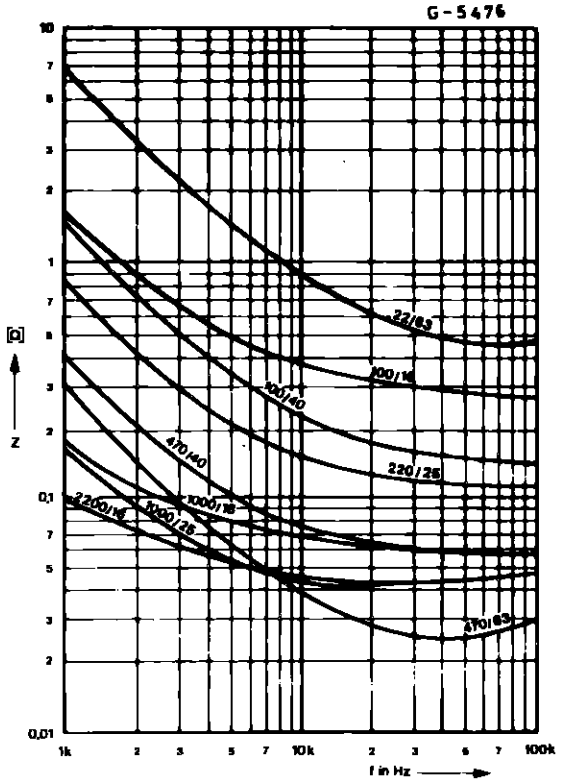
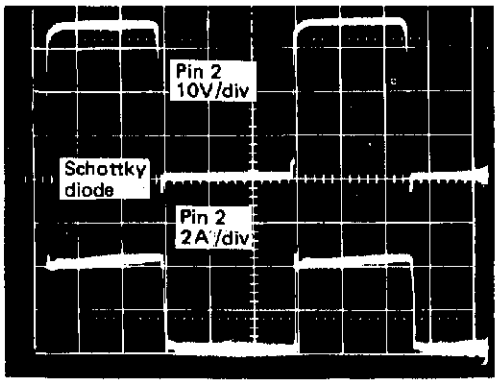
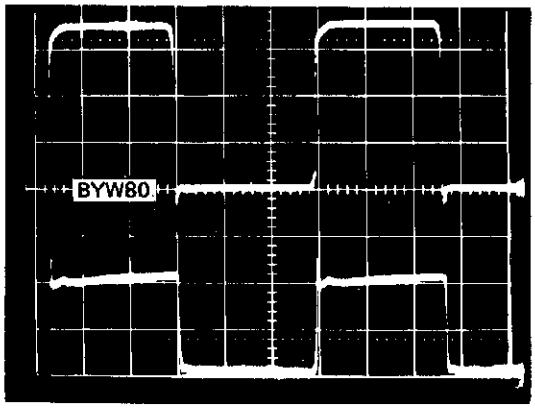
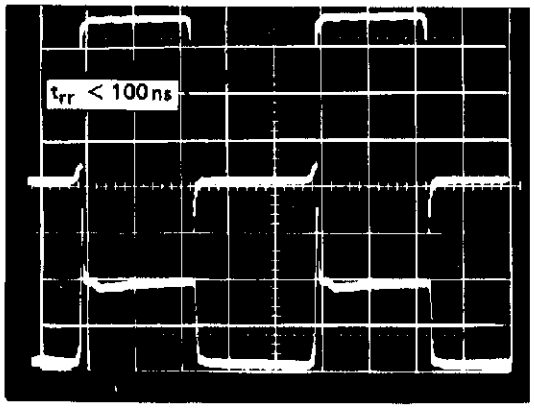


Figure 25 : Oscilloscope Photographs Showing the Waveform obtained with Diodes having Different t_{rr} Values.



t : 2μs/div





t: 2μs/div

LOW COST APPLICATION AND PRE-REGULATOR

Fig. 26 shows the low cost application of a 4A and V_o = 5.1V power supply. A minimum amount of essential external components is required, which are necessary for correct operation. It is impossible to save other components, specially the soft-start capacitor. Without soft-start, the system cannot reach the steady state and there is also a serious risk of damaging the device.

This application is very well suited not only as a low-cost power supply, but also as pre-regulator for post-regulators distributed in different circuit points, or even on different boards (fig. 27). The post-regulators may be selected among the low-drop types, like L4805 and L387 for example, still obtaining a high efficiency, combined with an excellent regulation. The use of L387 device allows us to use also the reset function, useful to power a microprocessor.

SWITCHING vs LINEAR

Switching regulators are more efficient than linear types so the transformer and heatsink can be smaller and cheaper. But how much can you gain ?

We can estimate the savings by comparing equivalent linear and switching regulators. For example, suppose that we want a 4 A/5 V supply.

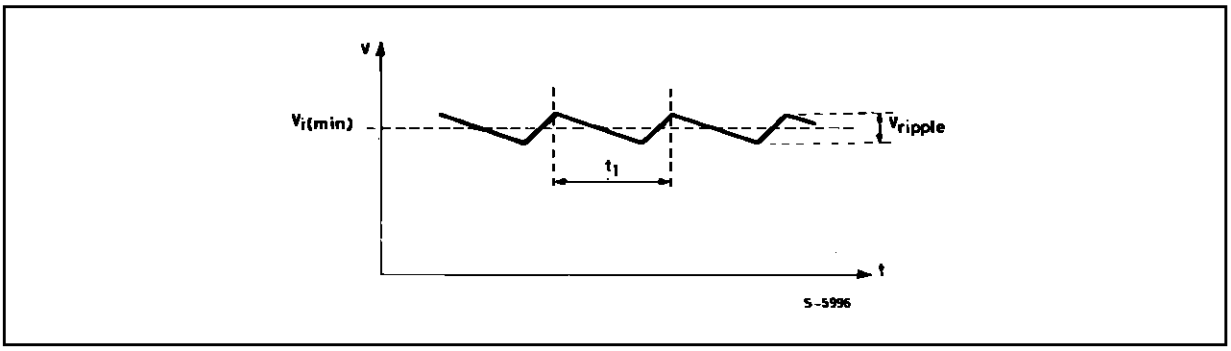
Linear

For a good linear regulator the minimum dropout will be at least 5V at 4A. The minimum input voltage is given by :

$$V_{i\,min} = V_o + V_{drop} + \frac{1}{2} V_{ripple}$$

where :

$$V_{ripple} \cong \frac{I_o\, t_1}{C} = \frac{4 \times 8 \times 10^{-3}}{10 \times 10^{-3}} = 3.2\ V$$



(a good approximation is 8ms for t_1 at mains frequency of 50Hz and 10.000µF for C, the filter capacitor after the bridge). Therefore $V_{imin} \cong 1.6V$. Since operation must be guaranteed even when the mains voltage falls 20%, the nominal voltage on load at the terminals of the regulator must be :

$$V_{nom} = \frac{V_{i\,min}}{0.8} = \frac{10.6}{0.8} = 13.25V$$

To allow even a small margin we have to choose :

$V_{nom} = 14V$

The power that the series element must dissipate is therefore :

$P_d = (V_{nom} - V_o)\, I_o = 36W$

and a heatsink will be necessary with a thermal resistance of :

$R_{th\ heats.} = 0.8°C/W$

and the transformer must supply a power of :

$P_{diss} = 14 \times 4 = 56W$

It must therefore be dimensioned for :

$$PD = \frac{56}{0.9} = 62VA$$

Switching (L296)

Assuming the same nominal voltage (14V), the L296 data sheet indicates that the power dissipated in this case is only 7W. And this power is dissipated in two elements ; the L296 itself and the recirculation diode.

It follows that the transformer must be roughly 30VA and the heatsink thermal resistance about 11°C/W.

	+Linear	+Switching
Transformer	62 VA	30 VA
Heat sink	0.8 °X/W	11 ∫X/W

This comparison shows that the L296 switching regulator allows a saving of roughly 50% on the cost of the transformer and an impressive 80-90% on the cost of the heatsink. Considering also the extra functions integrated by the L296 the total cost of active and passive components is roughly the same for both types.

Finally, it is important to note that a lower power dissipation means that the ambient temperature in the regulator enclosure can be lower - particularly when the circuit is enclosed in a box - with all the advantages cooler operation brings.

Figure 26 : A Minimal Component Count 5.1V / 4A Supply.

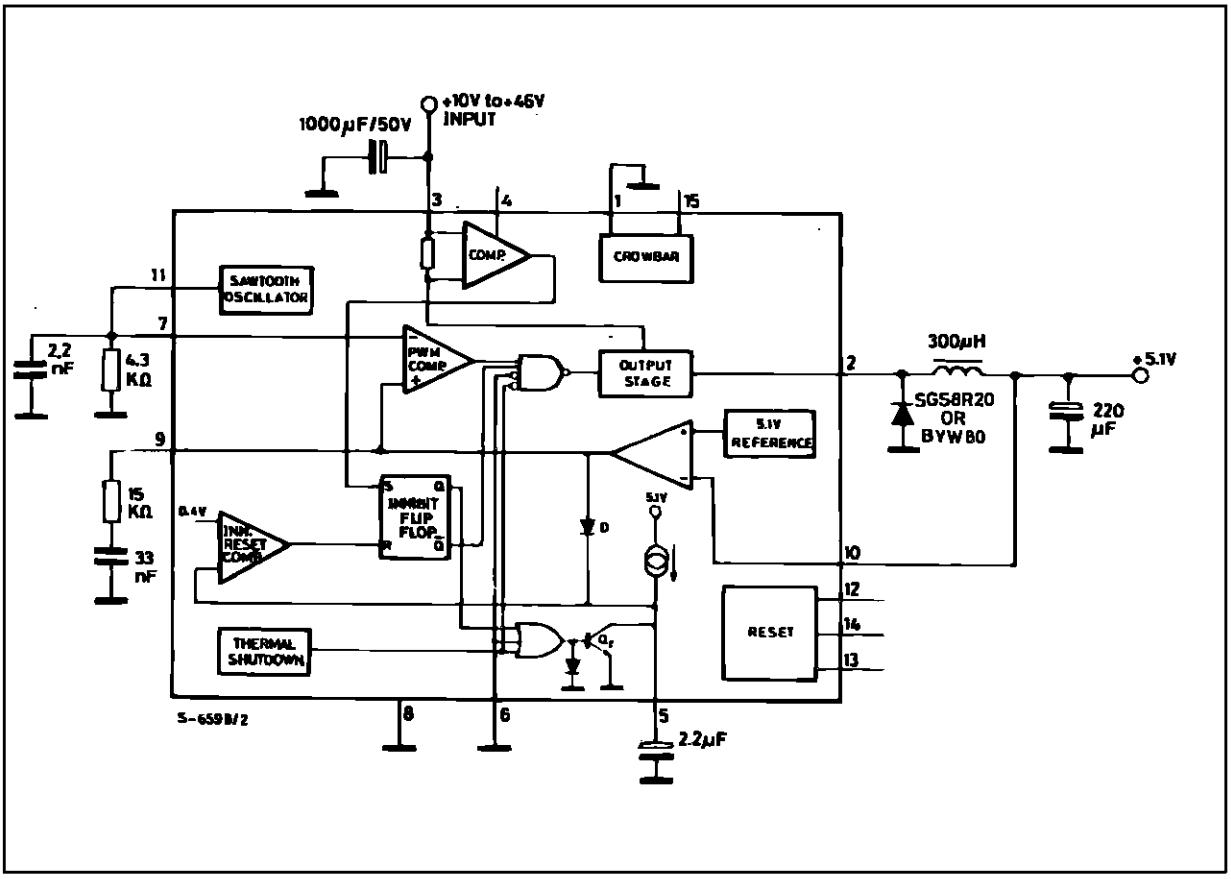
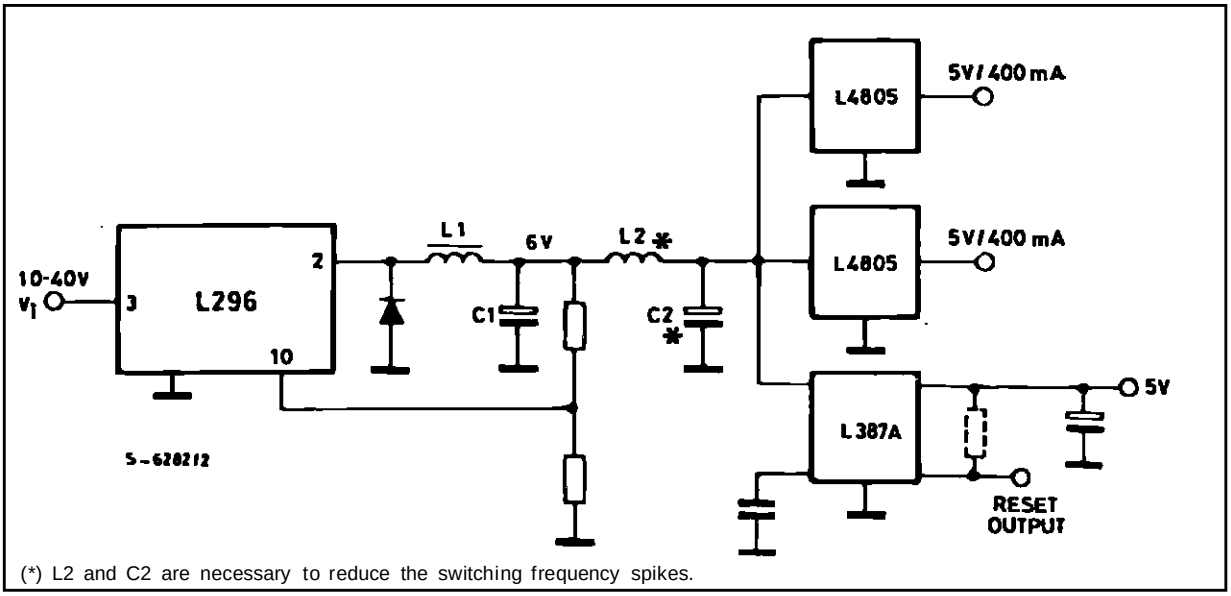


Figure 27 : The L296 may also be used as a preregulator in distributed supply systems.



(*) L2 and C2 are necessary to reduce the switching frequency spikes.

If for some reason it is necessary to use higher supply voltages the switching technique, and hence the L296, becomes even more advantageous.

POWER SUPPLY COMPLETE WITH TRANSFORMER

Fig. 28 shows a power supply complete of transformer, bridge and filter, with regulation on the output voltage from 5.1V to 15V.

As already stated above, the output capacitors have to show some speciale features, like low ESR and high current ripple, to obtain low voltage ripple values and high reliability. The input filter capacitors must not be neglected because they have to show excellent features, too, having to supply a pulsed current, required by the device at the switching frequency. The current ripple is rather high, greater than the load current. For this application, two parallel connected 3300µF/50V EYF (ROE) capacitors have been used.

POWER SUPPLY WITH MAINS SWITCHING PREREGULATOR

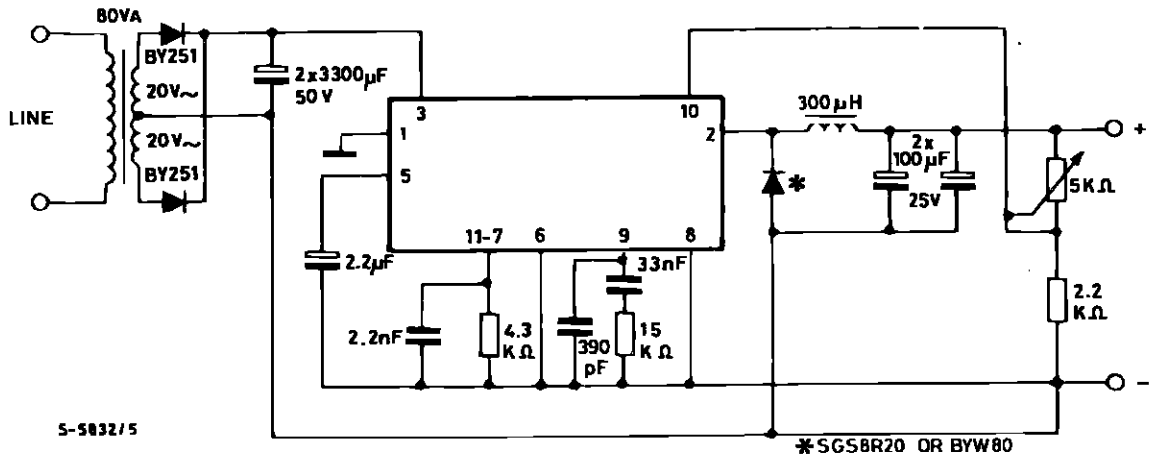
When it is desirable to eliminate the 50/60Hz transformer - in portable or volume-limited equipment-a mains preregulator can be added to reduce the input voltage to a level acceptable for the L296.

In this case the pre-regulator circuit is connected to the primary of the transformer which now operates at the switching frequency and is therefore smaller and lighter.

Using a UC3840 which includes the feed-forward function it is possible to compensate mains variation within wide limits. The secondary voltage is therefore only affected by load variations. Using one or more L296s as postregulators, feedback to the primary is no longer necessary, reduces the complexity and cost of the transformer which needs only a single secondary winding.

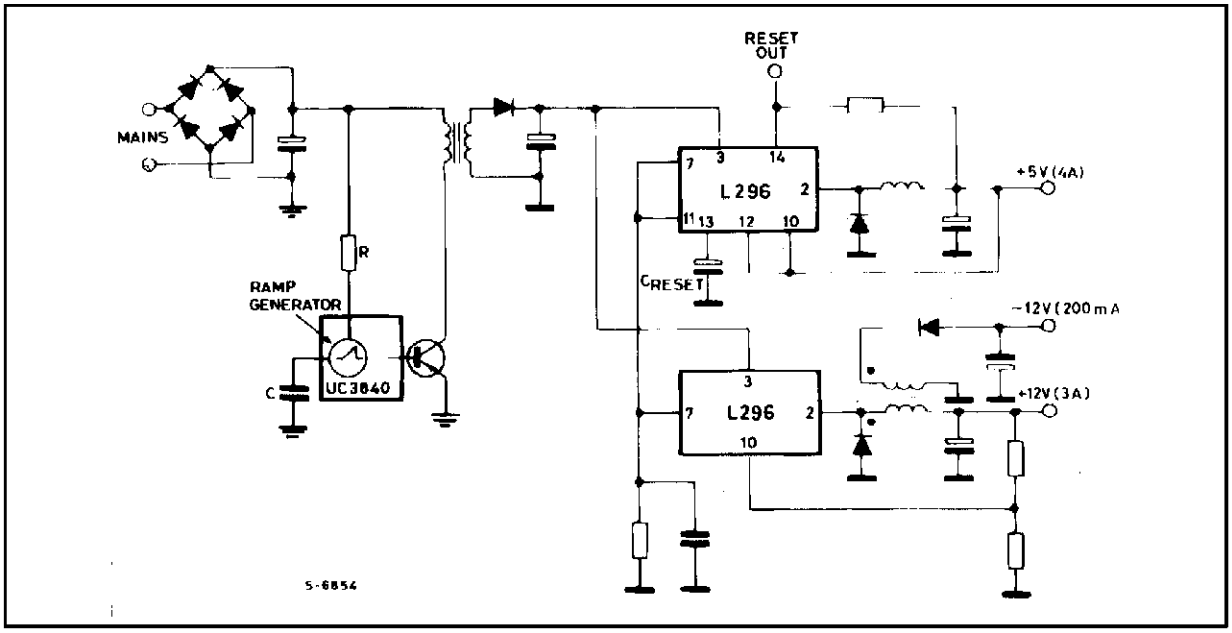
Fig. 28A shows a multi-output supply with a mains preregulator.

Figure 28 : A Typical Variable Supply showing the Mains Transformer.



V_o = 5.1 to 15V
I_o = 4A max. (min. load current = 100mA)
ripple ≤ 20mV
load regulation (1A to 4A) = 10mV (V_o = 5.1V)
line regulation (200V ± 15% and to I_o = 3A) = 15mV (V_o = 5.1V)

Figure 28A: A Multiple Output Supply using a Switching Preregulator rather than a Mains Trans-



POWER SUPPLY WITH 0 - 30V ADJUSTABLE VOLTAGE

When output voltages lower than 5V are required, the circuit shown in fig. 29 may be used.

Calibration is performed by grounding the P1 slider. Acting on P2, the current which flows through the 10kW resistor is fixed approximately 2.5mA to obtain an output voltage of 30V. The equivalent circuit is shown in fig. 30.

Acting now on the slider of P1, the current flowing through the divider may be varied. The new equivalent circuit is shown in fig. 31.

Reducing the current flowing, also the voltage drop across the 10kΩ resistance is reduced, together with V_O. When the current reaches zero, it follows that $V_O = V_{REF}$. When the voltage on the slider of P1 exceeds V_{REF}, the current start to flow in opposite direction and V_O begins to decrease below 5V.

When $I_1 \times 10k\Omega = V_{REF}$ it follows that $V_O = 0$.

DUAL OUTPUT REGULATOR

The application shown in fig. 32 is specially interesting because it provides two output voltages. The first voltage, the main one, is directly controlled by the feedback circuit. The second voltage is obtained through an auxiliary winding.

It often happens, when microprocessors, logic devices etc., have to be power supplied, that a main 5V output and an auxiliary +12V or –12V output are required, the latter with lower current requirements (100 to 200mA) and a stabilization level not excessively high. As the auxiliary power supply is obtained through a completely separated winding, it is possible to obtain either a positive or negative voltage (compared to the main voltage or also a completely isolated voltage. With V_i variable between 20V and 40V, V_O = 5.1V and I_O = 2.5A, the auxiliary -12V/0.2A voltage is within a ±2% tolerance.

Figure 29: Variable 0-30V supply illustrating how output voltages below 5.1V are obtained.

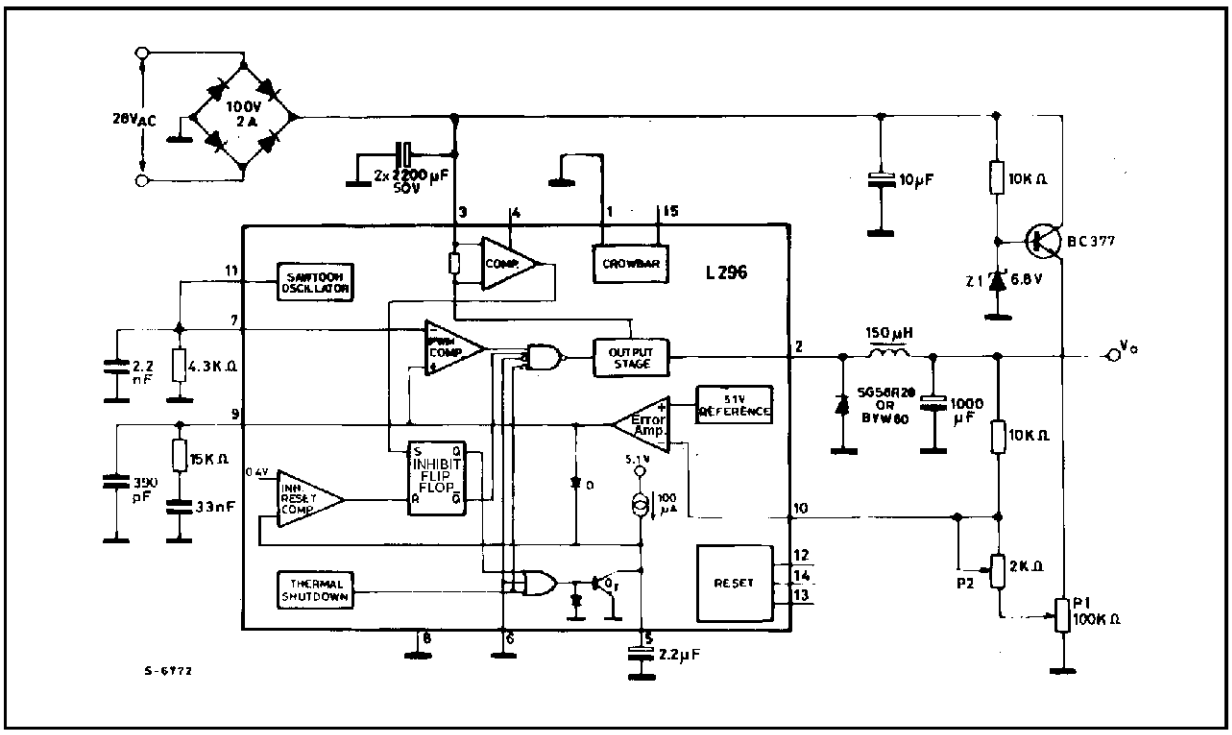


Figure 30: When setting up the figure 29 circuit the slider of P1 is grounded, giving the equivalent circuit shown here, and P2 adjusted to give an output voltage of 30V.

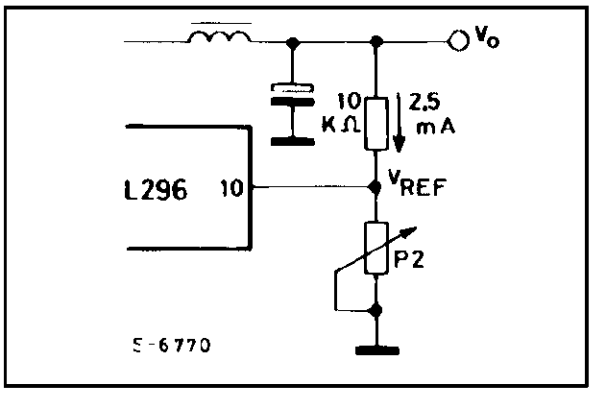


Figure 31: Partial Schematic showing Output Voltage Adjustment of Figure 29.

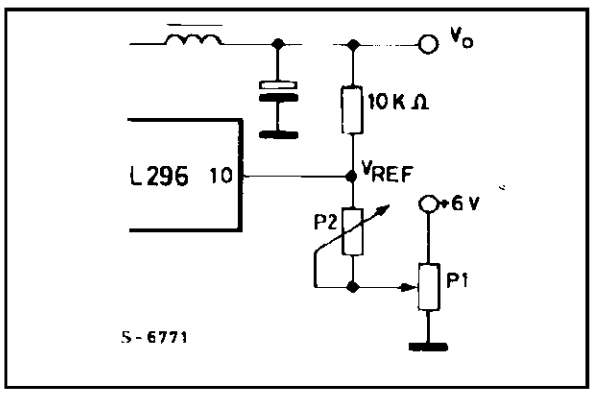
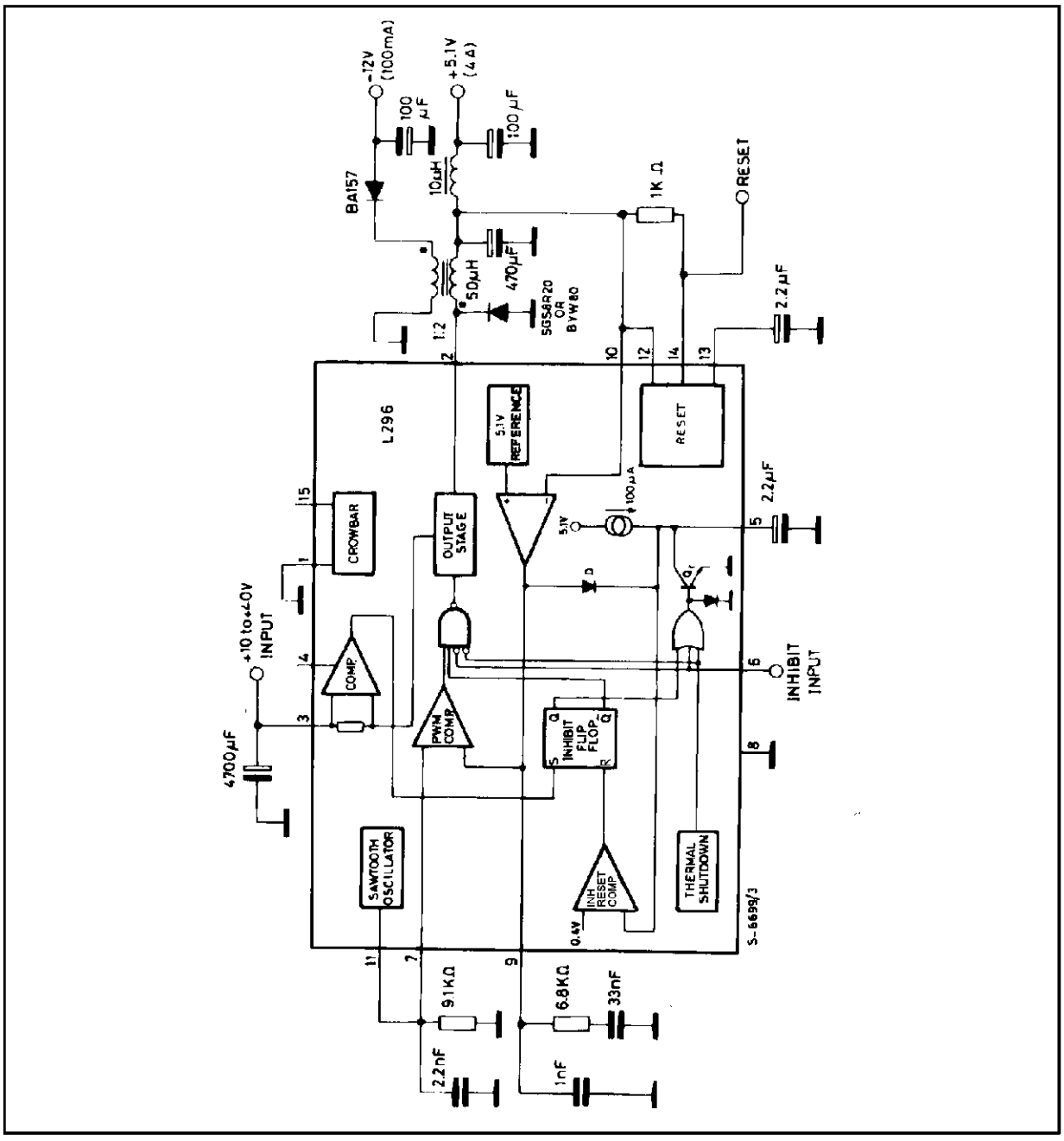


Figure 32: Dual output regulator showing how an additional winding can be added to the inductor to generate a secondary output.



PERSONAL COMPUTER POWER SUPPLY

Using two mutually synchronized devices it is possible to obtain a four output power supply suitable for power a microprocessor system.

V_{01} = 5.1V/4A

V_{02} = 12V/2.5A (up to 4A)

V_{03} = –5V/0.2A

V_{04} = –12V/0.2A

The schematic diagram is shown in fig. 33. The 5V output is also provided with the reset function, that is available also for the 12V output.

Figure 33: Microcomputer Supply with 5V, –5V, 12V and –12V Outputs.

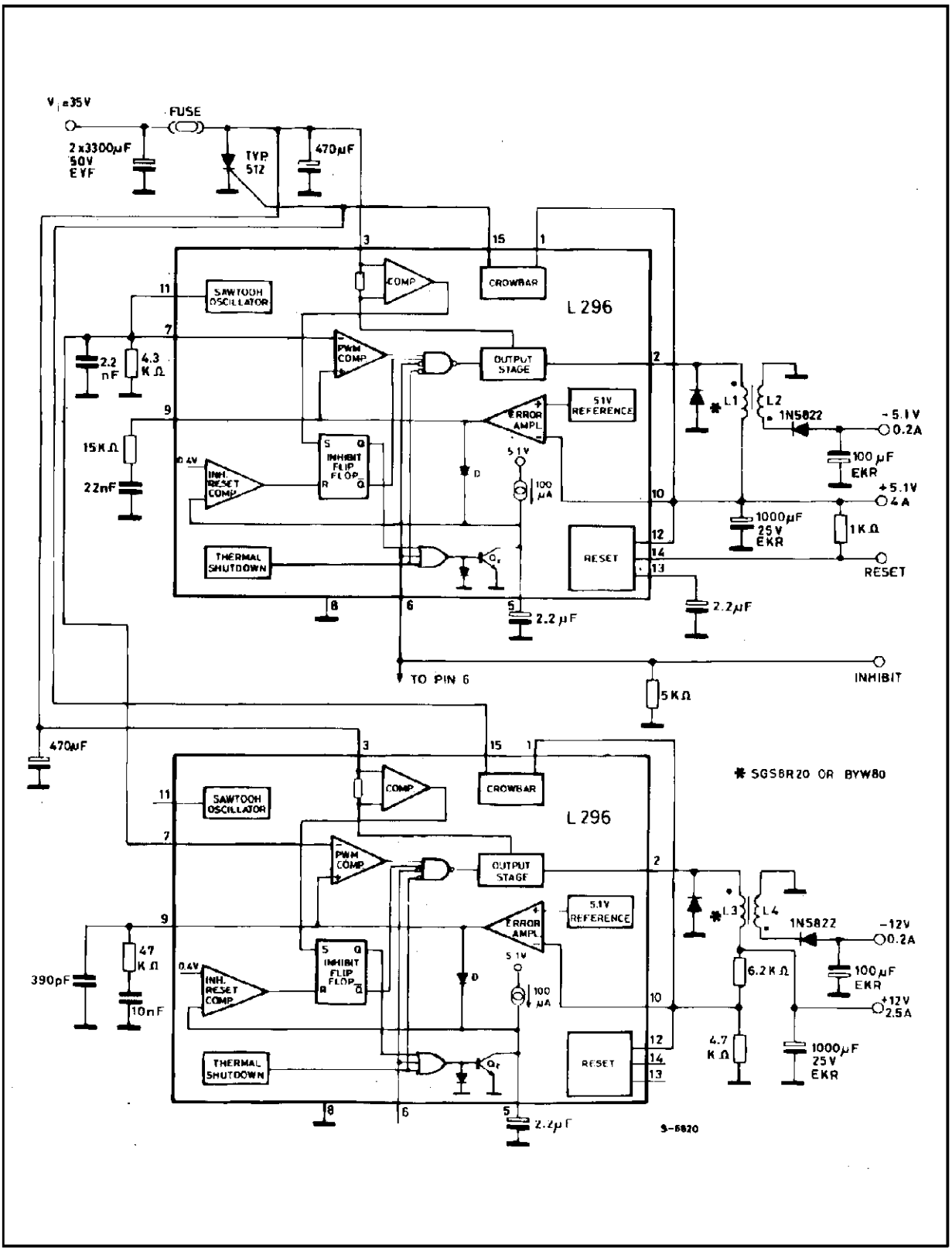
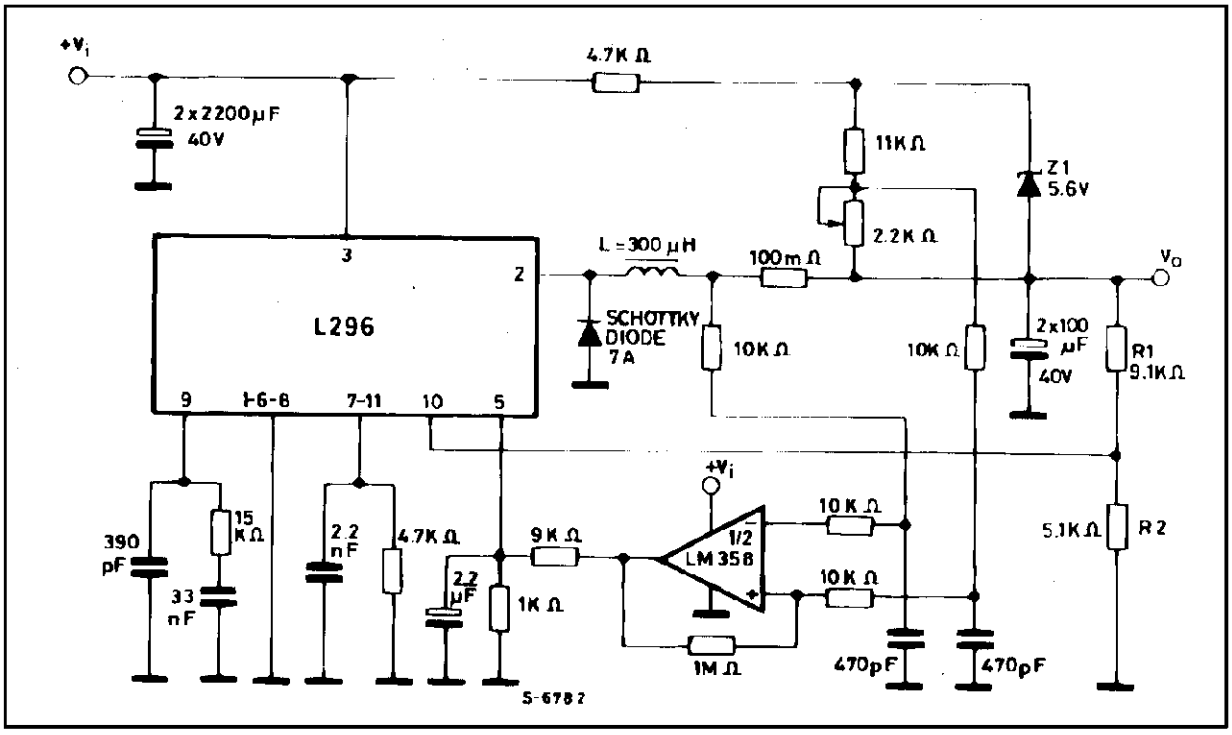


Figure 34: Battery charger circuit illustrating how the device is used to regulate the output current.



The feedback is direct, no other external component is used and no calibration is therefore required. An output is obtained with the accuracy of the reference voltage (±2%). For the 12V output, by using a resistive divider with 1% resistance an output is obtained whose spread is within ±4%.

The two devices are mutually synchronized not to give rise to intermodulation which could generate unpleasant noise and, at the same time, a further component saving is achieved.

The crowbar function is implemented on both 5V and 12V outputs, using a single SCR connected to the input. The latter, by discharging to ground the electrolytic filter capacitors, blows the fuse connected in series with the devices power supply. In this way, should a faulty be present on either of the main outputs, the supply is switched off for whole system.

To inhibit both the devices with a single input signal, it is possible to connect the two inhibit inputs (pin 6) together; the 5kΩ resistance is used when the inhibit input is left open. If this input is not used it must be grounded.

As may be noted in the diagram, to obtain the two auxiliary voltages is very simple and cost-effective.

It is suggested that the diodes are fast types (trr < 50ns); should slower diodes be required some more turns have to be added to the auxiliary winding.

BATTERY CHARGER

When the device has to be used as current generator it is necessary to avoid the internal current limiter is operated fig. 34 shows the circuit realizing constant current limitation. In this way it is possible to obtain a 6V, 12V and 24V battery charger. For each of these voltages a max. current of 4A is available, which is large enough for batteries up to 40-45Ah (for 12V type). With reference to the electric diagram through the 2kΩ potentiometer the max. output current is set, while through the R1 – R2 output divider the voltage is set. (R1 may be replaced by either a potentiometer or a 3 position switch, to directly obtain the three 6V, 12V and 24V voltages).

HIGHER INPUT VOLTAGE

Since a maximum input voltage of 46V (operating value) may be applied to the device the diagram shown in fig. 35 may be used when it is necessary to exceed this limit.

This system is particularly useful when operating at low output voltages. In this case a mean current I_{iDC} which has a low value when compared to I_O is obtained. In fact, since $V_o = V_i (T_{ON}/T)$ and $V_o I_o = V_i I_{iDC}$ (assuming the device has an ideal efficiency), it follows that $I_{iDC} = I_O (T_{ON}/T)$.

Assuming to be:

V_o = 5V I_o = 4A and V3 ≈ 37V

it follows that:

$$T_{ON}/T = V_o / V_i = \frac{5}{37} = 0.135$$

I_{iDC} = 4 x 0.135 = 0.54A.

With input voltage 50V and I_o = 4A, the external transistor dissipates about 7W. High good efficiency is still achieved, around 74%; in the real case, considering also the device losses, an efficiency around 62% is achieved.

During output short circuits the external transistor is not overloaded because in this condition I_{iDC} reduces to values lower than 100mA. It is not possible to realize this application with series post-regulator because the efficiency would be unacceptable low.

MOTOR CONTROL

The L296 is also suitable for use in motor controls applications. Fig. 36 shows how to use the device to drive a motor with a maximum power of about 100W and provided with a tachometer generator for a good speed control.

Figure 35: The maximum input voltage can be raised above 46V by adding a transistor as shown here.

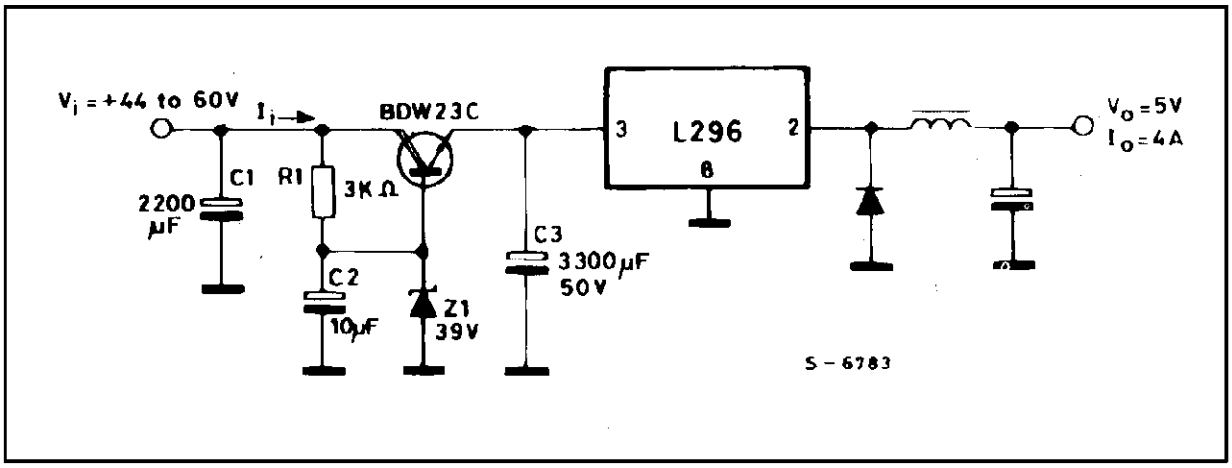
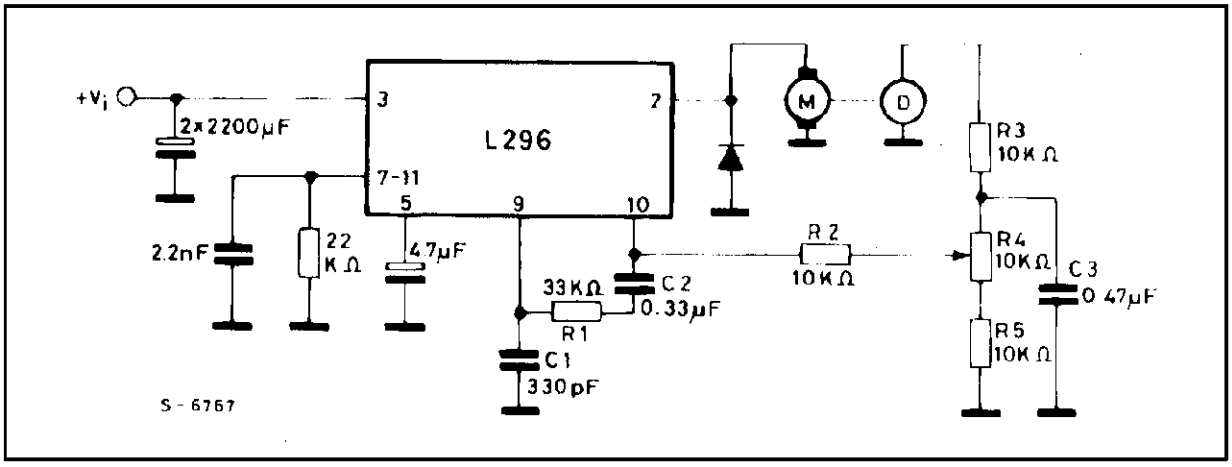


Figure 36: With a tacho dynamo supplying feedback the L296 can be used as a motor speed controller.



HIGHER CURRENT REGULATORS

It is possible to increase the output current to the load above 4A through the use of an external power transistor. Fig 37 shows a suitable circuit. The frequency is around 40kHz to prevent the device from loosing excessive power due to switching on the external power.

The circuits shown in fig. 38 and fig. 39 show how current limitation may be realized in two different ways: through a sensing resistor connected in series with the collector of the external power transistor or through a current transformer.

In the first case, the sensing resistor is a low value resistor able to withstand the maximum load current required. The V_{CE} of the power transistor is higher than its V_{CEsat}; when the resistor is connected in series to the collector V_{CE} is reduced; consequently since the overall dissipated power is constant, the power dissipated by the sensing resistor is subtracted from that dissipated by the power transistor.
The values indicated in figs. 38 and 39 realize adjustable current limitation for load currents around 10A.

Figure 37: The output current may be increased by adding a power transistor as shown in this circuit.

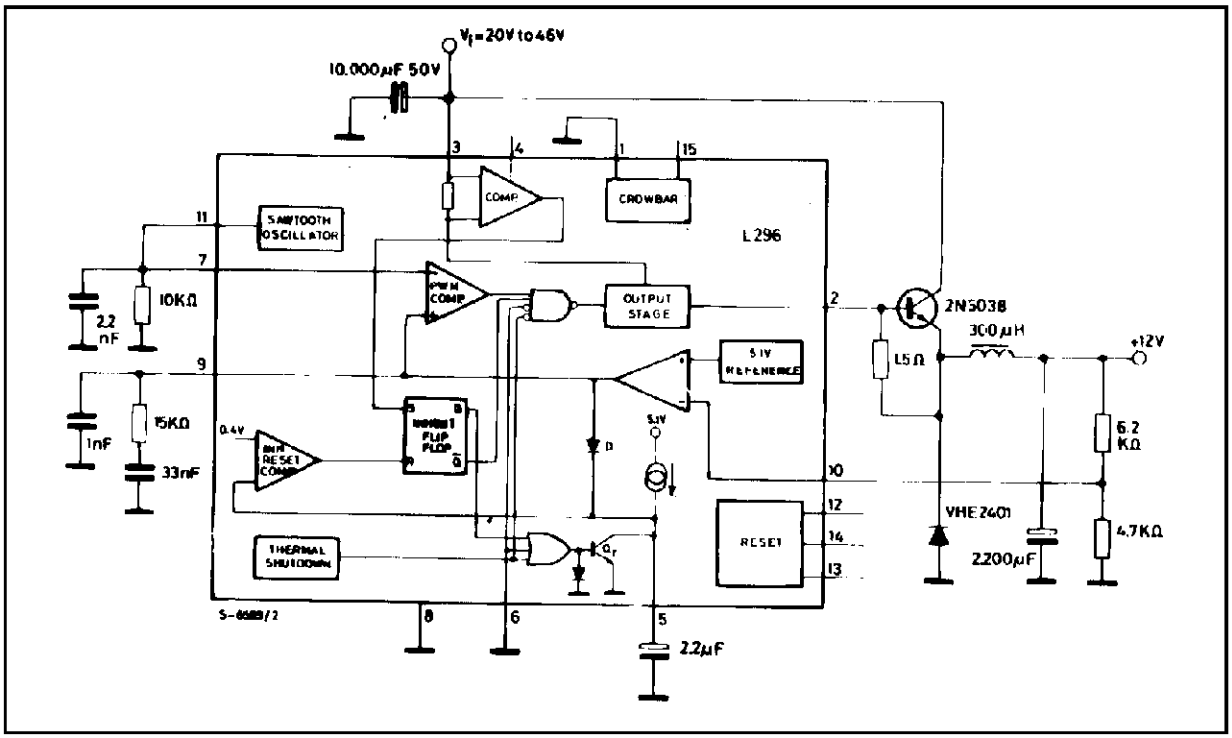


Figure 38: This circuit shows how current limiting for the external transistor is obtained with a sensing resistor.

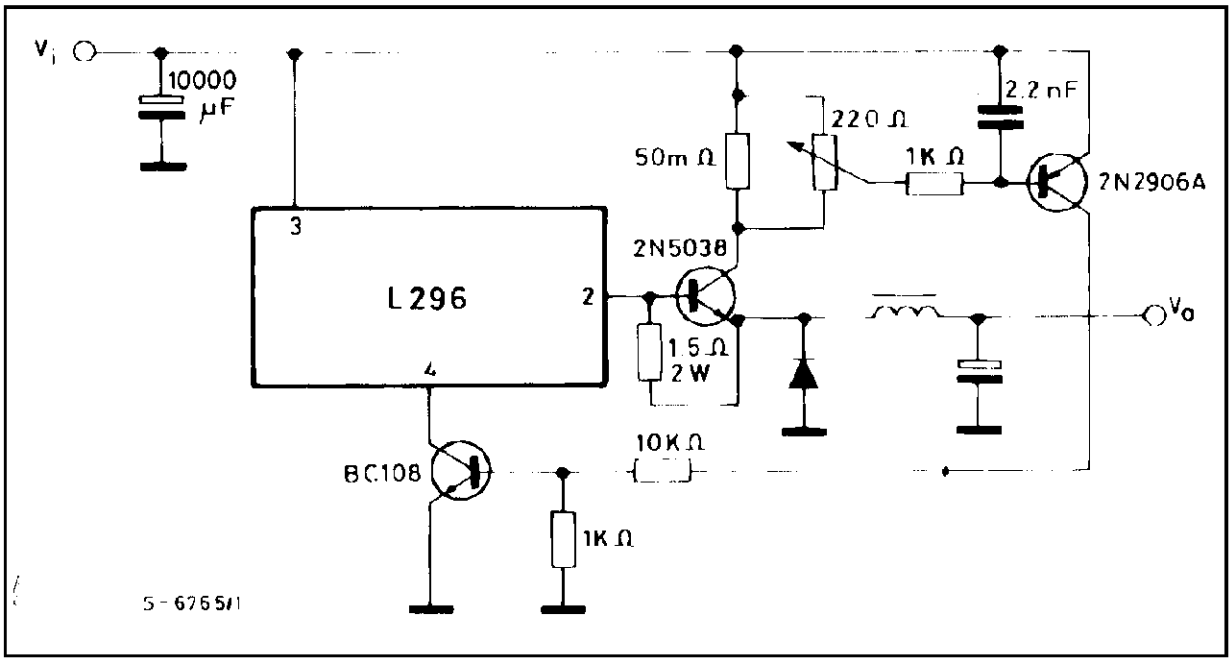


Figure 39: A small transformer is used in this example for current limiting.

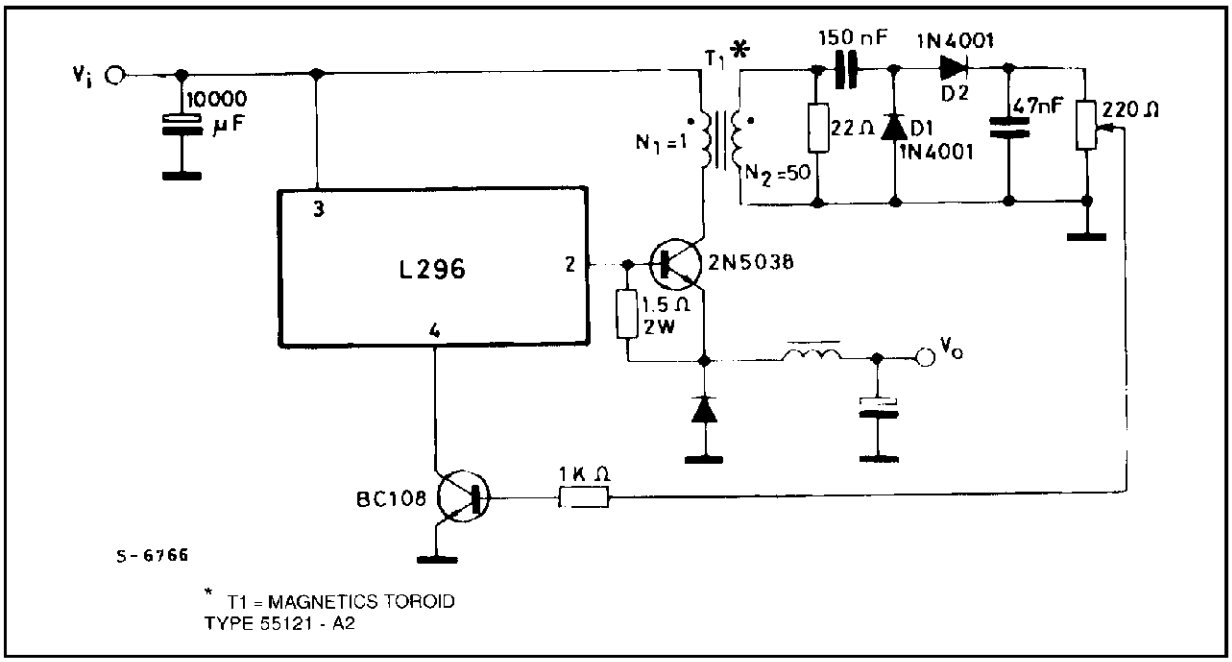
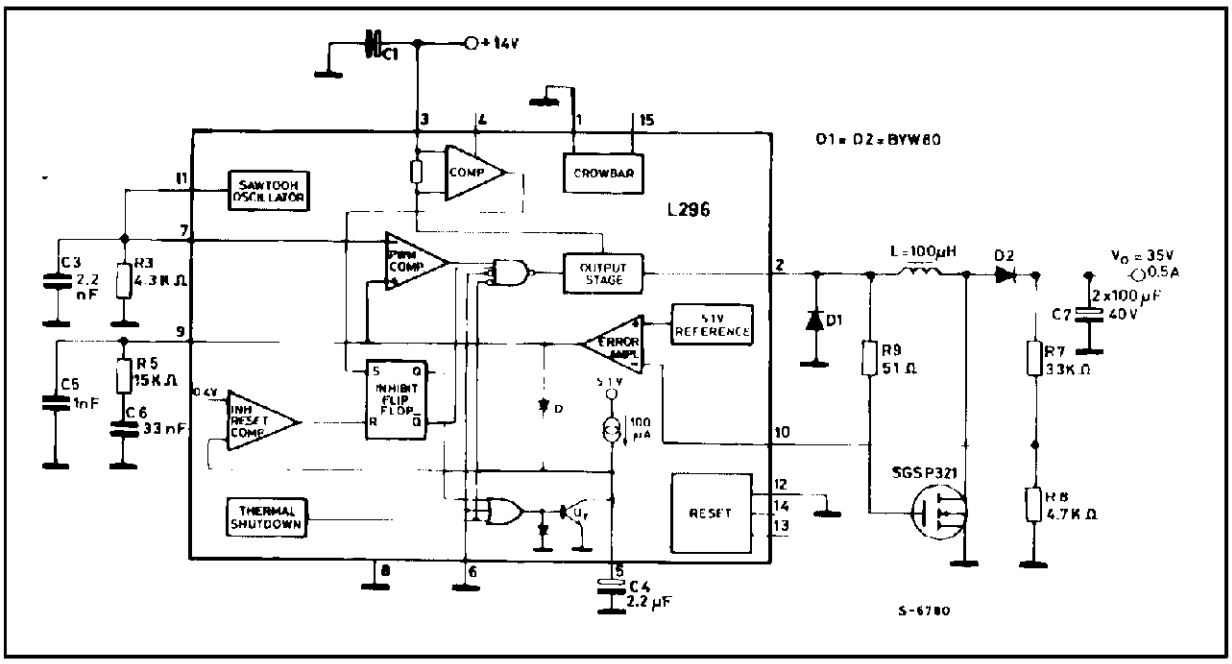


Figure 40: A step-up Converter using a Power MOS Transistors.



STEP-UP CONVERTER

With the L296 it is also easy to realize a step-up converter, by using a MOS power transistor. Fig. 40 shows the electric diagram of the step-up converter. The frequency is 100kHz, operation is in discontinuous mode and the device internal current limiter is used. Therefore no other external protection is required.

The input voltage could be a 12V car battery, from which an output voltage of 35V may be obtained. Lower output voltage of 35V may be obtained. Lower output voltage values may be obtained by reducing the value of R7.

DESCRIPTION OF OPERATION

Fig. 41 shows the diagram of the circuit realizing the step-up configuration.

When the transistor Q1 is ON, the inductance L charges itself with a current given by:

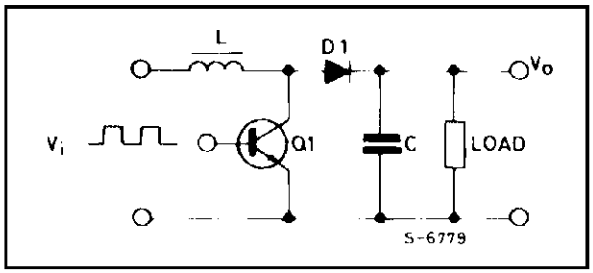
$$i_L = \frac{V_i}{L} t$$

The peak current in the coil is:

$$I_{peak} = \frac{V_i}{L} T_{ON}$$

In this configuration, unlike the step-down configuration, the peak current is not strictly related to the load current. The energy stored in the coil is successively discharged across the load when the transistor switches OFF. To calculate the I_o load current, the following procedure may be used:

Figure 41: Basic Schematic for Step-up Configurations.

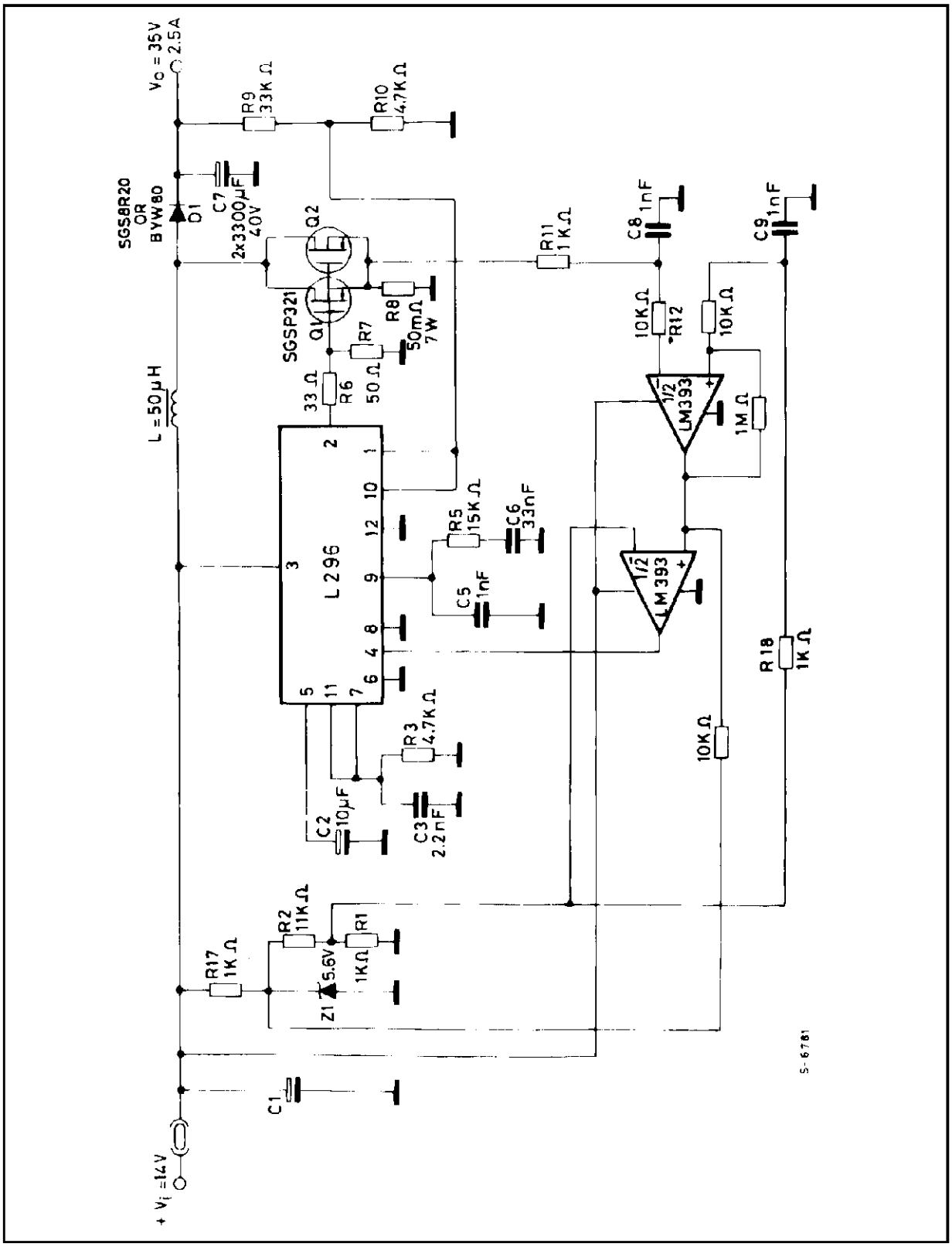


$$\frac{1}{2} L I^2 peak = V_o I_o T$$

$$I_o = \frac{L I^2 peak}{2 V_o T} = \frac{V_i^2 T_{ON}^2}{2 L V_o T}$$

For a greater output power to be available, the internal limitation must be replaced by an external circuit to protect the external power devices and to limit the current peak to a convenient value. A dual comparator (LM393) with hysteresis is used to avoid uncertaintes when the current limitation operates. The electric diagram is shown in fig. 42.

Figure 42: High power step-up converter showing how the current limiting function is realized externally.



LAYOUT CONSIDERATIONS

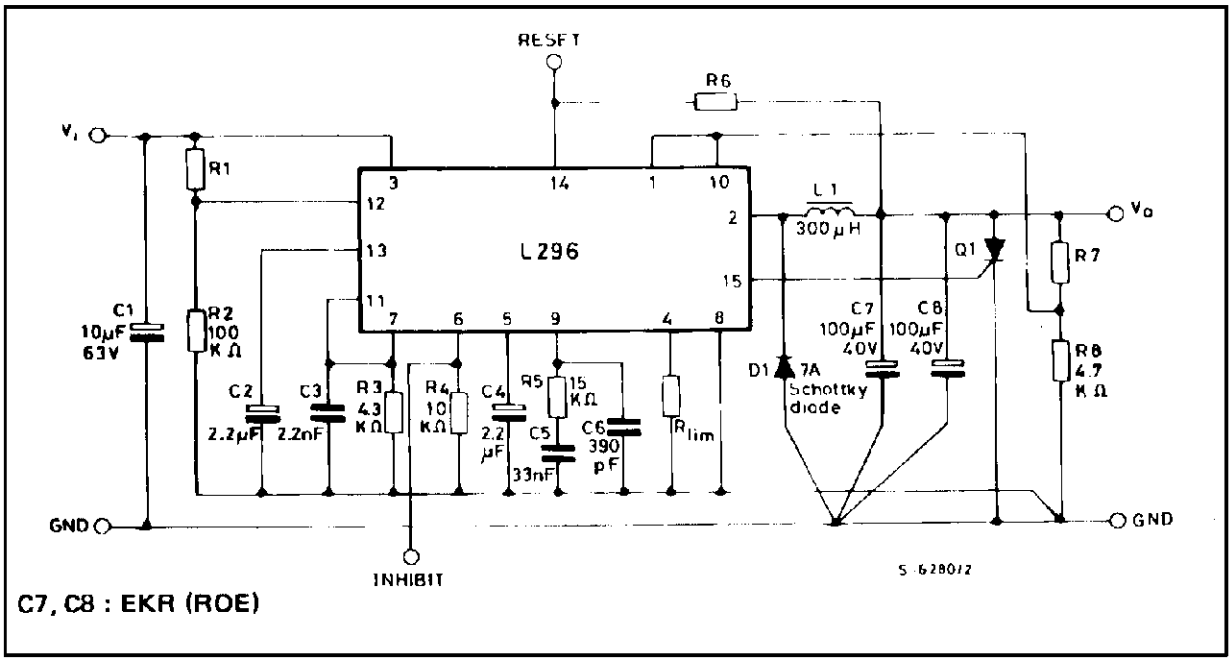
Both for linear and switching power supplies when the current exceeds 1A a careful layout becomes importantto achieve a good regulation. The problem becomes more evident when designing switching regulators in which pulsed currents are over imposed on dc currents. In drawing the layout, therefore, special care has to be taken to separate ground paths for signal currents and ground paths for load currents, which generally show a much higher value.

When operating at high frequencies the path length becomes extremely important. The paths introduce distributed inductances, producing ringing phenomena and radiating noise into the surrounding space.

The recirculation diode must be connected close to pin2, to avoid giving rise to dangerous extra negative voltages, due to the distributed inductance.

Fig. 43 and fig. 44 respectively show the electric diagram and the associated layout which has been realized taking these problems into account. Greater care must be taken to follow these rules when two or more mutually synchronized devices are used.

Figure 43: Typical application circuit showing how the signal and power grounds are connected.



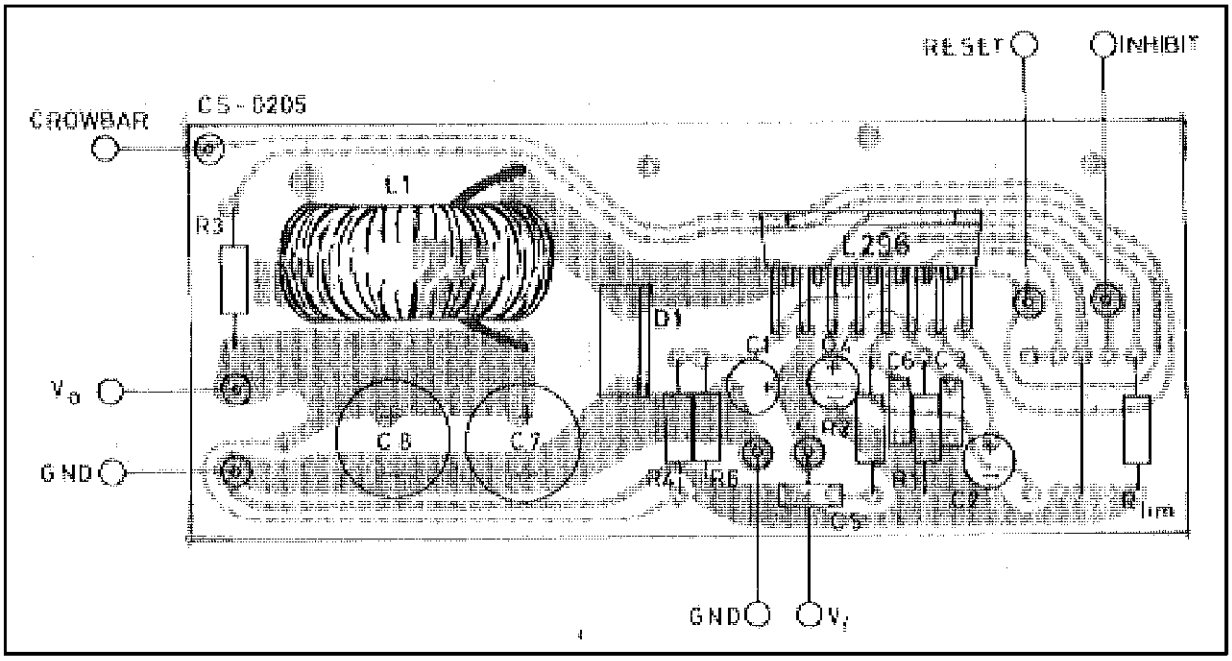
SUGGESTED INDUCTOR (L1)

Core Type	No. Turns	Wire Gauge	Air Gap
Magnetics 58930 - A2MPP	43	1.0mm.	
Thomson GUP 20 x 16 x 7	65	0.8mm.	1mm.
Siemens EC 35/17/10 (B6633 & - G0500 - x 127)	40	2 x 0.8mm.	
VOGT 250µH Toroidal Coil, Part Number 5730501800			

Resistor Value for Standard Output Voltages

V_o	R8	R7
12V	4.7kΩ	6.2kW
15V	4.7kΩ	9.1kΩ
18V	4.7kΩ	12kΩ
24V	4.7kΩ	18kΩ

Figure 44: A Suitable PCB Layout for the Figure 43 Circuit realized in Accordance with the Suggestions in the Text (1:1 scale).



HEATSINK DIMENSIONING

The heatsink dissipates the heat produced by the device to prevent the internal temperature from reacing values which could be dangerous for device operation and reliability.

Integrated circuits in plastic package must never exceed 150°C even in worst conditions. This limit has been set because the encapsulating resin has problems of vitrification if subjected to temperatures of more than 150°C for long periods or of more than 170°C for short periods. In any case the temperature accelerates the ageing process and therefore influences the device life; an increase of 10°C can halve the device life. A well designed heatsink should keep the junction temperature between 90°C and 110°C. Fig. 45 shows the structure of a power device. As demonstrated in thermo-dynamics, a thermal circuit can be considered to be an electrical circuit where R1, R2 represent the thermal resistance of the elements (expressed in °C/W) (see fig. 46).

C1,C2	are the thermal capacitance (expressed in °C/W)
I	is the dissipated power
V	is the temperature difference with respect to the reference (ground)

This circuit can be simplified as shown in fig. 47, where:

C_C	is the thermal capacitance of the die plus that of the tab.
C_h	is the thermal capacitance of the heatsink
R_{jc}	is the junction case thermal resistance
R_h	is the heatsink thermal resistance

Figure 45.

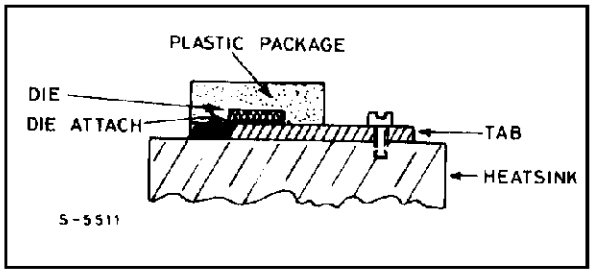


Figure 46.

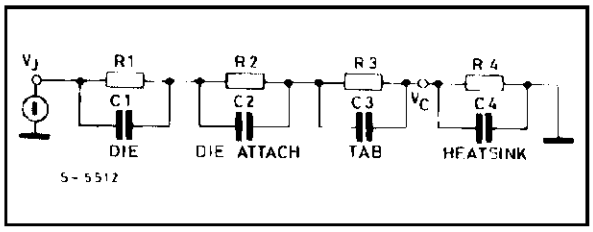
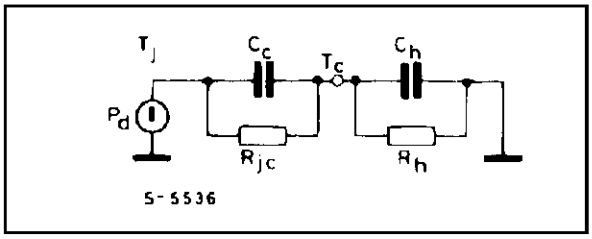
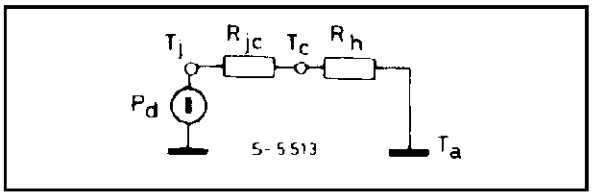


Figure 47.



But since the aim of this section is not that of studing the transistors, the circuit can be further reduced as shown in figure 48.

Figure 48.



If we now consider the ground potential as ambient temperature, we have:

$$T_j = T_a + (R_{jc} + R_h)P_d \quad a)$$

$$R_h = \frac{T_j - T_a - R_{jc}\,P_d}{P_d} \quad b)$$

$$T_c = T_a + R_h\,P_d \quad c)$$

Thermal contact resistance depends on various factors such as the mounting, contact area and planarity of the heatsink. With no material between thedevice and heatsink the thermal resistance is around 0.5°C/W; with silicone grease roughly 0.3°C/W and with silicone grease plus a mica insulator about 0.4°C/W. See fig. 49.

In application where one external transistor is used together, the dissipated power must be calculated for each component. The various junction temperature can be calculated by solving the circuit shown in fig. 50.

This applies if the dissipating elements are fairly close with respect to the dissipator dimensions, otherwise the dissipator can no longer be considered as a concentrated constant and the calculation becomes difficult.

This concept is better explained by the graph in fig. 51 which shows the case (and therefore junction) temperature variation as a function of the distance between two dissipating elements with the same type of heatsink and the same dissipated power.

Th graph in Fig. 51 refers to the specific case of two elements dissipating the same power, fixed on a rectangular aluminium plate with a ratio of 3 between the two sides.

The temperature jump will depend on the total dissipated power and on the total dissipated power and on the devices geometrical positions. We want to show that there exists an optimal position between the two devices:

Figure 49.

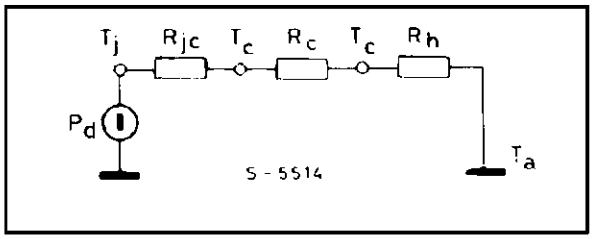
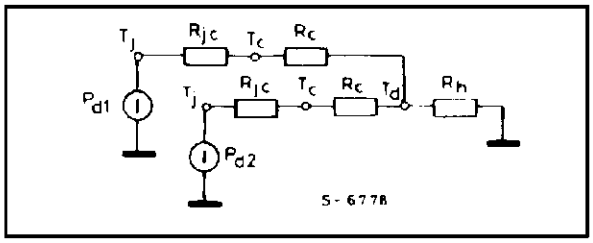


Figure 50.



$d = \frac{1}{2} \cdot$ side of the plate.

Fig. 52 shows the trend of the temperature as a function of the distance between two dissipating ele-

Figure 51.

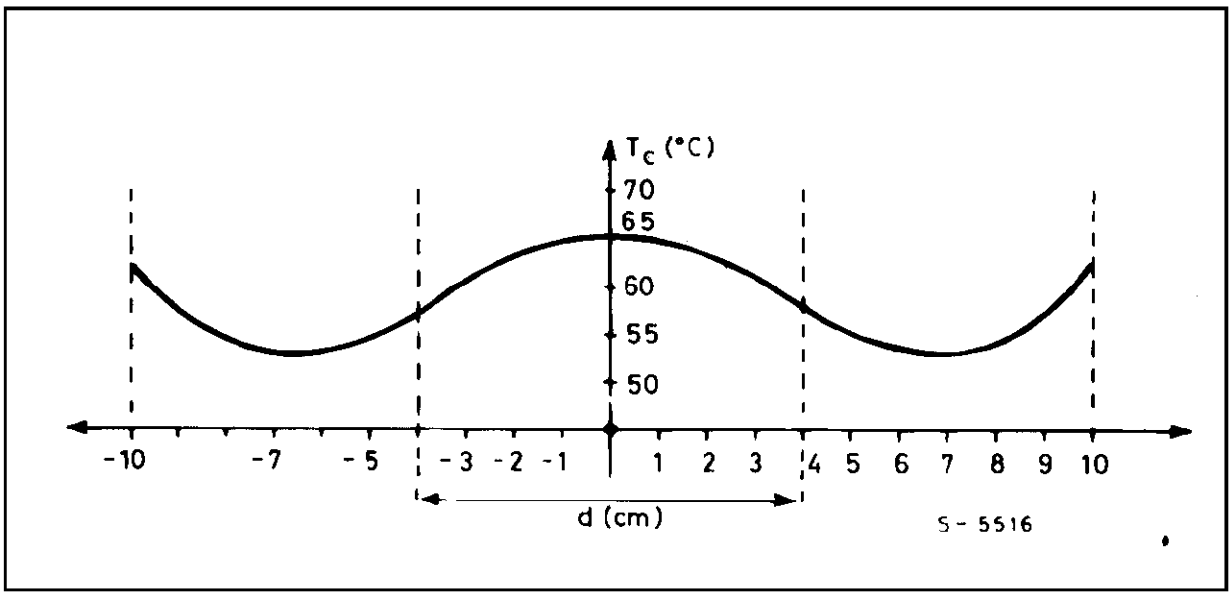
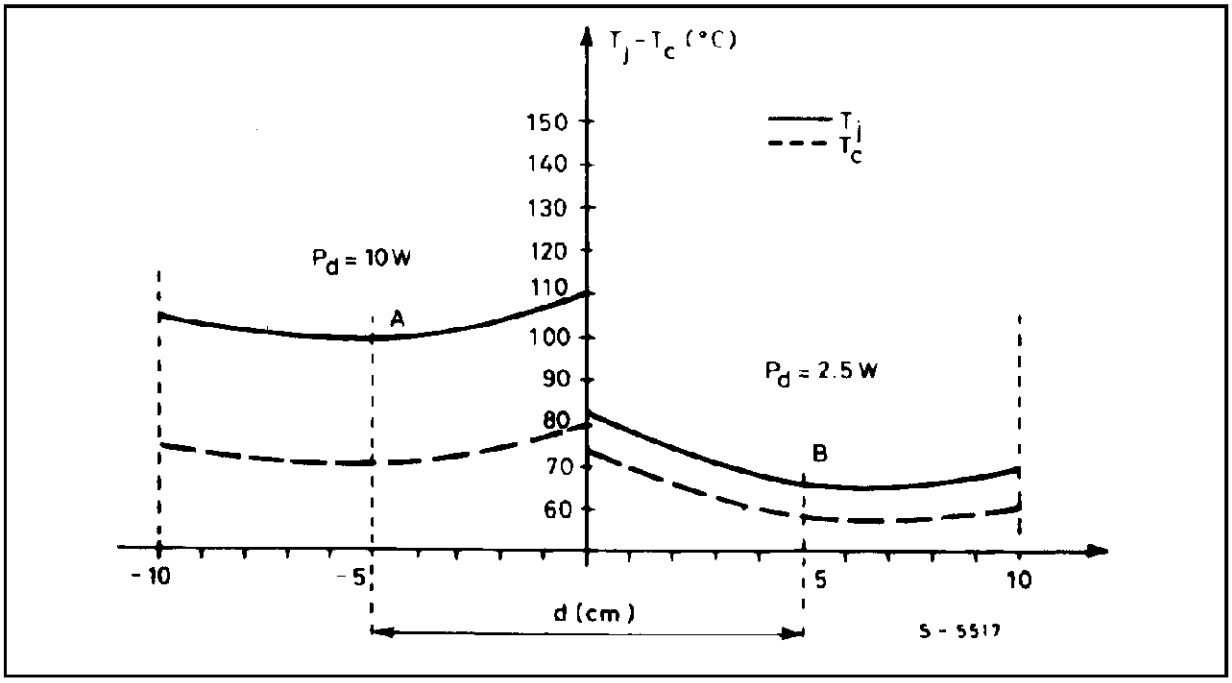


Figure 52.



APPENDIX A

CALCULATING SYSTEM STABILITY

This section is intended to help the designer in the calculation of the stability of the whole system.

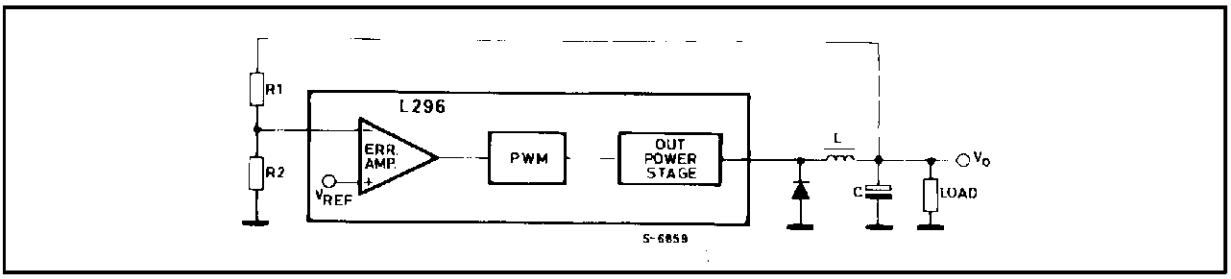
Figure A1 shows the entire control system of the switching regulator.

The problem which arises immediately is the transfer function of the PWM block and output stage, which is non-linear. If this function can be considered linear the analysis is greatly simplified.
Since the circuit operates at a constant frequency and the internal logic is fairly fast, the error introduced by assuming that this function linear is minimized. Factors which could contribute to the non-linearity are an excessive delay in the output power transistor, ringing and parasitic oscillations generated in the power stage and non-linearity introduced by magnetic part.

In the case of the L296, in which the power transistor is internal and driven by well-controlled and efficient logic, the contribution to non-linearity is further reduced.

For the assumption of linearity to be valid the cut-off frequency of the LC filter must be much lower than the switching frequency. In fact, switching operation introduces singularities (poles) at rougly half the switching frequency. Consequently, as long as the LC filter is still dominant, its cut-off frequency must be at least an order of magnitude lower than the switching frequency. This condition is not, however, diffucult to respect. The characteristics of LC filter affect the output voltage waveforms; is generally much less than an order of magnitude below the switching frequency.

Figure A1: The control Loop of the Switching Regulator.



GAIN OF THE PWM BLOCK AND OUTPUT STAGE

The equation which links V_o to V_i is:

$$V_o = V_i \frac{T_{ON}}{T}$$

A variation ΔT_{ON} in the conduction time of the switching transistor causes a corresponding variation in the output voltage, ΔVo, giving:

$$\frac{\Delta V_o}{\Delta T_{ON}} = \frac{V_i}{T}$$

Indicating with V_r the output voltage of the error amplifier, and with V_{ct} the amplitude of the ramp (the difference between the maximum and minimum values), T_{ON} is zero when V_r is at the minimum values), T_{ON} is zero when V_r is at the minimum value and equal to T when V_r is at a maximum. Consequently:

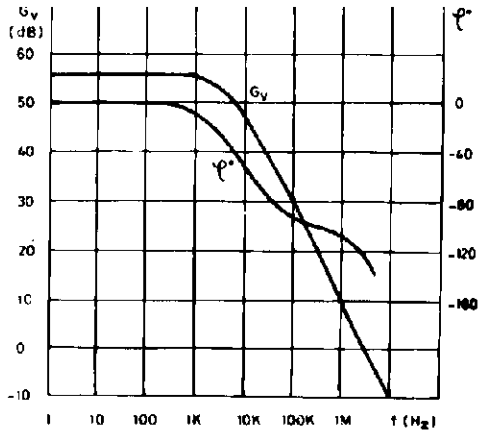
$$\frac{\Delta T_{ON}}{\Delta V_r} = \frac{T}{V_{ct}}$$

The gain is given by:

$$\frac{\Delta V_o}{\Delta V_r} = \frac{V_i}{V_{ct}}$$

Since V_{ct} is absolutely constant the gain of the PWM block is directly proportional to the supply voltage V_i.

Figure A2: Open Loop Frequency and Phase Response of Error Amplifier



The error amplifier is a transconductance amplifier (it trasforms a voltage variation at the input into a current variation at the output). It is used in open loop configuration inside the main control loop and its gain and frequency response are determined by a compensation network connected between its output and ground.

In the application a series RC network is recommended which gives high system gain at low frequency to ensure good precision and mains ripple rejection and a lower gain at high frequencies to ensure stability of the system. Figure A2 shows the gain and phase curves of the uncompensated error amplifier.

The amplifier has one pole at about 7kHz and a phase shift which reaches about –90° at frequencies around 1MHz.

The introduction of a series network Rc Cc between the output and ground modifies the circuit as shown in figure A3.

Figure A4 shows the gain and phase curves of the compensated error amplifier.

Figure A3: Compensation Network of the Error Amplifier

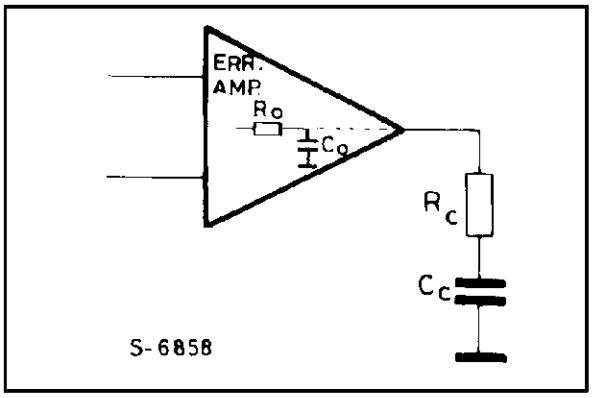
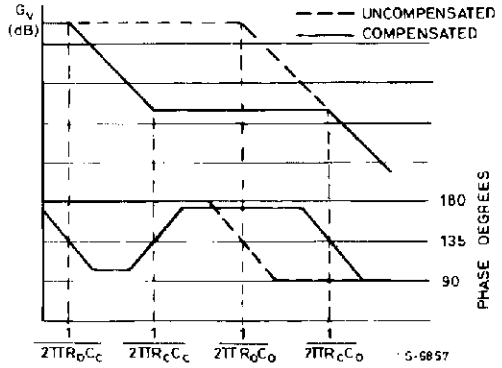


Figure A4: Bode Plot Showing Gain and Phase of Compensated Error Amplifier.



CALCULATING THE STABILITY

For the stability calculation refer to the block diagram shown in figure A5.

The transfer functions of the various blocks are rewritten as follows.

The simplified transfer function of the compensated error amplifier is:

$$G_{EA} = g_m Z_c = \frac{1 + s R_c C_c}{s C_c} \left(g_m = \frac{1}{2500} \right)$$

The DC gain must be considered equal to:

$A_o = g_m R_o$

PWM block and output stage:

$$G_{PWM} = \frac{V_i}{V_{ct}}$$

LC FILTER:

$$G_{LC} = \frac{1 + s C \cdot ESR}{s^2 LC + s C ESR + 1}$$

Where ESR is the equivalent series resistance of the output capacitor which introduces a zero at high frequencies, indispensable for system stability. Such a filter introduces two poles at the angular frequency.

$$\omega_o = \frac{1}{\sqrt{LC}}$$

Refer to the literature for a more detailed analysis.

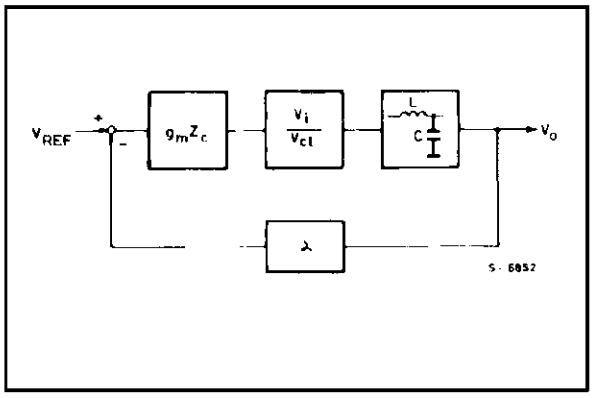
Feedback: consists of the block labelled α

$\alpha = 1$ when $V_o = V_{REF}$ (and therefore $V_o = 5.1V$)

and

$$\alpha = \frac{R2}{R1 + R2} \text{ when } V_o > V_{REF}$$

Figure A5: Block Diagram Used in Stability Calculation.



To analyse the stability we will use a Bode diagram. The values of L and C necessary to obtain the required regulator output performance, once the frequency is fixed, are calculated with the following formulae:

$$L = \frac{(V_i - V_o)\, V_o}{V_i\, f\, \Delta I_L}$$

$$C = \frac{(V_i - V_o)\, V_o}{8L\, f^2\, \Delta I_L}$$

Since this filter introduces two poles at the angular frequency

$$\omega_o = \frac{1}{\sqrt{LC}}$$

we place the zero of the R_c C_c network in the same place:

$$\omega_z = \frac{1}{R_c\, C_c}$$

Taking into account also the gain of the PWM block, the Bode plot of figure A6 is obtained.

The slope where the curve crosses the axis at 0dB is about 40dB/decade therefore the circuit is unstable.

Taking into account now the zero introduced by the equivalent series resistance (ESR) of the output capacitor, we have further condition for dimensioning the R_c C_c network. Knowing the ESR (which is supplied by the manufacturer for the quality components) we can determine the value of R_c so that the axis is crossed at 0dB with a single slope. The zero introduced by the ESR is at the angular frequency:

$$\omega_{zESR} = \frac{1}{ESR \cdot C}$$

The overall Bode diagram is therefore as shown in figure A7.

Figure A6: Bode Plot of System Taking Filter and Compensation Network into Account.

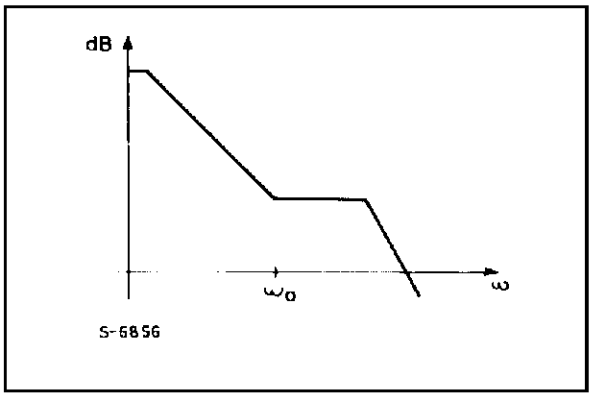
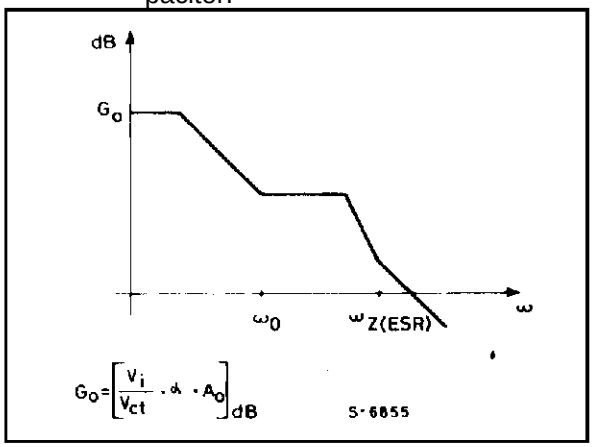


Figure A7: Bode Plot of Complete System Taking into Consideration the Equivalent Series Resistance of the Output Capacitor.



DC GAIN AND LINE REGULATION

Indicating the open-loop gain of the error amplifier with A_o, the overall open-loop gain of the system is:

$$A_t = A_o \frac{V_i}{V_{ct}} \cdot \frac{R2}{R1 + R2}$$

When $V_o = V_{REF}$, the gain becomes:

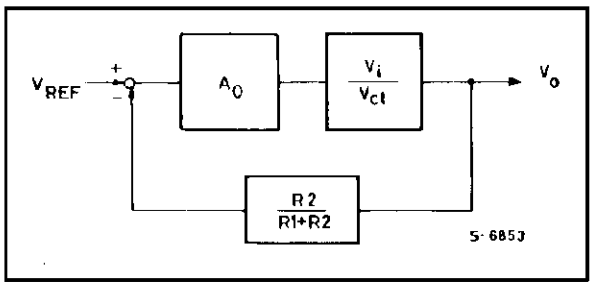
$$A_t = A_o \frac{V_i}{V_{ct}}$$

Considering the block diagram of figure A8 and calculating the output variation ΔV_o caused by a variation of V_i, from the literature we obtain:

$$\frac{\Delta V_o}{V_o} = \frac{\frac{\Delta V_i}{V_i}}{\frac{A_o\, V_i}{V_{ct}} \cdot \frac{R2}{R1 + R2}}$$

This espression is of general validity. In our case the percentage variation of the reference must be added by vector addition.

Figure A8: Block Diagram for Calculation of Line Regulation.



APPENDIX B

REDUCING INTERFERENCE

The main disadvantage of the switching technique is the generationof interferencewhich can reach levels which cause malfunctions and interfere with other equipment.

For each applicationit is thereforenecessary to study specific means to reduce this interference within the limits allowed by the appropriate standards.

Among the main sources of noise are the parasitic inductances and capacitances within the system which are charged and discharged fastly. Parasitic capacitances originate mainly between the device case and the heatsink, the windings of the inductor and the connectionwires. Parasitic inductances are generally found distributed along the strips of the printed circuit board.

Fast switching of the power transistors tends to cause ringing and oscillations as a result of the parasitic elements. The use of a diode with a fast reverse recovery time (trr) contributes to a reduction in the noise flowing by the current peak generated when the diode is reverse biased.

Radiated interference is usually reduced by enclosing the regulator in a metal box.

To reduce conducted electromagnetic interference (or radio frequency interferences - RFI) to the levels permitted a suitably dimensioned filter is added on the supply line. The best method, generally, to reduce conducted noise is to filter each output terminal of the regulator. The use of a fixed switching frequency allow the use of a filter with a relatively narrow bandwidth. For off-line switching eregulators this filter is usuallycostly and bulky. In contrast, if the device is supplied from a 50/60Hz transformer the RFI filter problem is gratly reduced.

Tests have been carried out the laboratories of Roederstein to determine the dimensions of a mains supply filter which satisfies the VDE 0871/6.78, class B standard. The measurements (see figs. B1 and B2) refer to the application with the L296 supplied with a filtered secondary voltage of about 30V, with V_o = 5.1V and I_o = 4A. The switching frequency is 100kHz.

Figure B1 shows the results obtainedby introducing on the transformer primary a 0.01µF/250V ~ class X capacitor (type ERO F1753-210-124). To reduce interference further below the limit set by the standards an additional inductive filter must be added on the primary of the transformer.

Figure B2 shows the curves obtained by introducing this inductive filter (type ERO F1753-210-124). Measurements have also been performed beyond 30MHz; the maximum value measured is still well below the limit curve.

Figure B1: EMI Measurements with a Capacitor Connected across the Primary Transformer with Screen Grounded (A)

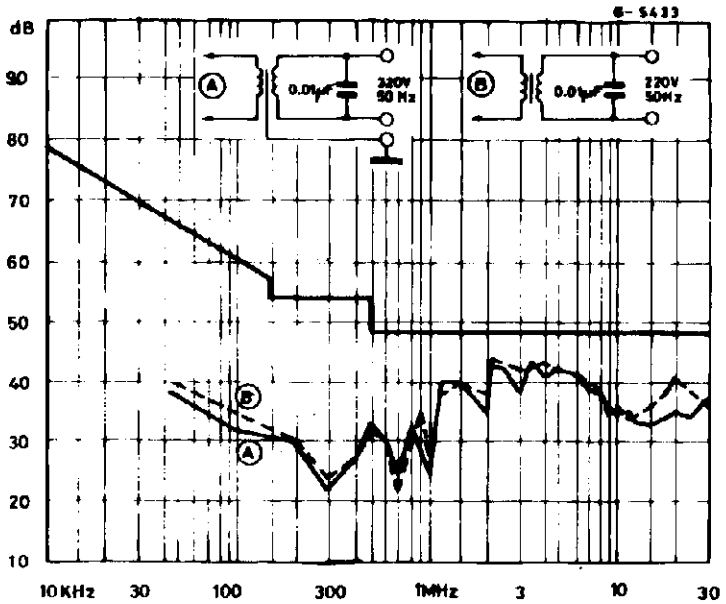


Figure B2: EMI results with the addition of an inductive filter on the mains input.