AN1261
APPLICATION NOTE

GETTING FAMILIAR WITH THE L6590 FAMILY HIGH-VOLTAGE FULLY INTEGRATED POWER SUPPLY

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In offline switchers in general and in low power ones in particular, the driving factors when making a design are reduction of cost, component count, size, weight as well as design to market.

The monolithic or "one-chip" solution, where PWM control and power switch are integrated on the same silicon and/or housed in the same package, looks very attractive especially in low power applications, where the typical approach, with separate PWM IC and power switch, features the higher cost-per-watt. A monolithic solution, which allows to build an SMPS with very few external parts, has in this case a dramatic impact. On the other hand, the flexibility of the "two-chip" approach does not provide significant advantages in such systems where no sophisticated functionality is normally required. Additionally, the monolithic approach improves system reliability and reduces design effort.

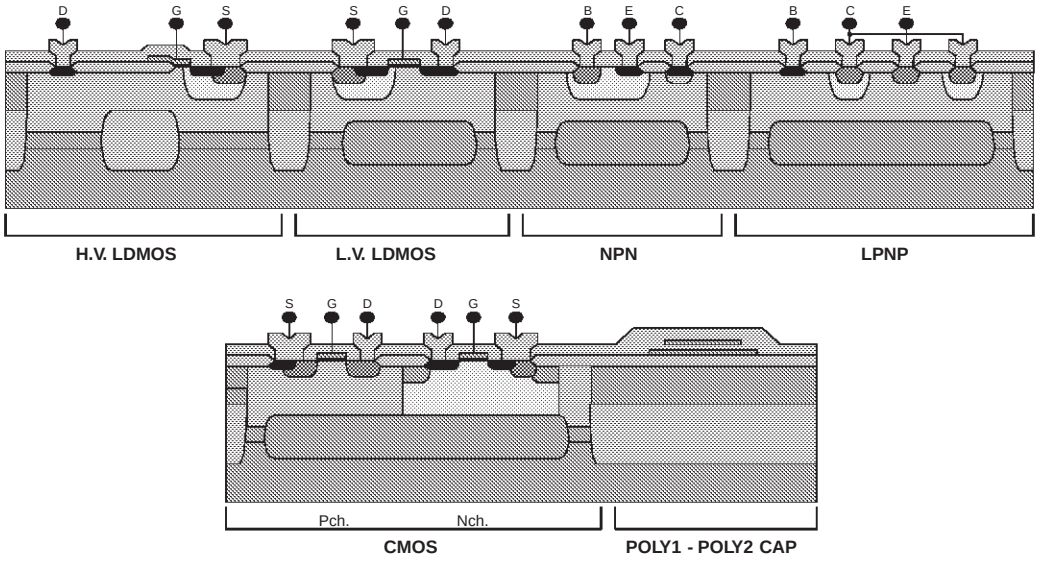
This application note describes in details the L6590 and the L6590A, a set of integrated monolithic switching regulators for offline converters. After a brief description of BCD OFFLINE, the technology used for these devices, their internal architecture and functionality will be described in details, then a number of application ideas and application examples will be provided.

BCD OFF-LINE TECHNOLOGY

The high level of integration of the L6590 family is made possible by the BCD OFF-LINE technology. Compared to other high voltage technologies, BCD allows more design flexibility due to the large variety of components available:

- high voltage N-channel LDMOS (700V)
- medium voltage bipolar transistor (20V, both NPN and PNP type)
- low and medium voltage CMOS devices (5 to 10V)
- zener voltage references
- resistors and capacitors.

Figure 1. BCD Off-line Cross Sections



In this way it is possible to realize compact and robust design solutions by integrating on the same silicon chip both high voltage power components and sophisticated control and protection functions .

Standard junction isolation is used, as shown in the cross section of the technology in Figure 1. The waste of silicon area due to lateral diffusion in thick epitaxial layers, normally required for high voltage capability, is eliminated with the so-called RESURF (Reduced Surface Field) approach. This technique allows the IC to withstand high voltages in very thin epitaxial layers (≤10 µm).

The RESURF approach implies lateral current flow in the high voltage DMOS, so this device has a lateral structure. As a result, the substrate of the IC is grounded and there is much less noise generation compared to a discrete FET.

GENERAL DEVICE DESCRIPTION

This family is a set of monolithic switching regulators able to operate with a very wide range of input voltage and primarily intended for Flyback, Boost or Forward topologies in offline applications. The power that the devices are able to handle is in excess of 10W in 110Vac or Wide Range Mains (WRM) applications and from 15 to 20W in 220Vac mains applications. In this power range flyback is the most common topology, so it will be considered as the reference topology in the following.

The family includes three members: the L6590 (housed in minidip), the L6590D (housed in SO16W) and the L6590A (housed in minidip).

Typically, the L6590 and the L6590D are suitable for low-power AC-DC adapters, auxiliary power supplies of CRT and LCD monitors and TV's. The L6590A may be used in these applications as well, however it is more specific for auxiliary power supplies of desktop PC's and servers. All of the devices can be used also to build both high-voltage and low-voltage DC-DC converters since they are able to operate with input voltages as low as 40V

Figure 2. L6590 Family Internal Block Diagram

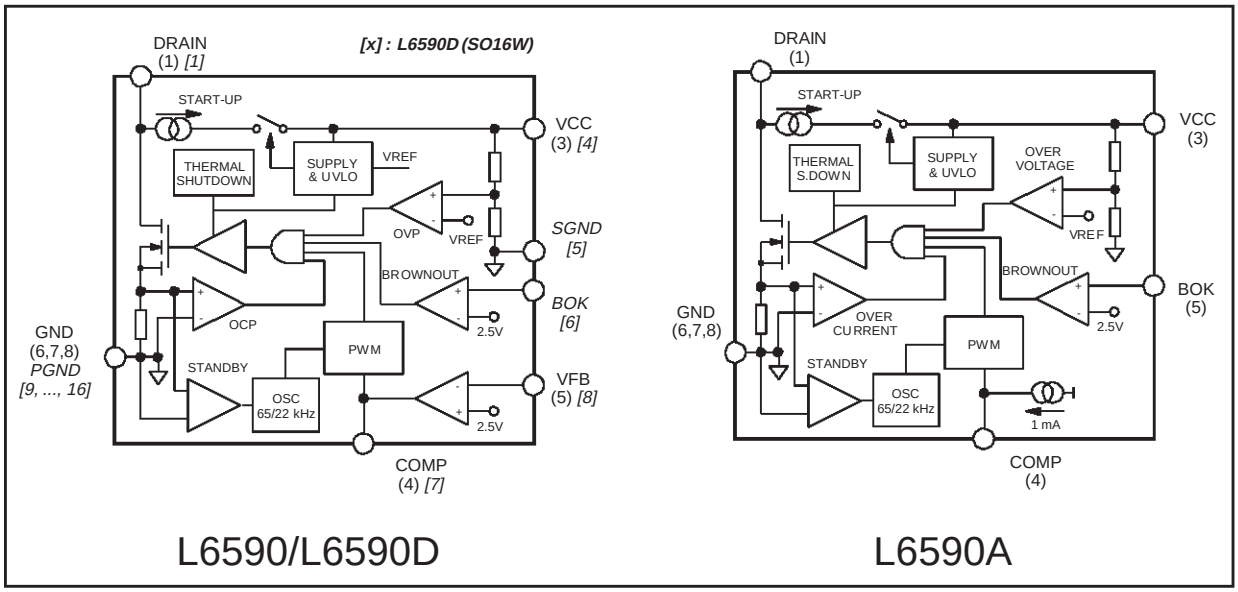


Figure 2 shows the internal block diagrams of the devices. The internal power switch is realised with a lateral high voltage power MOSFET with a typical $R_{DS(on)}$ of 13Ω and a $V_{(BR)DSS}$ of 700V. The fixed frequency (65 kHz) internal oscillator and the non-dissipative start-up allow to minimize the external components count.
The PWM control incorporates a voltage mode control scheme and converter's output voltage regulation can be achieved with both opto-isolated and primary sensing feedback. Internal protections like cycle-by-cycle current

limiting, output overvoltage protection, mains undervoltage (brownout) protection and thermal shutdown generate robust design solutions.
An outstanding feature of the converters based on the L6590 family is their very low consumption under no-load conditions. The low operating current and low parasitics of the devices, as well as their Standby function, which automatically reduces the oscillator frequency from 65kHz to 22kHz under light load conditions, allow to accomplish with regulations on standby consumption from the mains, such as Blue Angel or others.

Pin Connections and Description

The L6590 and L6590A are housed in minidip package for through-hole assembly, while the L6590D is housed in SO16W package for SMD assembly. Devices' pinout in both package versions is shown in figure 3. Table 1 summarises briefly pin functionality.

Figure 3. L6590 Family Pin Connections

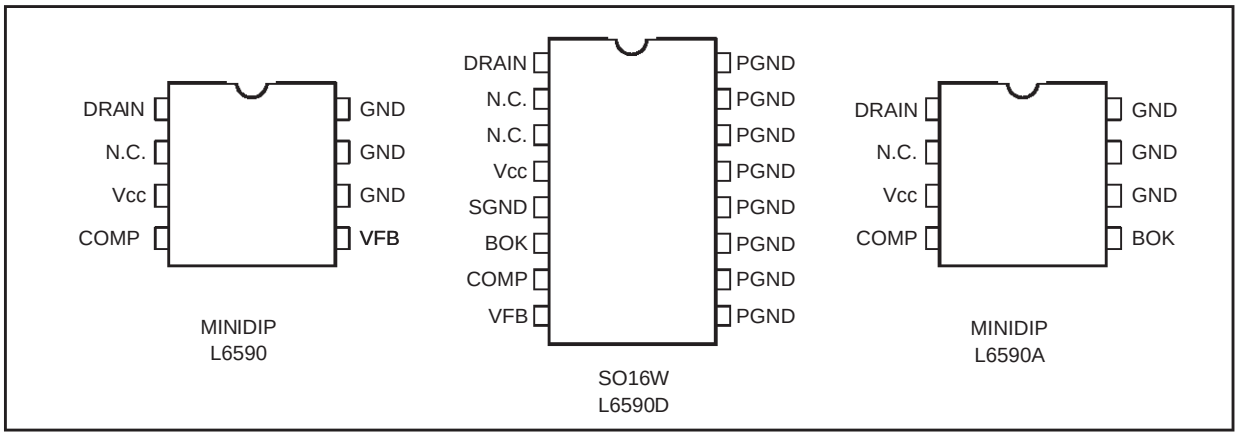


Table 1. L6590 Family Pin Connections

Pin #			Name	Description
L6590	L6590A	L6590D		
1		1	DRAIN	Drain connection of the internal power MOSFET. The internal high voltage start-up generator sinks current from this pin.
2		2, 3	N.C.	Not internally connected. Provision for clearance on the PCB.
3		4	V_{CC}	Supply pin of the IC. An electrolytic capacitor is connected between this pin and ground. The internal start-up generator charges the capacitor until the voltage reaches the start-up threshold. The PWM is stopped if the voltage at the pin exceeds a certain value.
4		4	COMP	Output of the Error Amplifier. Used for control loop compensation or to directly control PWM with an optocoupler.
5	-	8	VFB	Inverting input of the Error Amplifier. The non-inverting one is internally connected to a 2.5V± 2% reference. This pin can be grounded in some feedback schemes.
6 to 8		-	GND	Connection of both the source of the internal MOSFET and the return of the bias current of the IC. Pins connected to the metal frame to facilitate heat dissipation.
-	5	6	BOK	Brownout Protection. If the voltage applied to this pin is lower than 2.5V the PWM is disabled. This pin is typically used for sensing the input voltage of the converter through a resistor divider. If not used, the pin can be either left floating or connected to Vcc through a 15 kΩ resistor.
-	-	5	SGND	Current return for the bias current of the IC.
-	-	9 to 16	PGND	Connection of the source of the internal MOSFET. Pins connected to the metal frame to facilitate heat dissipation.

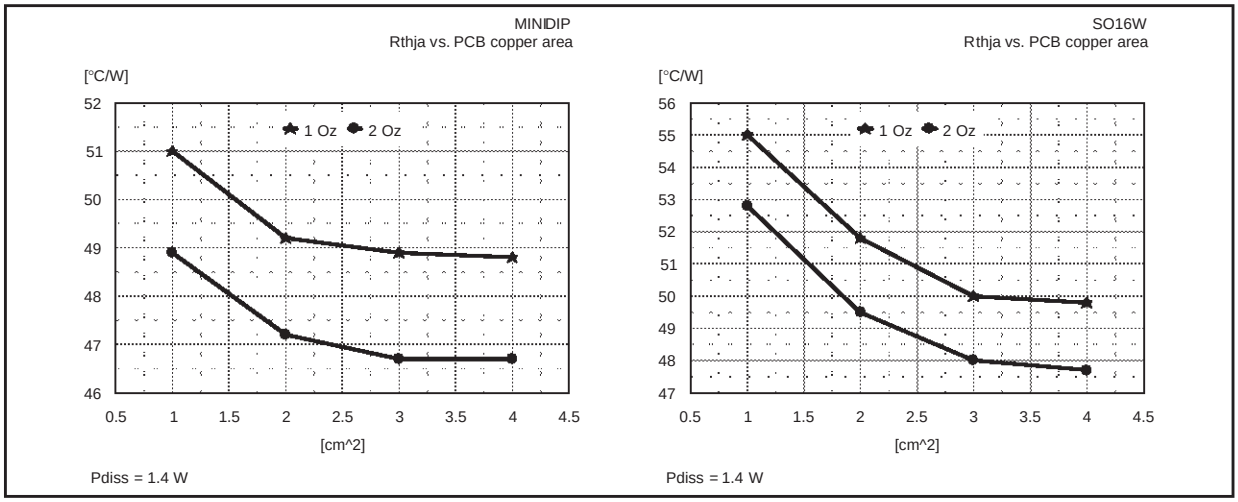
The L6590 is provided with an error amplifier for both primary and opto-isolated feedback; the L6590A, specific for PC auxiliary SMPS, has brownout protection on board in place of the error amplifier, thus it is eligible for opto-isolated feedback. Both the error amplifier and brownout protection are available in the SMD version L6590D.

Thermal properties

All of the ground pins (6, 7 and 8 in MINIDIP, 9 to16 in SO16W) are internally connected to the copper frame in order for heat to be easily removed from the silicon die. An heatsink can then be realized by simply making provision of some cm^2 of copper on the PCB.

Figure 4 shows the junction-to-ambient thermal resistance achievable with both packages as a function of the dissipating copper area on the PCB. The junction-to-pin thermal resistance is estimated about 15 °C/W in the MINIDIP package and about 20 °C/W in the SO16W.

Figure 4. L6590 Family Packages Junction-to-Ambient Thermal Resistance



DETAILED FUNCTIONS DESCRIPTION

In the following sections the various functional blocks shown in fig. 2 as well as the most important internal functions will be described in details.

Start-up circuit and Internal Supply

When power is first applied to the circuit the voltage on the bulk capacitor builds up and, as it reaches some ten volts, an internal high-voltage current generator is sufficiently biased to start operating. It draws about 4.5mA from the input bulk capacitor through the primary winding of the transformer and the drain pin. This current charges the capacitor connected between pin V_{CC} (3) and ground, making its voltage rise linearly.

As the Vcc voltage reaches the start-up threshold (14.5V typ.) the chip, after resetting all its internal logic, starts operating, the internal power MOSFET is enabled to switch and the internal high-voltage generator is disconnected. The IC is powered by the energy stored in the V_{CC} capacitor until the self-supply circuit (typically an auxiliary winding of the transformer) develops a voltage high enough to sustain the operation. This start-up sequence is summarised in figure 5.

Figure 5. Start-up sequence

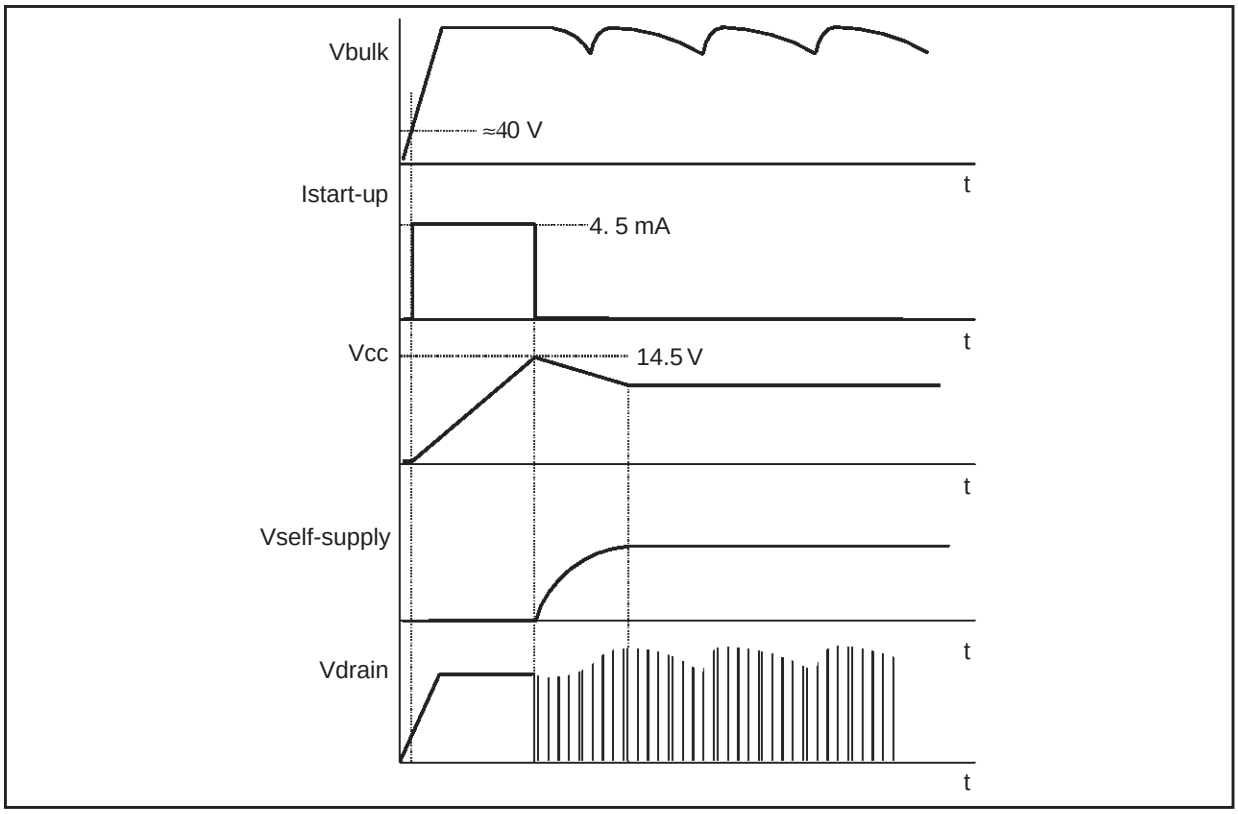


Figure 6 shows the internal schematic of the high-voltage start-up generator. It is made up of a high-voltage N-channel FET whose gate is biased by a 15MΩ resistor. If the V_{CC} voltage is below the start-up threshold, the $\overline{UVLO}$ signal is low and the high-voltage FET is biased above its threshold as the drain voltage is high enough. The drain current is controlled and held constant by the negative feedback loop including the 150Ω resistor and the BJT. As the V_{CC} voltage reaches the start-up threshold the $\overline{UVLO}$ signal goes high, the small FET is turned on and the high voltage FET is cut off. The two diodes prevent reverse flow current that would otherwise occur as the drain, during the ON-state of the power FET, has a voltage below V_{CC}. The residual consumption of this circuit is just the one on the 15MΩ resistor (≈10 mW at 400Vdc), typically 50-70 times lower, under the same conditions, compared to a standard start-up circuit made with an external dropping resistor.

As the IC is running, the supply voltage, typically generated by a self-supply winding, can range between the Overvoltage protection limit (OVP, see the relevant section) and the threshold of the Undervoltage Lockout (UVLO). Below this value the device is switched off and the internal start-up generator is activated. The two thresholds are in tracking.

The voltage on the V_{CC} pin is limited at safe values by a zener diode. Its breakdown voltage tracks the Overvoltage protection threshold.

The internal supply architecture is illustrated in figure 7. The V_{CC} voltage is monitored by the UVLO block which turns the device off if it falls below the UVLO threshold and is directly used to supply the driver of the power MOSFET. From the V_{CC} bus it is derived the bandgap reference, internally trimmed and temperature compensated, used to generate the 2.5V reference for the Error Amplifier (not in the L6590A). Also this reference voltage is monitored by the UVLO block and the device is stopped if the value is not within the spec. The 2.5V reference is also used for the linear regulator that provides the two 5V internal buses supplying the analog part and the digital part of the IC respectively. For increased noise immunity the two buses are separately buffered.

Figure 6. High-voltage Start-up generator

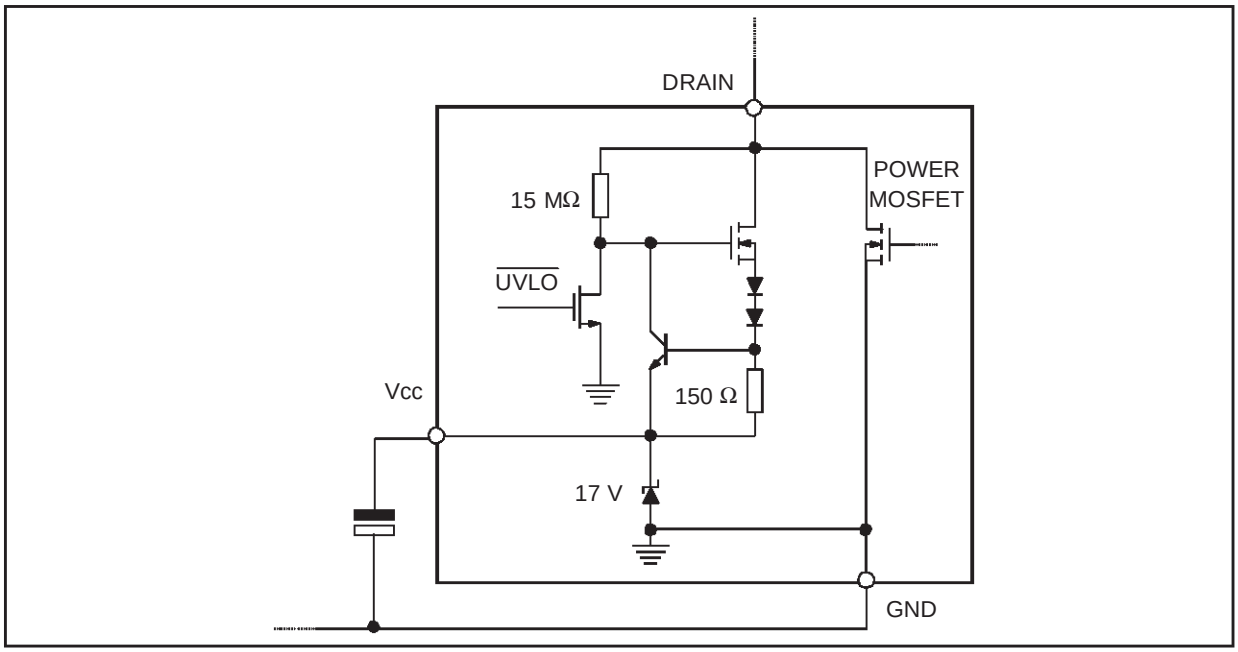
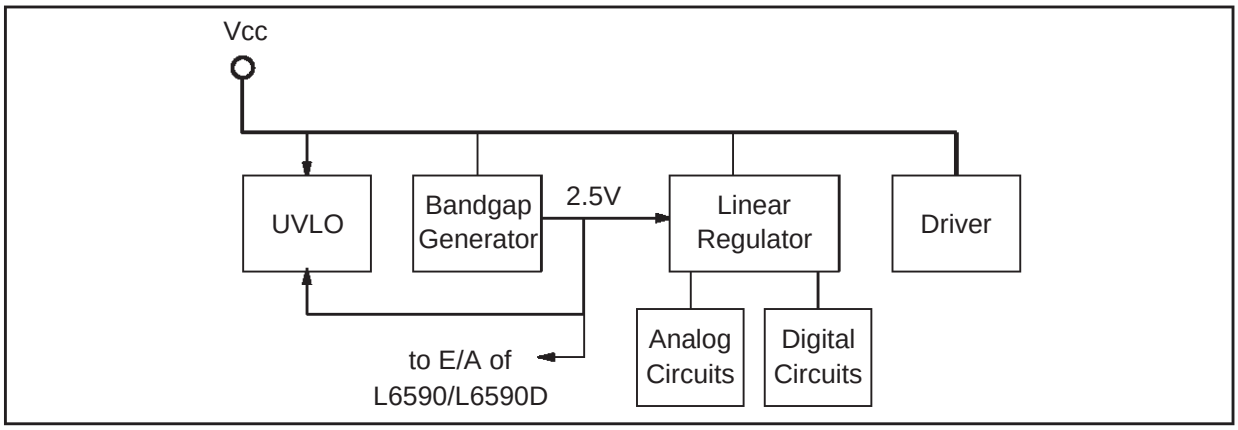


Figure 7. L6590 Internal Supply Architecture



Under UVLO conditions the consumption of the IC, mainly due to the UVLO block and the Bandgap generator, is below 1mA and this current is supplied by the internal start-up generator.

When the device is running the consumption is obviously higher. At V_{CC} = 10V the consumption, driver not included, is about 3.6mA (typ.). The consumption of the Driver depends on which frequency the oscillator is set at: it is typically 0.2mA at low frequency and 0.5mA at high frequency, for a total consumption of 4.1mA maximum, that is 41mW.

Power MOSFET and Gate Driver

The power switch is implemented with a lateral N-channel DMOS having a $V_{(BR)DSS}$ of 700V min. and a typical $R_{DS(on)}$ of 13Ω. It has a SenseFET structure to allow a virtually lossless current sensing (used only for protection).

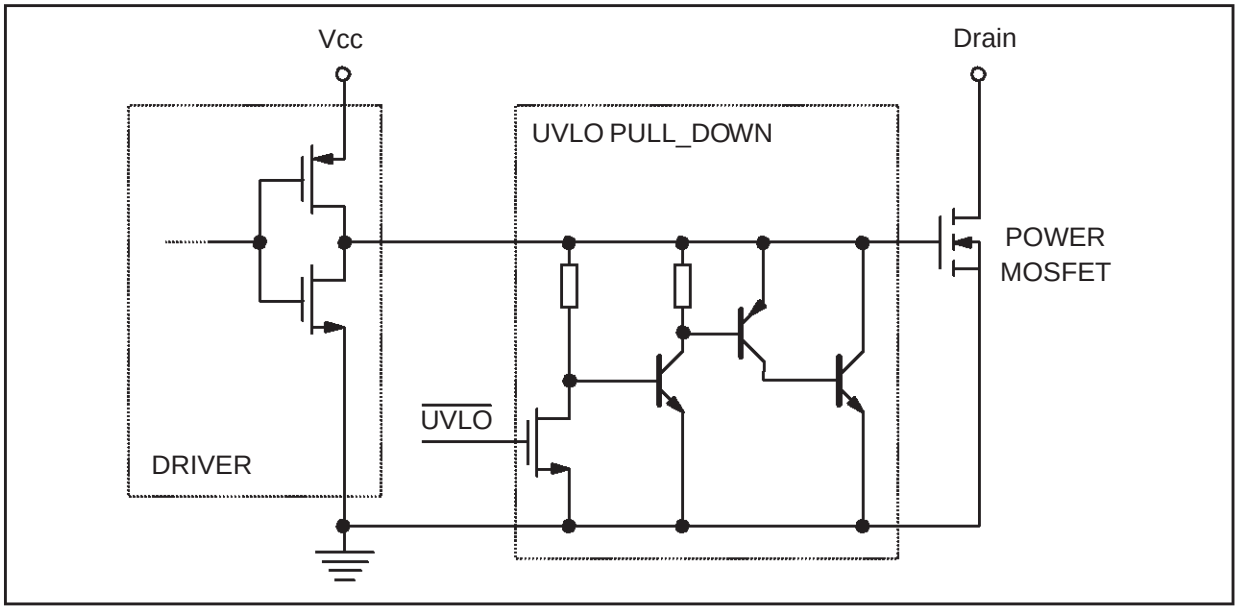
During operation in Discontinuous Conduction Mode at low mains the drain voltage is likely to go below ground.

Any risk of injecting the substrate of the IC on such occurrence is prevented by an internal structure surrounding the NDMOS.

The gate driver of the power MOSFET is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize common mode EMI.

Under UVLO conditions an internal pull-down circuit, shown in figure 8, holds the gate low in order to ensure that the power MOSFET cannot be turned on accidentally. When the device is turned on the $\overline{\text{UVLO}}$ signal is pulled high (refer to figure 8) and the circuit is disabled.

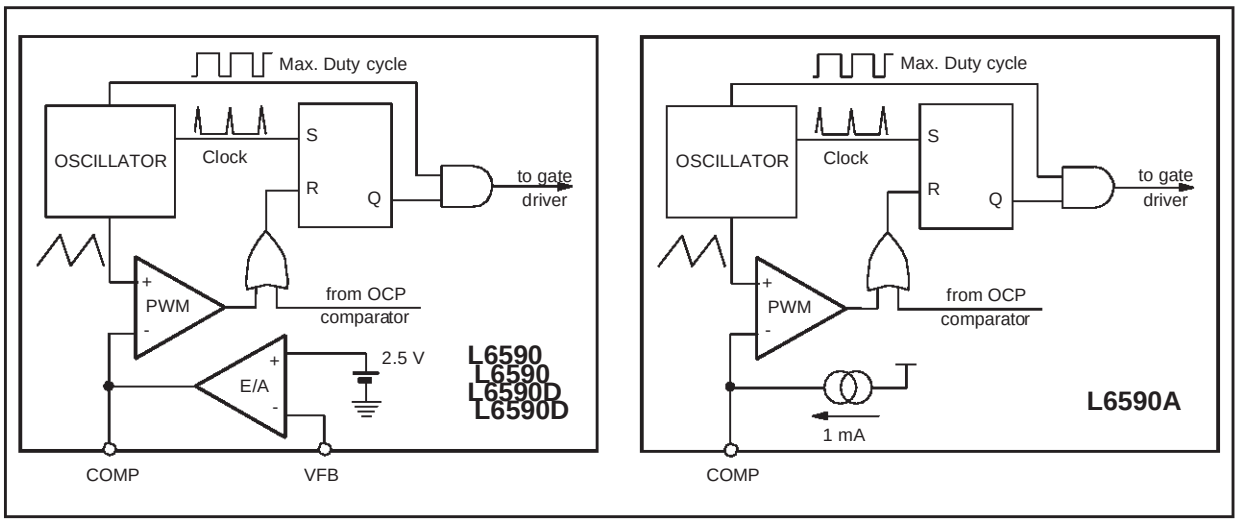
Figure 8. Gate pull-down during UVLO



Oscillator and PWM Control

PWM regulation is accomplished by implementing voltage mode control. As shown in fig. 9, this block includes an oscillator, a PWM comparator, a PWM latch and, in the L6590 and L6590D, an Error Amplifier as well.

Figure 9. PWM Control Block



The oscillator generates three signals: a clock pulse train to set the PWM latch, a triangular sawtooth applied to the (+) input of the PWM modulator and a square wave with 70% duty cycle used to gate the output of the PWM latch and set the maximum duty cycle of the power switch.

The oscillator operates at a frequency internally fixed at 65 kHz with a precision of ±10%. This value has been selected so that the second harmonic falls below 150kHz, beyond which some international EMC standards envisage more severe limits.

The oscillator is implemented by means of two current generators trimmed and temperature compensated (see fig. 10).

Figure 10. Oscillator internal schematic

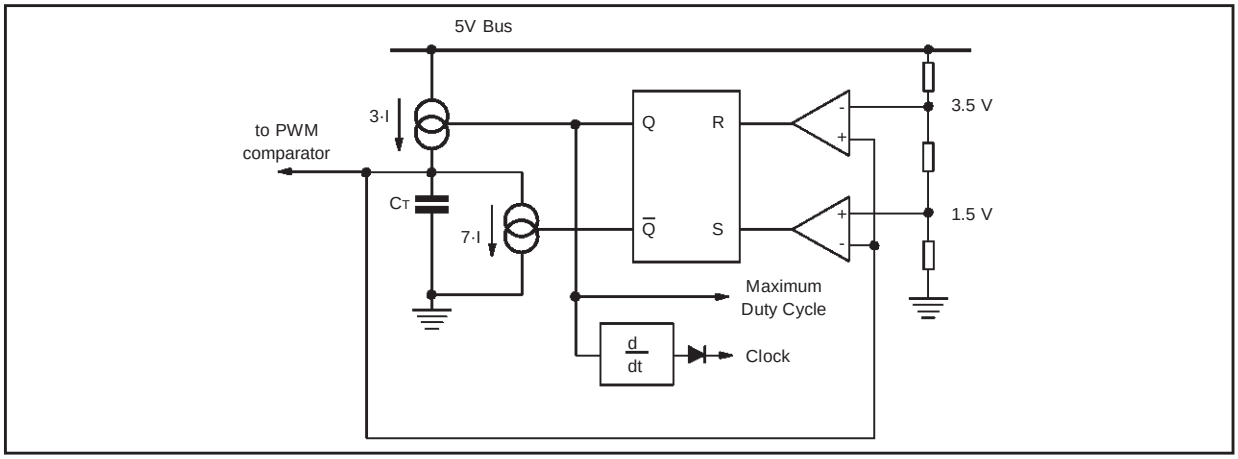
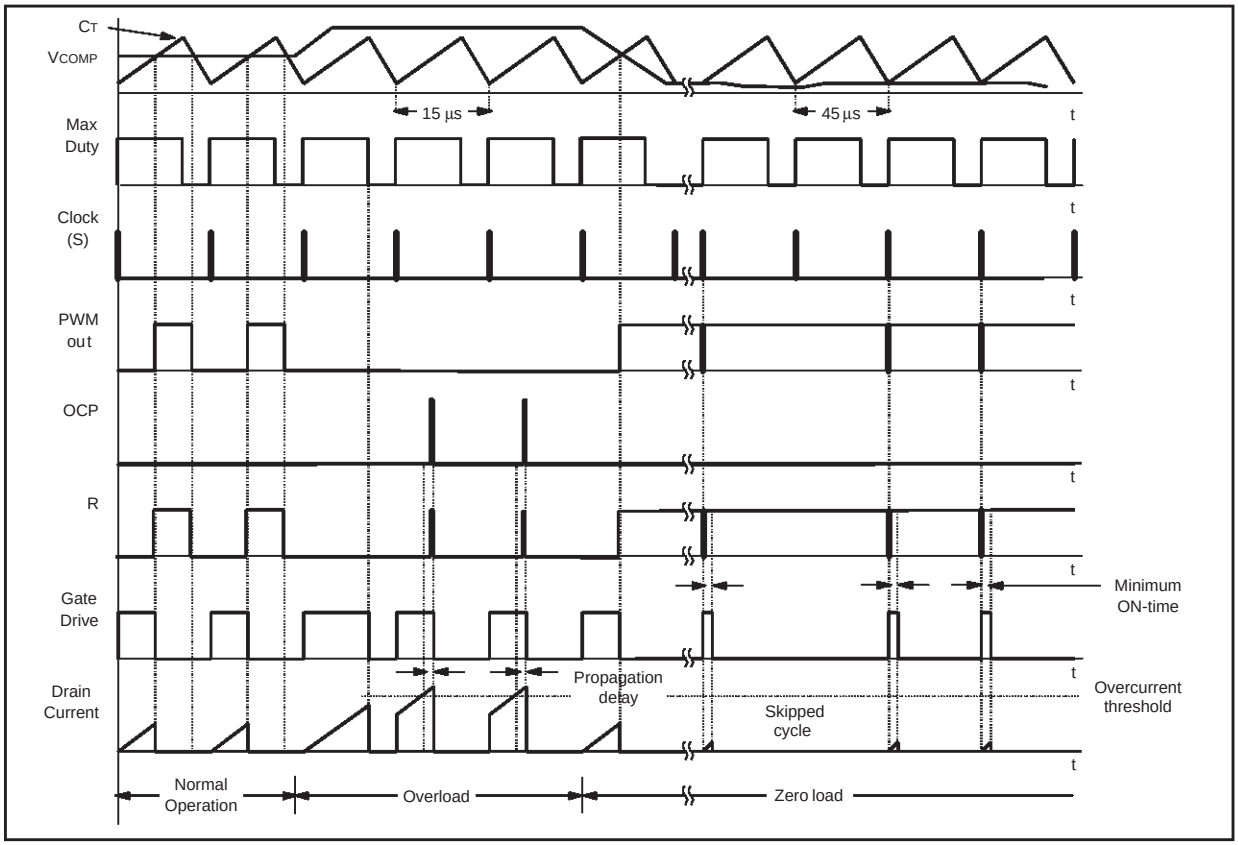


Figure 11. Voltage Mode Control PWM Timing Diagram



They alternately charge and discharge an internal capacitor C_T between two voltage levels (1.5V and 3.5V) thus generating a triangular waveform. To achieve 70% duty cycle the charge and discharge currents are in a 3:7 ratio. The gating signal to set the maximum duty cycle is taken from the Q output of the RS latch, while the clock pulse is generated during the low-high transition of the output Q.

The PWM latch (reset dominant) is set by the clock pulses of the oscillator and is reset by either the PWM comparator or the Overcurrent comparator (OCP, see "Protections" section).

The Error Amplifier (E/A) of the L6590 and L6590D is an op-amp with a MOS input stage and a class AB output stage. The amplifier is compensated for closed loop stability at unity gain, has a small-signal DC gain of 70dB (typ.) and a gain-bandwidth product over 1 MHz. The output of the E/A is fed to the inverting input of the PWM comparator and is externally available at pin 4 (COMP) for frequency compensation. Since this voltage controls the duty cycle, it will be referred to as the "control voltage".

In the L6590A the inverting input of the PWM comparator, that is the control voltage, is externally available at pin 4 (COMP) in order for an optocoupler-based circuit to modulate its voltage, so as to close the control loop that regulates the converter's output voltage.

The operation of this voltage mode control loop is illustrated in fig. 11. A clock pulse from the oscillator sets the PWM latch, which drives high the gate driver, and the power MOSFET is switched on.

The voltage on C_T ramps up and, as it hits the level at the inverting input, the PWM comparator reverses and resets the PWM latch terminating the conduction of the power MOSFET. The voltage on C_T completes its ramp-up, after that it starts ramping down until the valley is reached. Then another clock pulse is released and another cycle begins.

In case of overcurrent the control voltage saturates high and the conduction of the power MOSFET is stopped by the OCP comparator instead of the PWM comparator. At very light load the control voltage is close to its low saturation and the gate drive delivers as short pulses as it can, bottom limited by internal delays. They are however too long to maintain the long-term energy balance, thus from time to time some cycles need to be skipped and the operation becomes asynchronous. This is automatically done by the control loop: if there is a short-term excess of energy the control voltage saturates low completely and the reset signal is still high while the set clock pulse is released by the oscillator. Being the PWM latch reset dominant, the power MOSFET will not be turned on in that cycle.

Standby Function

The standby function, optimized for flyback topology, automatically detects a light load condition for the converter and decreases the oscillator frequency on that occurrence. The normal oscillation frequency is automatically resumed when the output load builds up and exceeds a defined threshold.

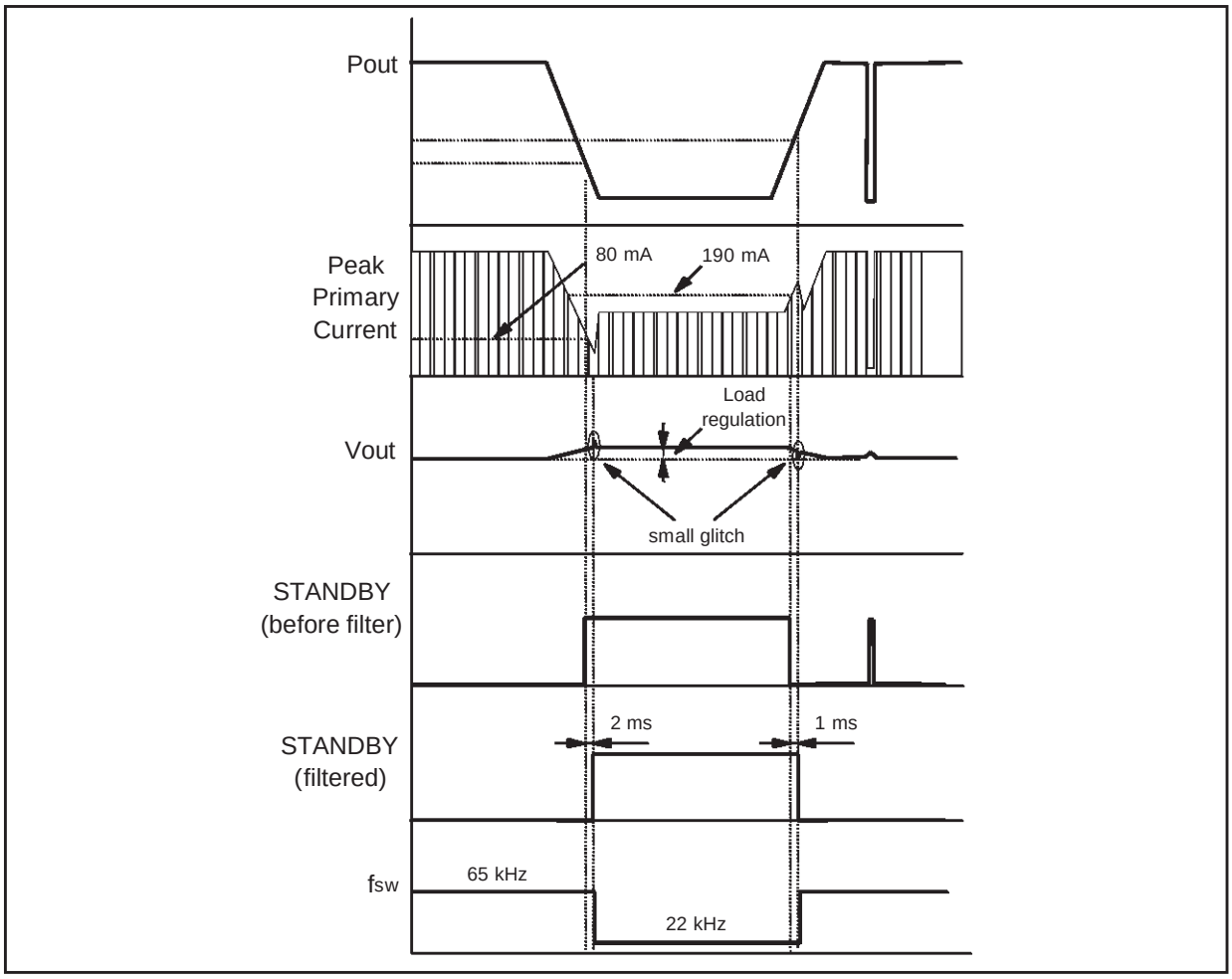
This function allows to minimize power losses related to switching frequency, which represent the majority of losses in a lightly loaded flyback, without giving up the advantages of a higher switching frequency at heavy load.

A positive side effect is a smooth transition from fixed frequency to asynchronous operation, as described in the previous section, when the load decays to very low values and approaches zero.

The Standby function is realized by monitoring the peak current in the power switch, being this related to the input power (see Ref. [1] for details). If the peak primary current decreases below a fixed threshold (80 mA) as a result of a reduced power demanded by the load, the oscillator frequency will be set at a lower value (22 kHz). This is done by dividing by three the capability of the current generators shown in fig. 10.

When the load demands more power, the peak primary current increases and exceeds a second threshold (190mA): then the oscillator frequency is reset at the normal value (65kHz). This 110mA hysteresis prevents undesired frequency change when power is such that the peak current is close to the threshold.

Figure 12. Standby Function Timing Diagram

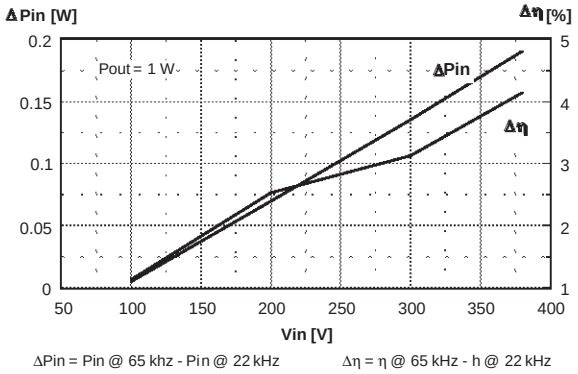


The signal coming from the sense circuit is digitally filtered to avoid false triggering of this function as a result of large load changes or noise. The filtering time is about 2 ms during the transition high-low and about 1 ms during the transition low-high. Figure 12 illustrates the operation of the function.

The effect of the frequency change to the converter's output voltage is a few mV glitch, much smaller than the overshoots and the undershoots resulting from a step load change.

The effect of the frequency reduction in terms of input power saving and efficiency increase (for a given load) is shown in fig. 13, with reference to the 10W test-board (2) shown in the datasheet of the L6590. The effect would be much more pronounced if RC snubbers were to be used on the secondary rectifier(s) or on the primary side to comply with EMI requirements.

Figure 13. Power saving and efficiency rise due to the standby function



Brownout Protection (L6590A and L6590D only)

Brownout Protection is basically a not-latched device shutdown functionality whose typical use is to sense a mains undervoltage. Nevertheless, this function

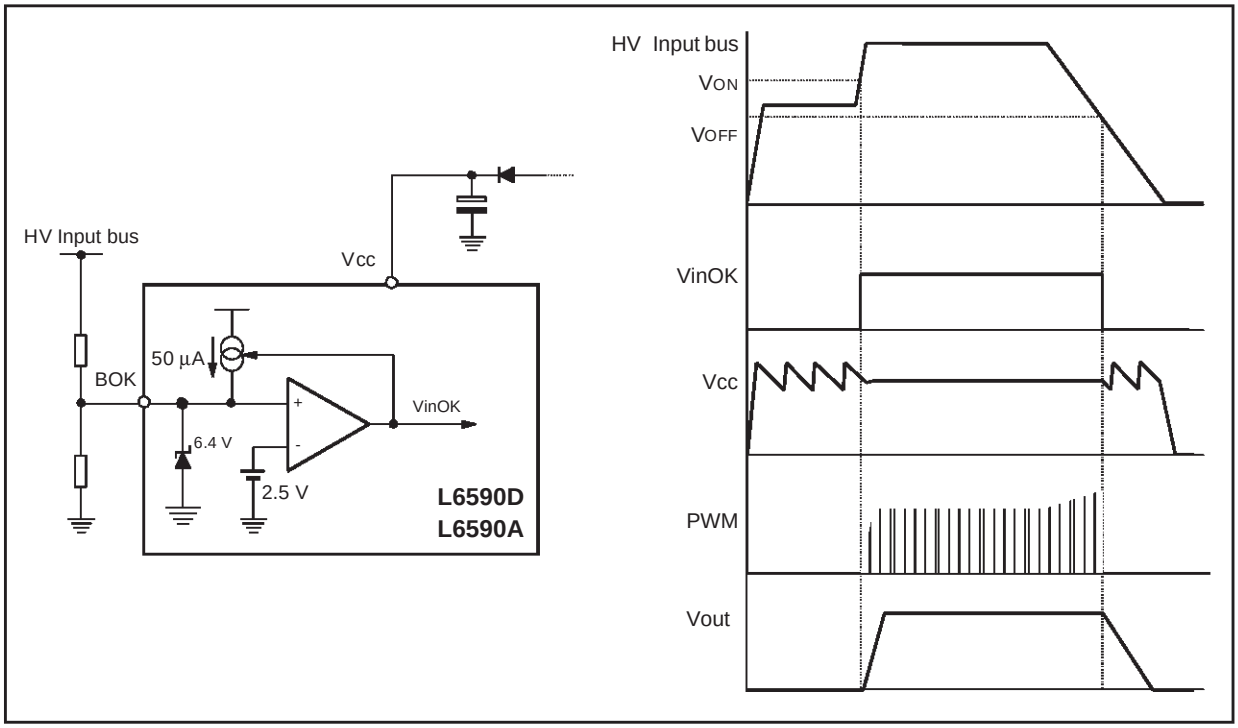
can serve other purposes as well, as shown in the section ”Application Ideas”, figure 20.

There are several reasons why it may be desirable to shut down a converter during brownout conditions, that is when the mains voltage falls below the minimum specification of normal operation.

One of these is that a brownout condition may cause overheating of the primary power section due to an excess of RMS current. Although this does not concern the IC directly since it is thermally protected (see the section ”Thermal Shutdown”), however this might be a problem in an SMPS including two converters (a high-power main converter and a low-power one for housekeeping and/or standby operation), such as in PC’s Silver Boxes. If either the L6590A or L6590D is used for the auxiliary converter and powers the controller of the main converter as well, the latter could benefit from shutdown in case of brownout.

Brownout can also cause a converter to work open-loop and this could be dangerous to the converter itself and the load, should the input voltage return abruptly to its rated value. Another problem is the spurious restarts that are likely to occur during converter power down if the input voltage decays slowly (e.g. with a large input bulk capacitor) and that cause the output voltage not to decay to zero monotonically.

Figure 14. Brownout Protection Internal Circuit and Timing Diagram



Converter shutdown can be accomplished with the L6590A or the L6590D by means of an internal comparator that can be used to sense the input voltage downstream the bridge rectifier, across the input bulk capacitor. This comparator is internally referenced to 2.5V and disables the PWM if the voltage applied at its externally available (non-inverting) input is below the internal reference, as shown in fig. 14. PWM operation is re-enabled as the voltage at the non-inverting input is more than 2.5V.

The brownout comparator is provided with current hysteresis instead of a more usual voltage hysteresis: an internal 50µA current generator is ON as long as the voltage applied at the non-inverting input exceeds 2.5V and is OFF if the voltage is below 2.5V.

This approach provides an additional degree of freedom: it is possible to set the ON threshold and the OFF threshold separately by properly choosing the resistors of the external divider (see below). With voltage hyster-

esis, instead, fixing one threshold automatically fixes the other one depending on the built-in hysteresis of the comparator.

The following relationships can be established for the ON (V_{inON}) and OFF (V_{inOFF}) thresholds of the input voltage:

$$V_{inON} \cdot \frac{R2}{R1+R2} = 2.5; \quad \frac{V_{inOFF}-2.5}{R1} + 50 \cdot 10^{-6} = \frac{2.5}{R2},$$

which, solved for R1 and R2, yield:

$$R1 = \frac{V_{inON}-V_{inOFF}}{50 \cdot 10^{-6}}; \quad R2 = R1 \cdot \frac{2.5}{V_{inON}-2.5}.$$

For a proper operation of this function, V_{inON} must be less than the peak voltage at minimum mains and V_{inOFF} less than the valley voltage on the input bulk capacitor at minimum mains and maximum load.

While the brownout protection is active the start-up generator keeps on working but there is no PWM activity, thus the V_{CC} voltage continuously oscillates between the start-up and the UVLO thresholds, as shown in the timing diagram of fig. 14.

The BOK pin is a high impedance point connected to high value resistors, thus it is prone to pick up noise. This might alter the OFF threshold when the converter is running or give origin to undesired switch-off of the IC during ESD tests. A film capacitor (e.g. 1-100 nF) can be connected in parallel to R2 to prevent any malfunctioning of this kind. If the function is not used the pin can be left floating: a small internal pull-up generator (≈ 5µA, not shown in fig. 14 for simplicity) maintains the voltage high and lets the device run normally. For more noise immunity the pin can be connected to V_{CC} through a 15 kΩ resistor.

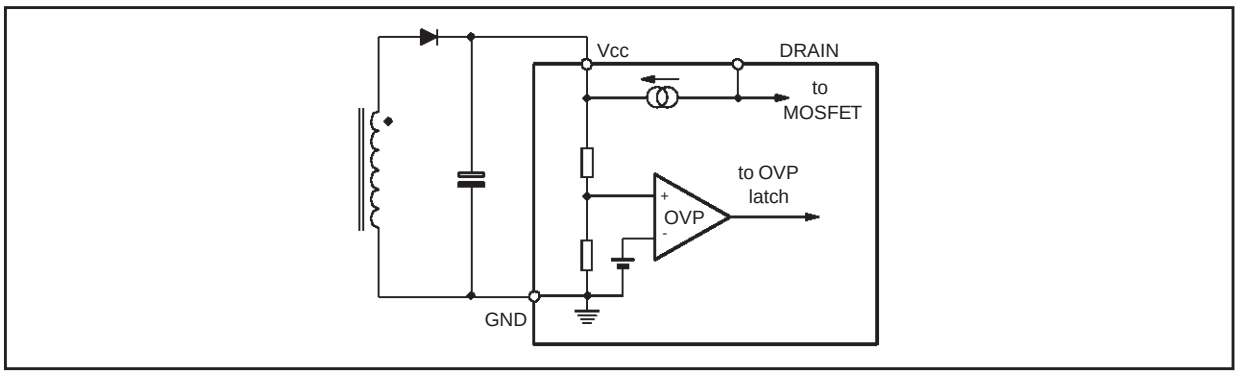
Overvoltage Protection

The devices of the L6590 family incorporate an Overvoltage Protection (OVP) that can be particularly useful to protect the converter and the load against voltage feedback loop failures. This kind of failure causes the output voltage to rise with no control and easily leads to the destruction or damage of the load and of the converter itself if not properly handled.

If such an event occurs, the voltage generated by the auxiliary winding that supplies the IC will fly up tracking the output voltage.

An internal comparator (see figure 15) continuously monitors the V_{CC} voltage and stops the operation of the IC if the voltage exceeds a threshold. This condition is latched and maintained until the V_{CC} voltage falls below the UVLO threshold. The converter will then operate intermittently.

Figure 15. OVP Circuit



Such kind of operation may also occur when the converter is overloaded because of the large spikes on the positive-going edges of the voltage delivered by the self-supply winding. These spikes may charge the V_{CC} capacitor to an abnormal value and trigger the OVP comparator. This will help reduce the power throughput and the stress on the secondary rectifier(s).

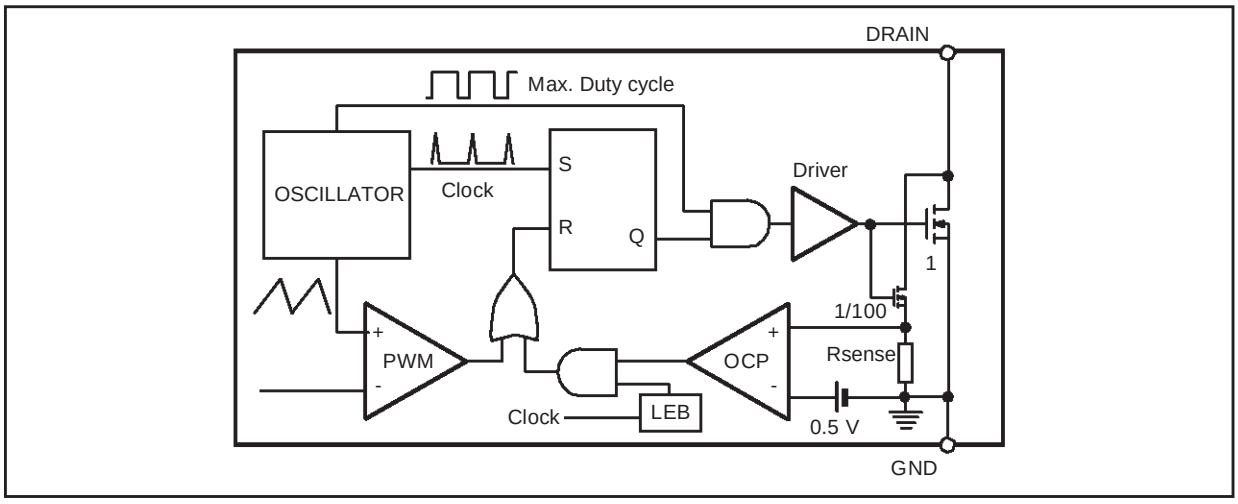
Overcurrent Protection

The devices use pulse-by-pulse current limiting for Overcurrent Protection (OCP), not to overstress of the internal MOSFET: its current during the ON-time is monitored and, if exceeding a determined value, the conduction is terminated immediately. The MOSFET will be turned on again in the subsequent switching cycle.

As previously mentioned, the MOSFET has a SenseFET structure: the source of a few cells are connected together and kept separate from the other source connections, to realize a 1:100 current divider. The "sense" portion is connected to a 75Ω ground referenced sense resistor R_{sense} having a low thermal coefficient (the resistance drift is less than 3% over the operating temperature range). As shown in fig. 16, the OCP comparator senses the voltage drop across Rsense and resets the PWM latch (thus turning off the MOSFET) if the drop exceeds a threshold set at 0.5V (this value is trimmed to get an overall precision of ±10%). In this way the overcurrent limit will be set at Ilim = (0.5V/75Ω)*100 ≈ 0.65A (typical value).

To increase noise immunity, the output of the OCP comparator is blanked for a short time (about 120 ns) just after the MOSFET is turned on, so that any disturbance within the blanking time is rejected. This is what is commonly known as LEB (Leading Edge Blanking). This blanking time adds up to other internal delays in the control loop path giving origin to the total propagation delay shown in fig. 11, which has an impact on the OCP characteristics as a function of the current slope.

Figure 16. OCP Circuit internal Schematic



Thermal Shutdown

Overheating of the device due to an excessive power throughput or insufficient heatsinking is avoided by the Thermal Shutdown function. A thermal sensor monitors the junction temperature close to the power MOSFET and, when the temperature exceeds 150 °C (min.), sets an alarm signal that stops the operation of the device. There is no more PWM activity but the start-up generator keeps on working, thus the V_{CC} voltage continuously oscillates between the start-up and the UVLO thresholds. This behaviour is identical to the one shown in fig. 14, resulting from the brownout protection. In these conditions, the device's quiescent current is reduced at less than 1mA.

This is a not-latched function and the power MOSFET is re-enabled as the chip temperature falls about 40 °C.

APPLICATION INFORMATION

Application Ideas

The following schematics show a few simple circuits able to solve some common application issues that can be encountered during the implementation of converters based on the L6590 family devices.

Figure 17. Protection against overload, short circuit or open feedback: a) HICCUP MODE; b) LATCH MODE

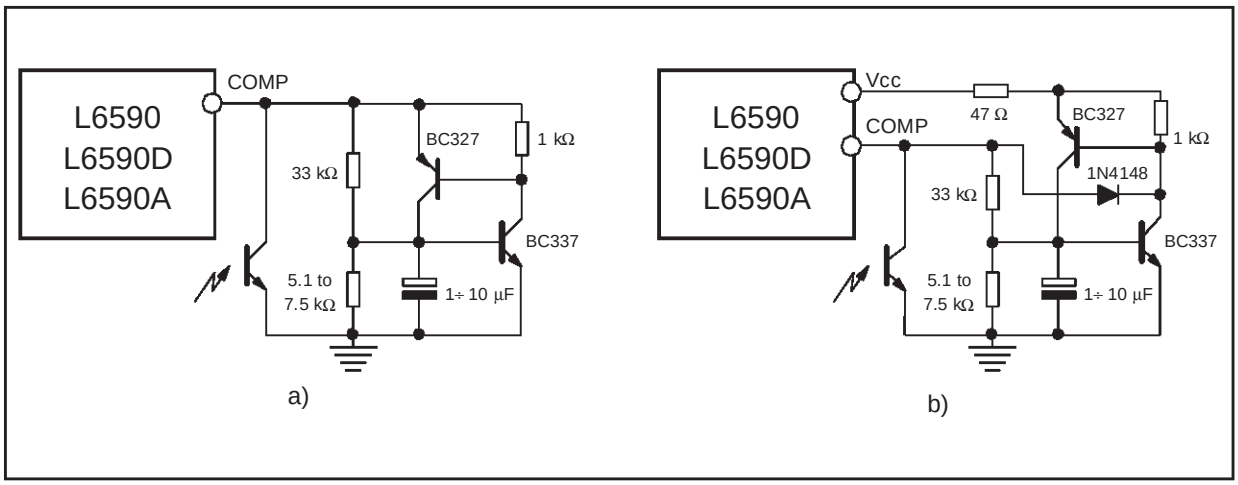


Figure 18. Mains OVP (the values shown set the threshold at 412V)

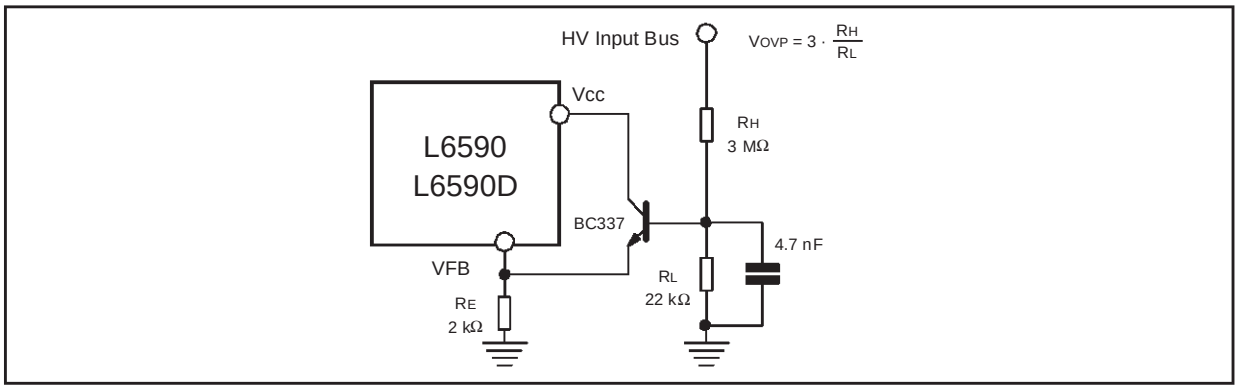


Figure 19. LEB circuit for leakage inductance spikes filtering, to improve primary regulation.

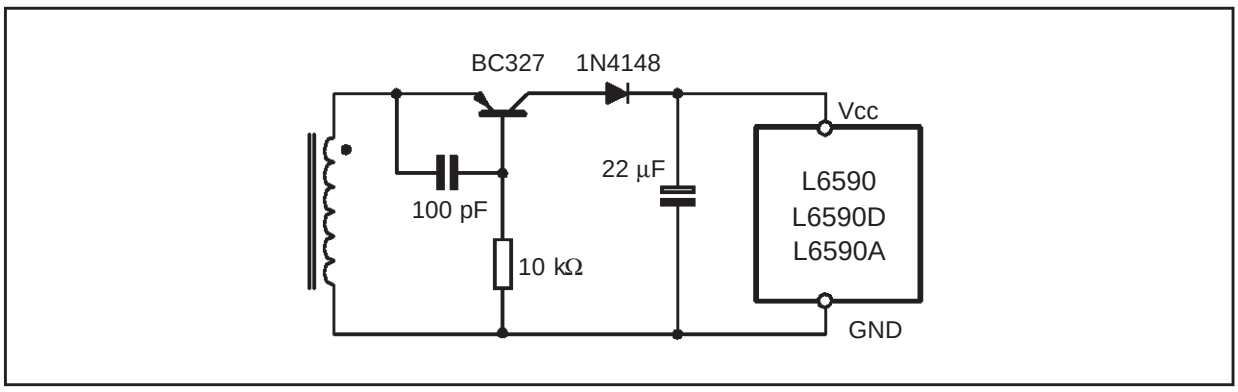


Figure 20. Simple secondary feedback

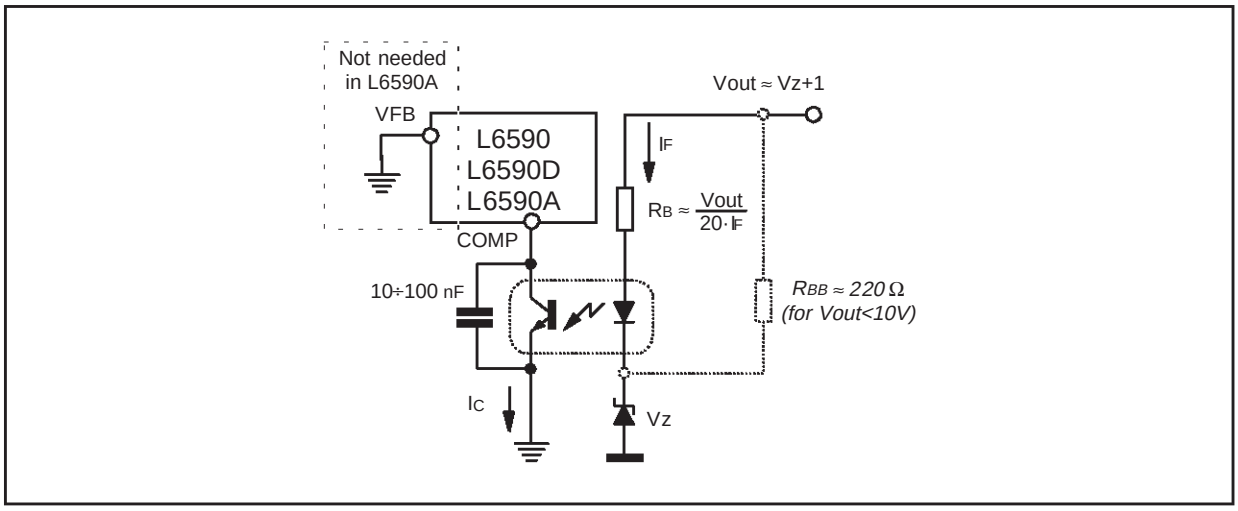


Figure 21. Secondary feedback with floating optocoupler (L6590, L6590D)

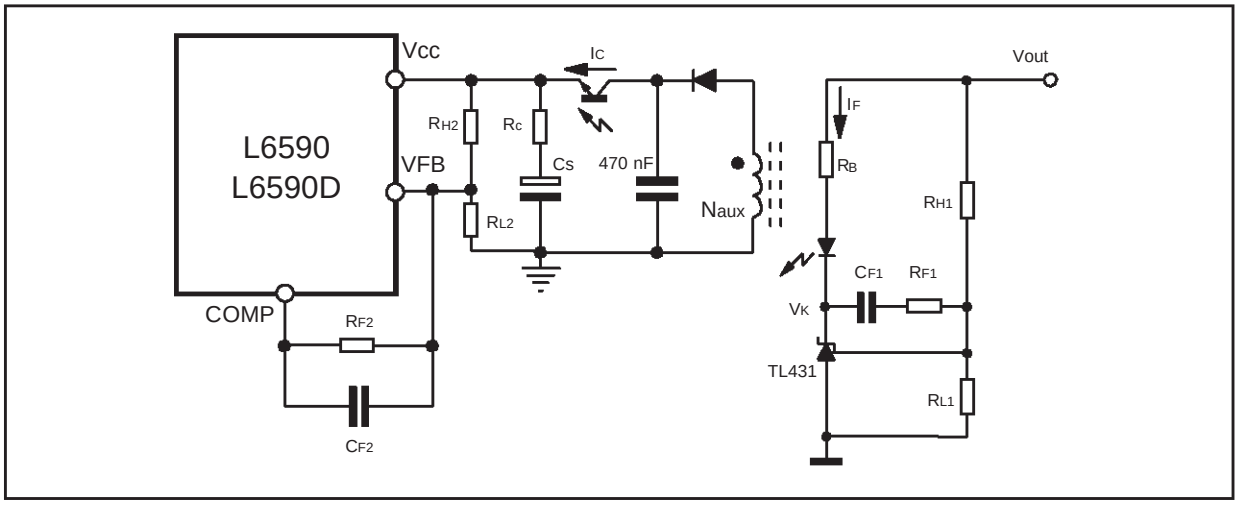


Figure 22. Secondary feedback with floating optocouler (L6590A)

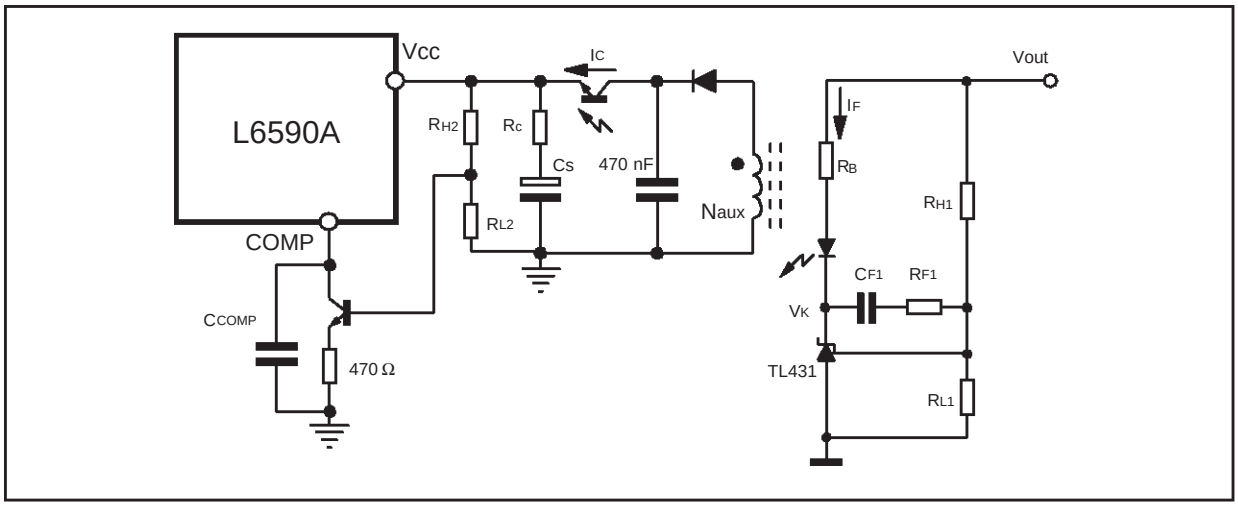


Figure 23. Primary feedback with the L6590A

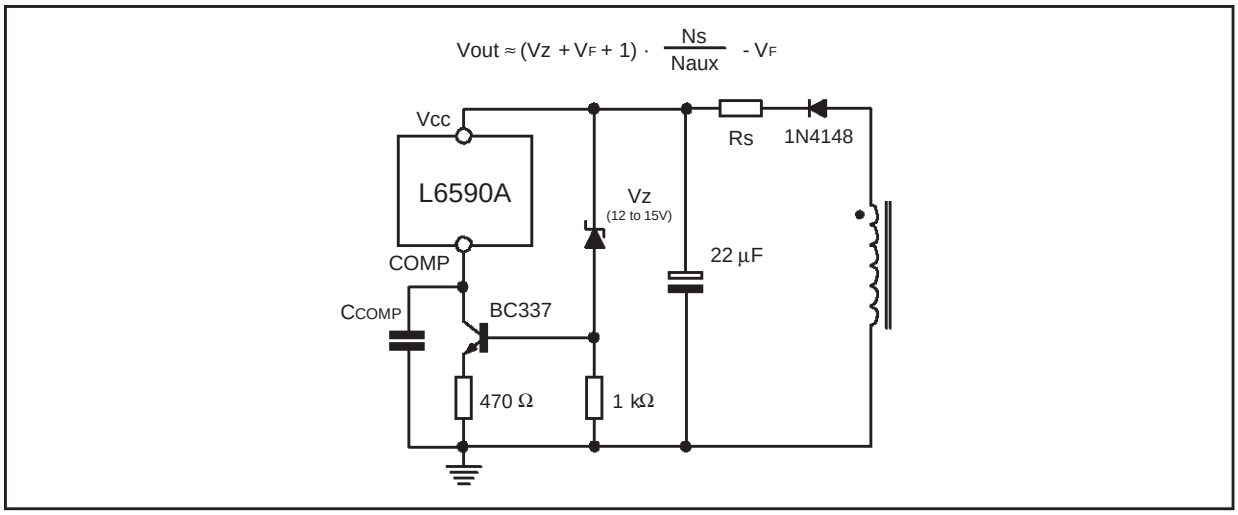


Figure 24. Compensation of voltage drop on long wires

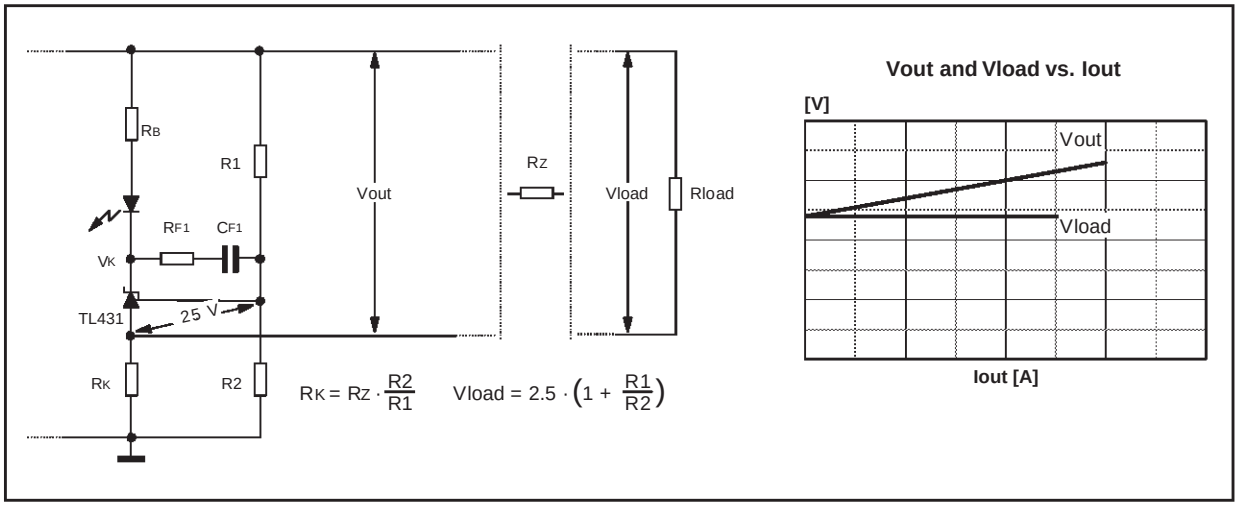
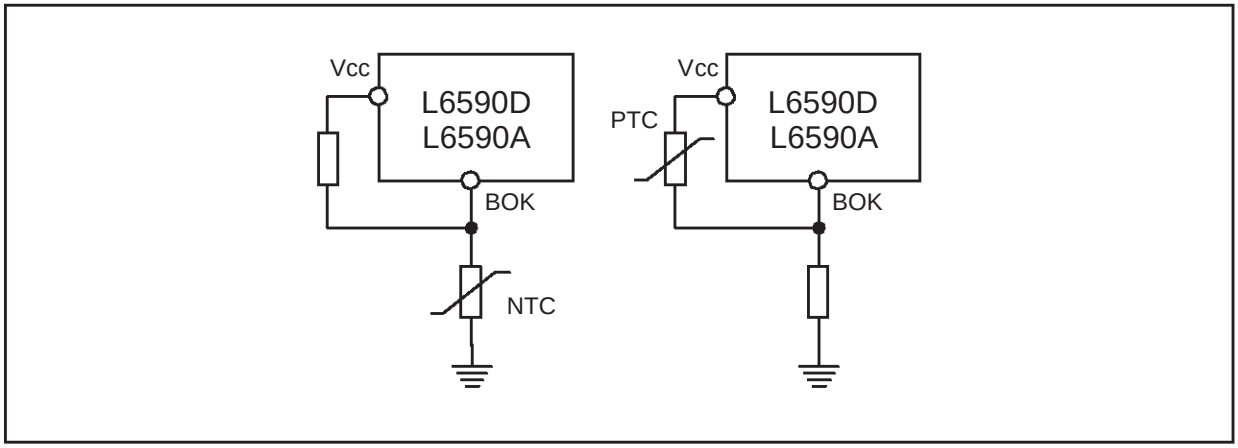


Figure 25. Thermal protection



The circuits of figure 17 can be used for reduction of the power throughput of the converter (a), or for stopping it completely (b), in case of overload, short circuit or feedback disconnection.

Circuit a) pulls the output of the error amplifier to ground if this saturates high and stays latched. The PWM is stopped and the converter remains idle until the V_{CC} voltage goes below the UVLO threshold, after that the latch turns off and the device is started again. The result is an intermittent operation that reduces the power throughput significantly ("hiccup" mode operation). A delay is provided to avoid improper activation at start-up.

Circuit b) works the same way but pulls low the supply voltage of the IC too. The latch is kept alive by the internal start-up generator, hence it is necessary to disconnect the input source to restart the converter.

Figure 18 shows how to implement a mains overvoltage protection. The system offers a precision better than ±5% since it uses the precise internal reference as a pedestal, so that the variations of the BJT threshold have a limited impact. Shutdown is not immediate, the output voltage is reduced progressively as the threshold is approached. For a sharper intervention use lower R_L, R_H values or higher R_E values. Note that in not-isolated or primary regulated configurations R_E is the low-side resistor of the divider that sets the output voltage.

Figure 19 shows a LEB (Leading Edge Blanking) circuit that blanks the spike (due to the transformer's leakage inductance) appearing at the rising edges of the voltage generated by the self-supply winding. This reduces the influence of the converter's load on the V_{CC} voltage. In a system with secondary feedback V_{CC} will drift less, in case of primary feedback load regulation will be improved considerably.

Figure 26. Remote ON/OFF control

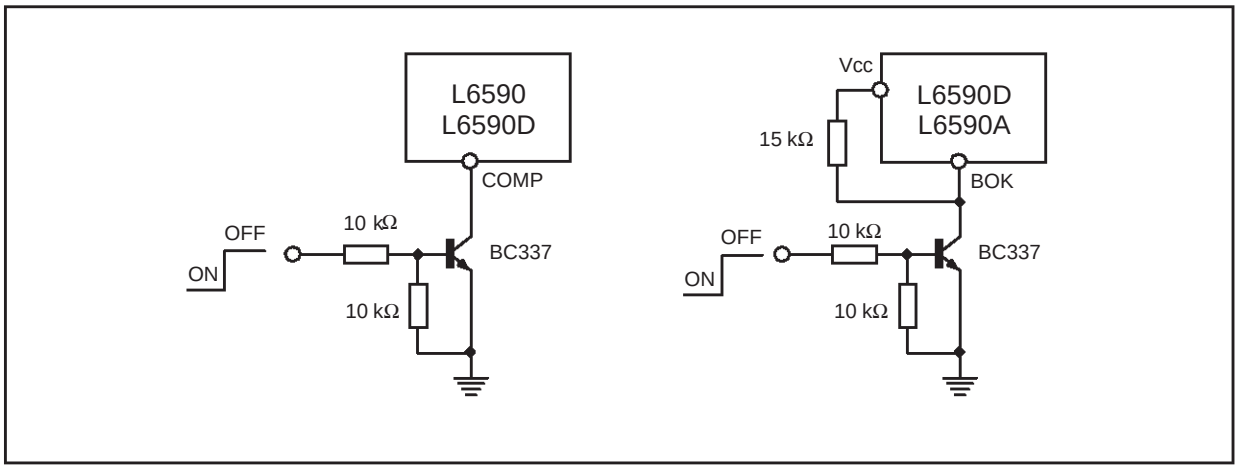


Figure 27. Soft-start

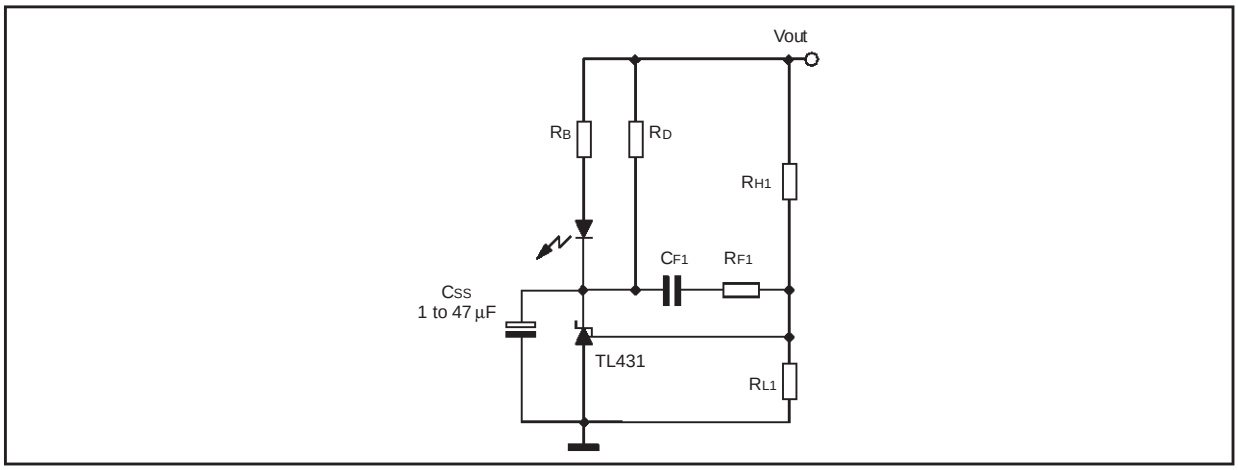


Figure 20 shows a very simple type of secondary feedback that can be used when the tolerance required on the output voltage, although not so tight as to require a precise secondary reference, is too stringent for primary feedback (e.g. because there is a very large load range). The resulting tolerance depends mainly on the zener voltage spread and its temperature variation.

In figure 21 an alternative connection of the phototransistor is shown. It is useful to achieve hiccup mode operation in case of overload or short circuit. It is useful also when the supply voltage of the IC experiences a very large variation (e.g. in battery chargers). The IC's OVP protection is bypassed by such configuration, but if the optocoupler failes the phototransistor will no longer be able to supply the IC, which will go into UVLO just like in case of overload or short circuit.

Figure 22 illustrates the circuit of figure 21 adapted to the L6590A, which is not provided with an E/A.

Figure 23 shows how to make a primary sensing feedback with the L6590A (which is not provided with an E/A) in converters where load regulation is not a concern.

In figure 24 it is shown how to arrange the feedback loop on the secondary side to achieve a perfect voltage regulation on the load when this is connected to the converter's output with a long cable, provided the total resistance Rz of the cable is known. This can be useful in AC-DC adapters.

Figure 25 shows a different use of the BOK pin: the thermal protection of a power component besides the IC, for instance the transformer or a secondary rectifier. The first solution (with an NTC) is preferred with primary regulation because Vcc is fixed by the feedback and the temperature threshold is then tightly determined. The second one is preferred in secondary regulation because Vcc may vary, thus precision is given by the abrupt change of the PTC resistance value at its critical temperature.

Figure 26 shows two possible solutions to turn on and off the device by means of a logic signal, while figure 27 gives a clue on how to realize soft-start to avoid excessive inrush current at start-up. C_{SS} is connected to a low impedance point, thus it has little effect on the feedback loop compensation. R_D is used for discharging C_{SS} when the converter is powered off.

Application Examples

Here follows a series of example circuits aimed at covering the most common applications that the L6590 family can address.

Figure 28. 10W AC-DC Adapter with primary feedback (L6590 and L6590D)

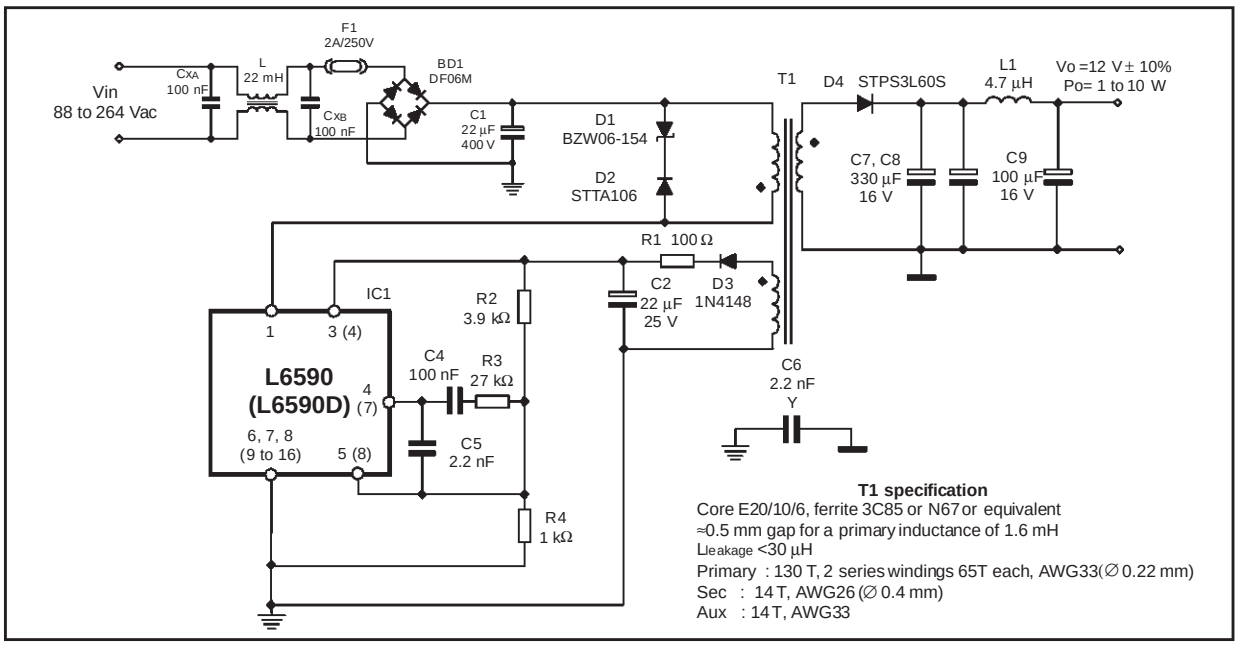


Figure 29. Not-isolated 10W AC-DC Adapter (L6590 and L6590D)

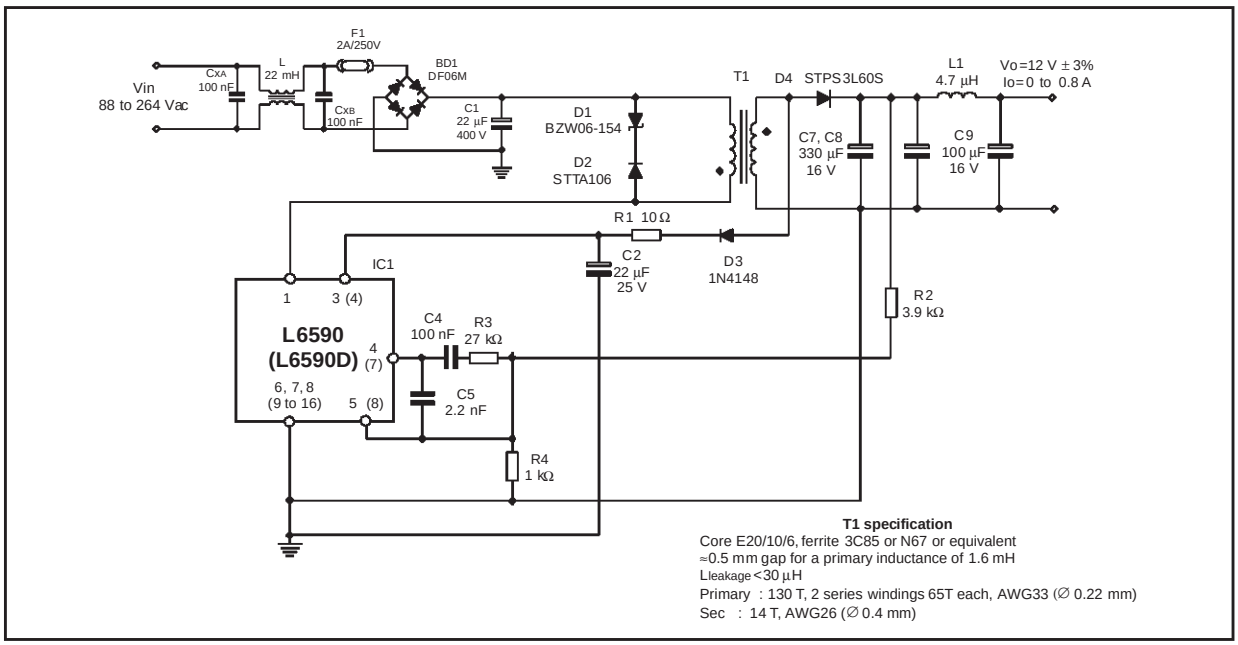
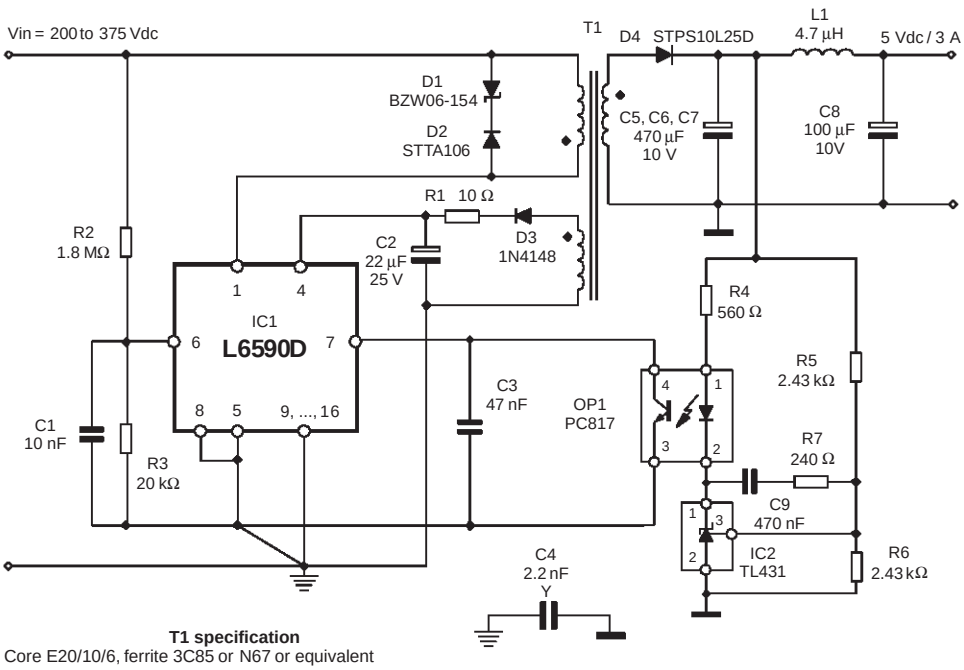


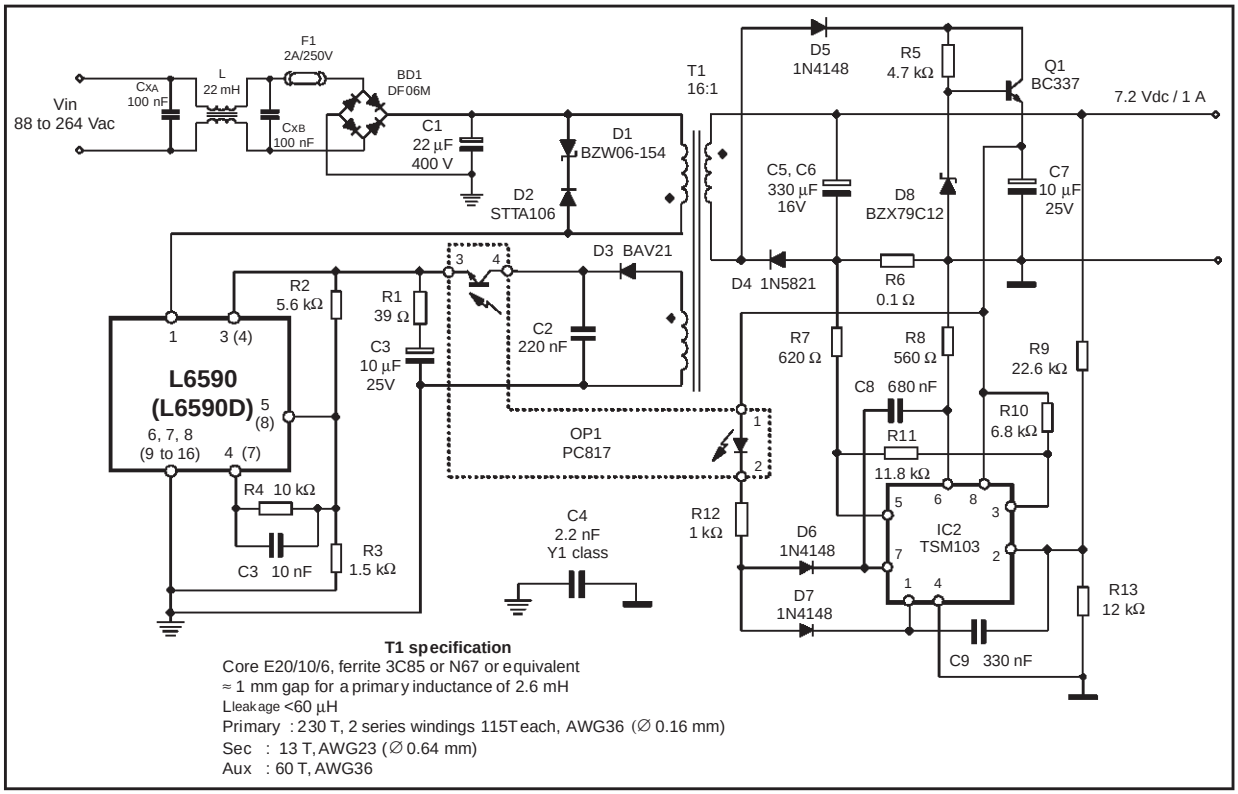
Figure 30. 15W Auxiliary SMPS for PC (L6590D)



T1 specification

Core E20/10/6, ferrite 3C85 or N67 or equivalent
≈ 0.9 mm gap for a primary inductance of 2 mH
Lleakage <50 µH
Primary : 200 T, 2 series windings 100T each, AWG33(∅ 0.22 mm)
Sec : 9 T, 2 x AWG23 (∅ 0.64 mm)
Aux : 21 T, AWG33

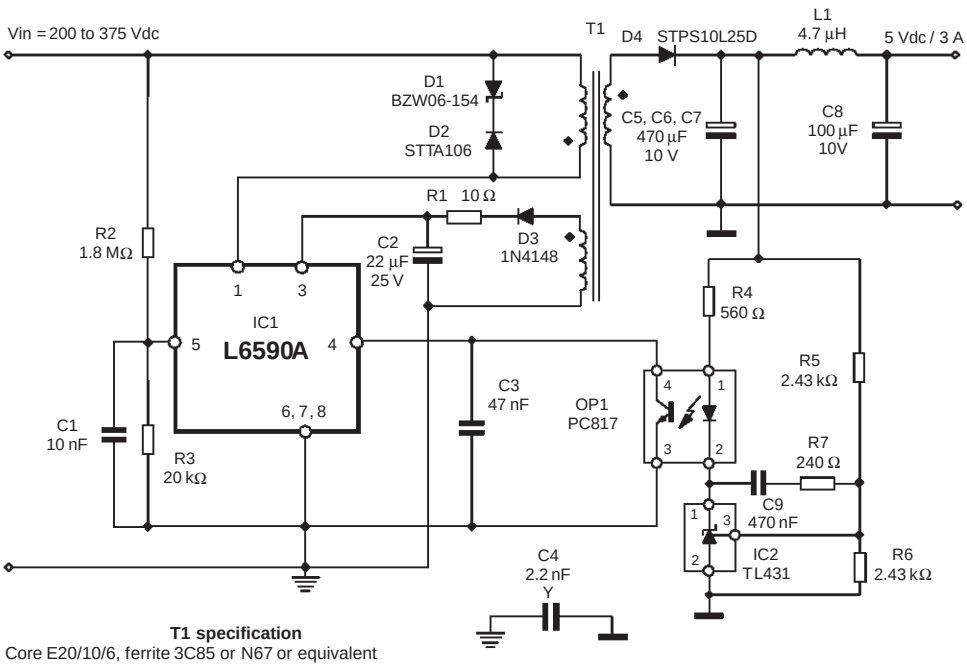
Figure 31. 7W Battery Charger (L6590 and L6590D)



T1 specification

Core E20/10/6, ferrite 3C85 or N67 or equivalent
≈ 1 mm gap for a primary inductance of 2.6 mH
Lleakage <60 µH
Primary : 230 T, 2 series windings 115T each, AWG36 (∅ 0.16 mm)
Sec : 13 T, AWG23 (∅ 0.64 mm)
Aux : 60 T, AWG36

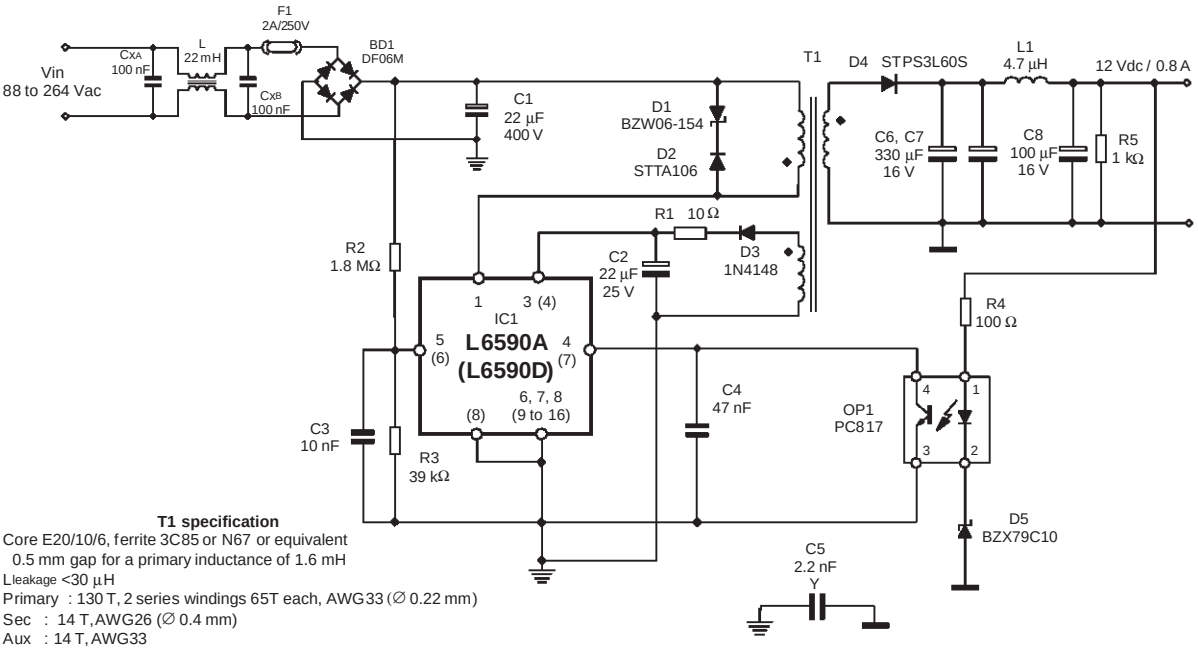
Figure 32. 15W Auxiliary SMPS for PC (L6590A)



T1 specification

Core E20/10/6, ferrite 3C85 or N67 or equivalent
≈ 0.9 mm gap for a primary inductance of 2 mH
Lleakage <50 µH
Primary : 200 T, 2 series windings 100T each, AWG33(∅ 0.22 mm)
Sec : 9 T, 2 x AWG23 (∅ 0.64 mm)
Aux : 21 T, AWG33

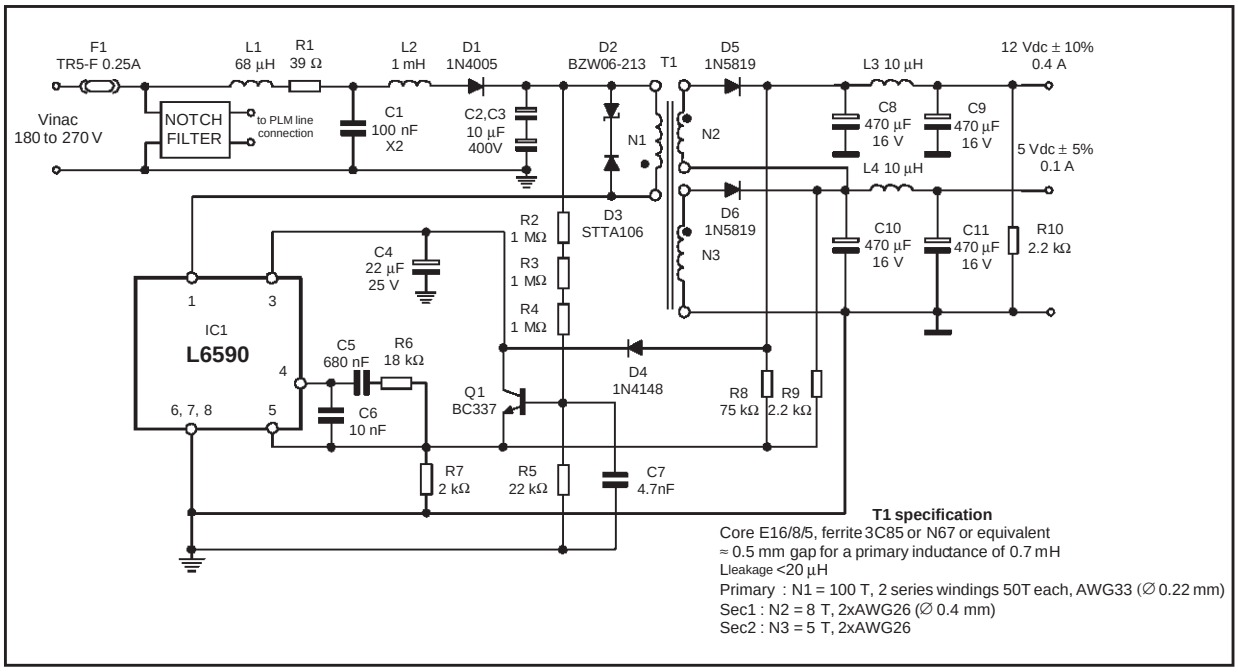
Figure 33. Simple 10W AC-DC Adapter with brownout protection (L6590A and L6590D)



T1 specification

Core E20/10/6, ferrite 3C85 or N67 or equivalent
0.5 mm gap for a primary inductance of 1.6 mH
Lleakage <30 µH
Primary : 130 T, 2 series windings 65T each, AWG33 (∅ 0.22 mm)
Sec : 14 T, AWG26 (∅ 0.4 mm)
Aux : 14 T, AWG33

Figure 34. Non-isolated 5.5W, European mains SMPS for PLM



Miscellaneous topologies

The following schematics show some topologies other than flyback that can be approached with the devices of the L6590 family.

Figure 35. Forward converter

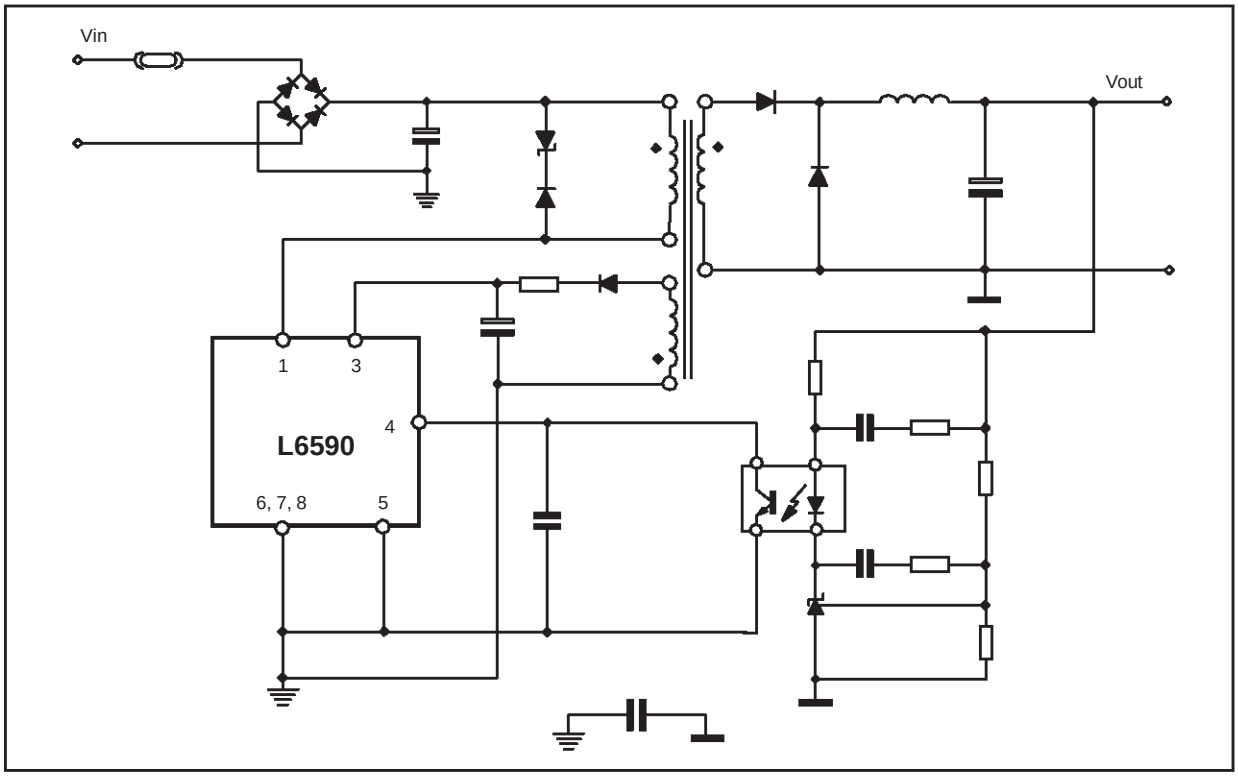


Figure 36. Boost Converter

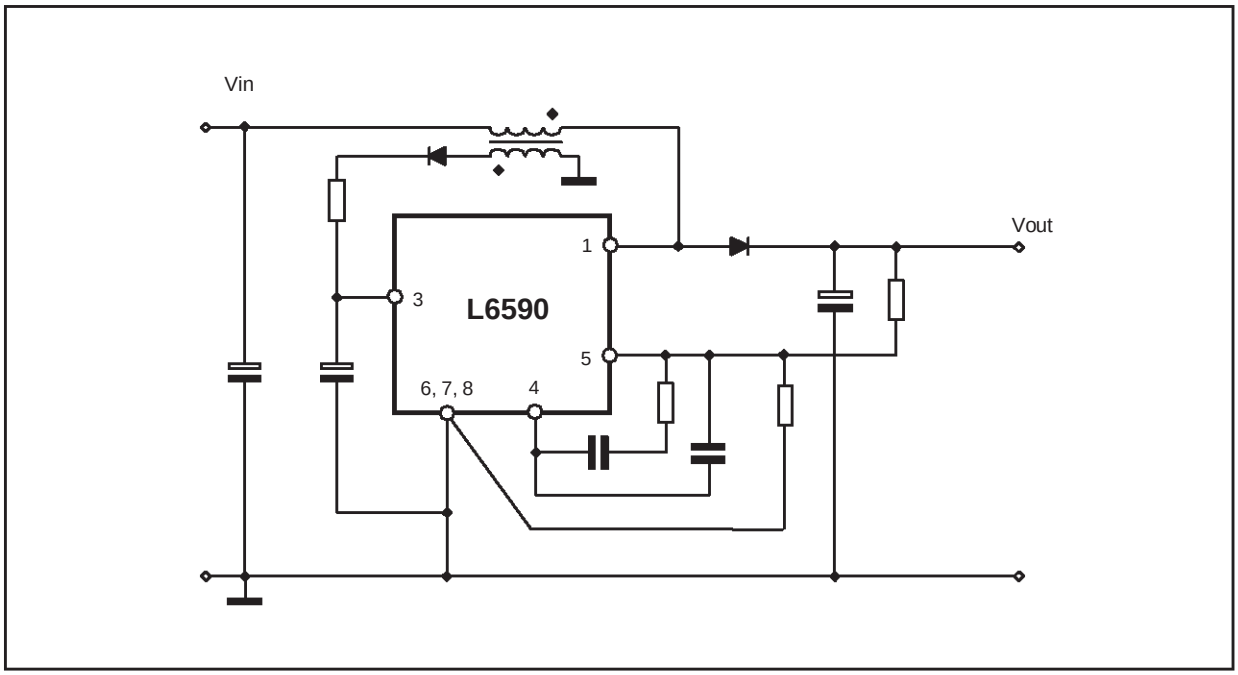


Figure 37. Voltage-boosted Boost converter

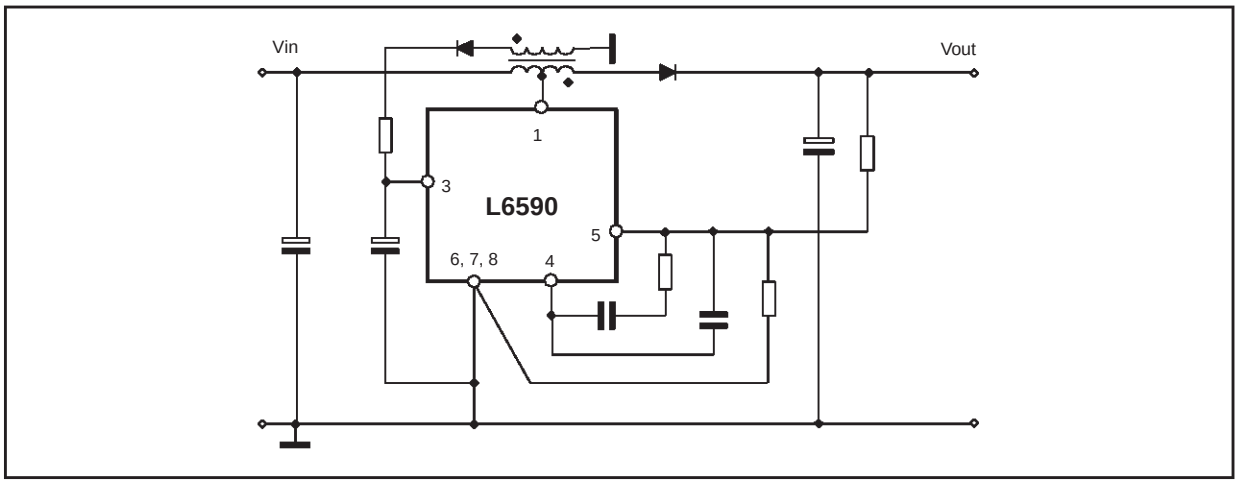


Figure 38. Current-boosted Boost Converter

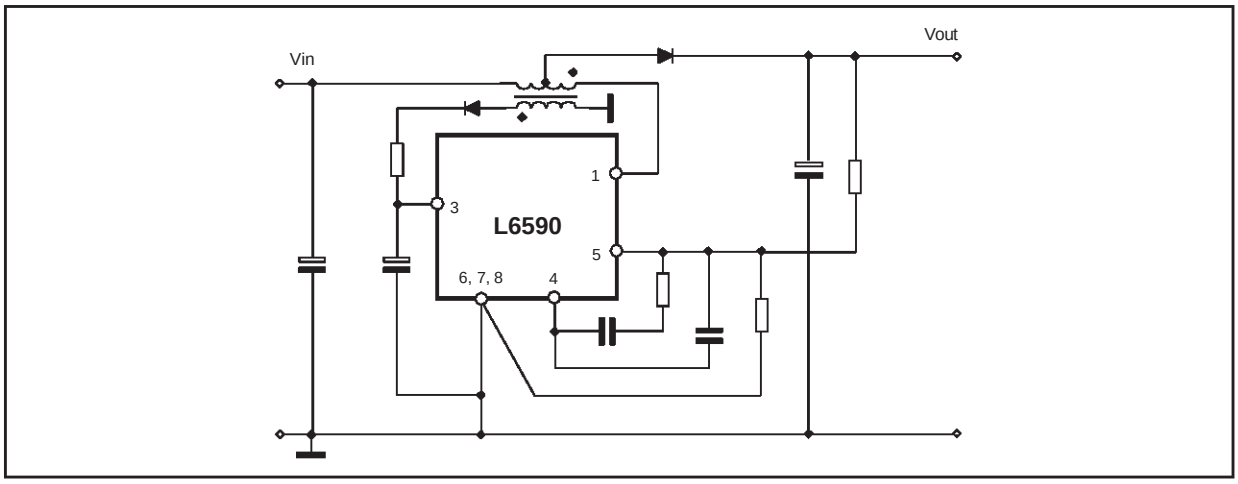


Figure 39. Positive Buck converter

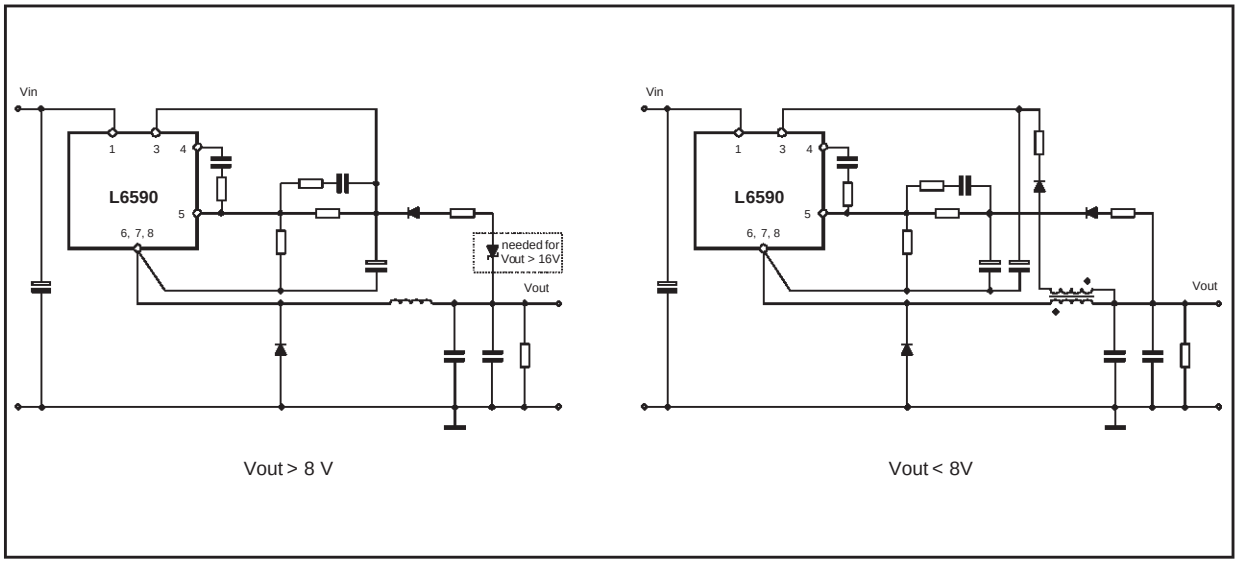


Figure 40. Negative Buck converter

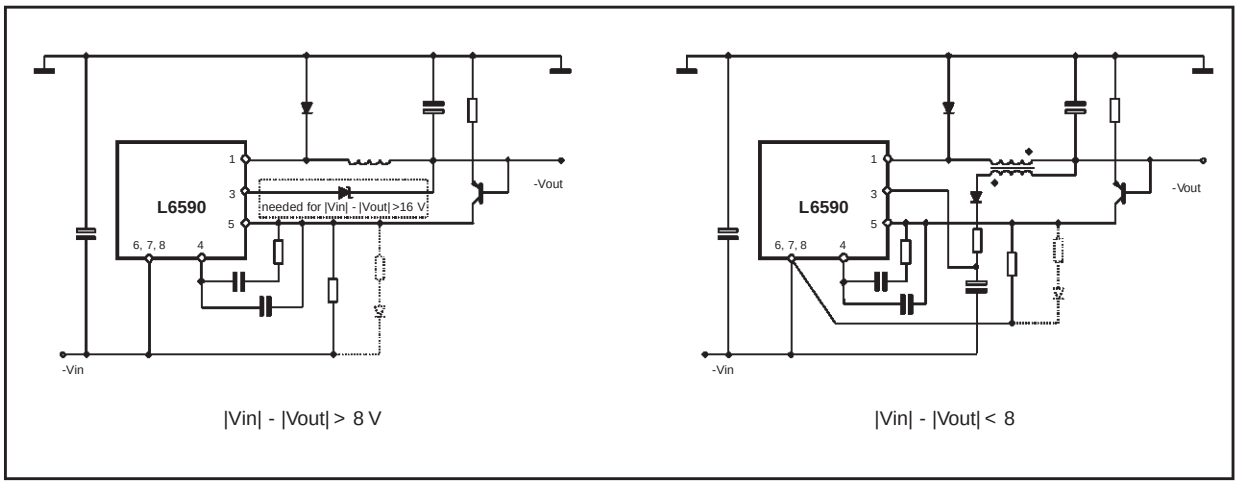


Figure 41. Positive-to-negative Buck-Boost converter

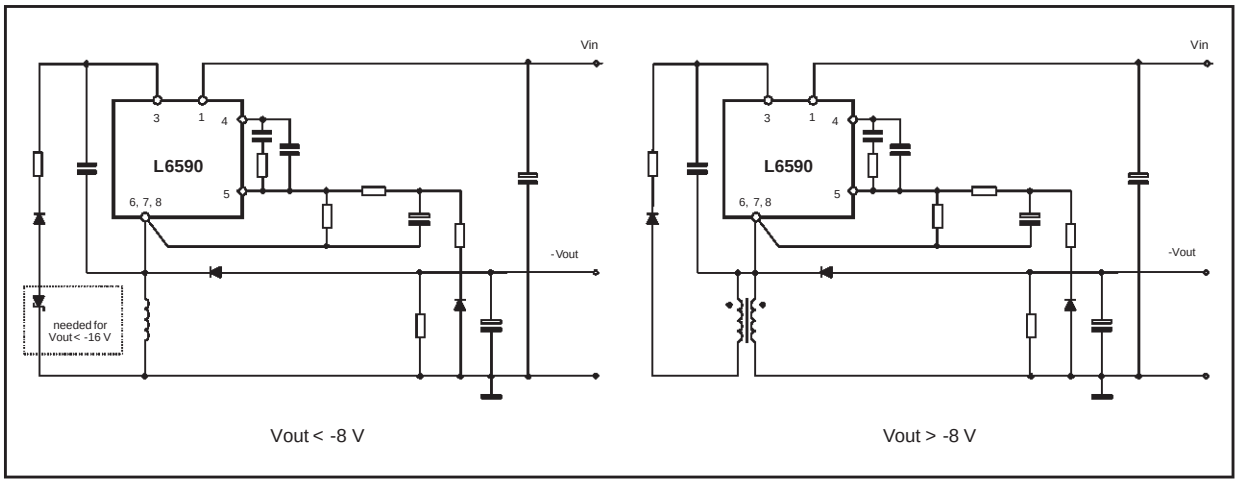


Figure 42. Negative-to-positive Buck-Boost converter

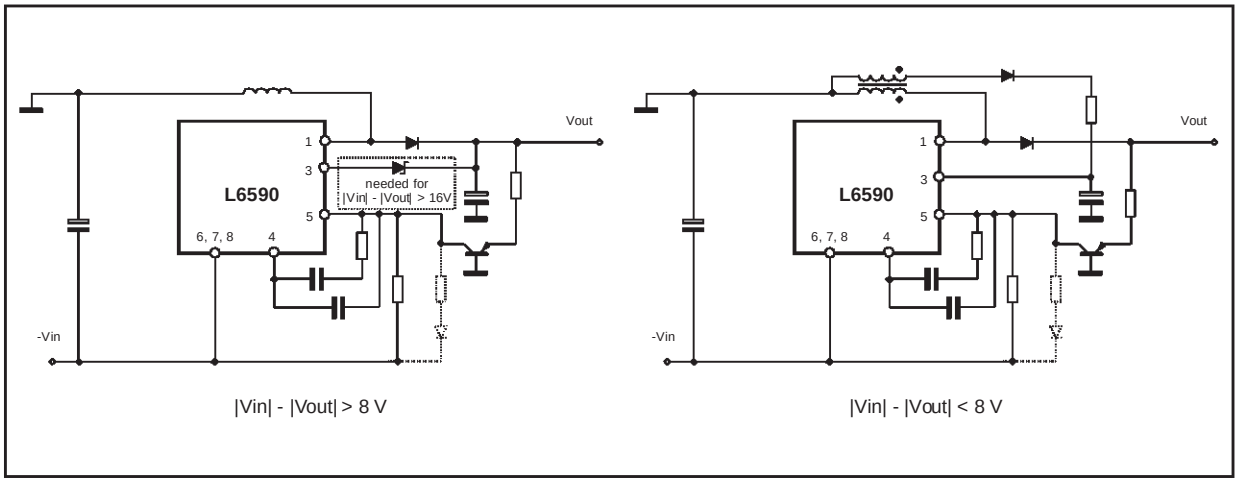


Figure 43. Cascaded-flyback converter

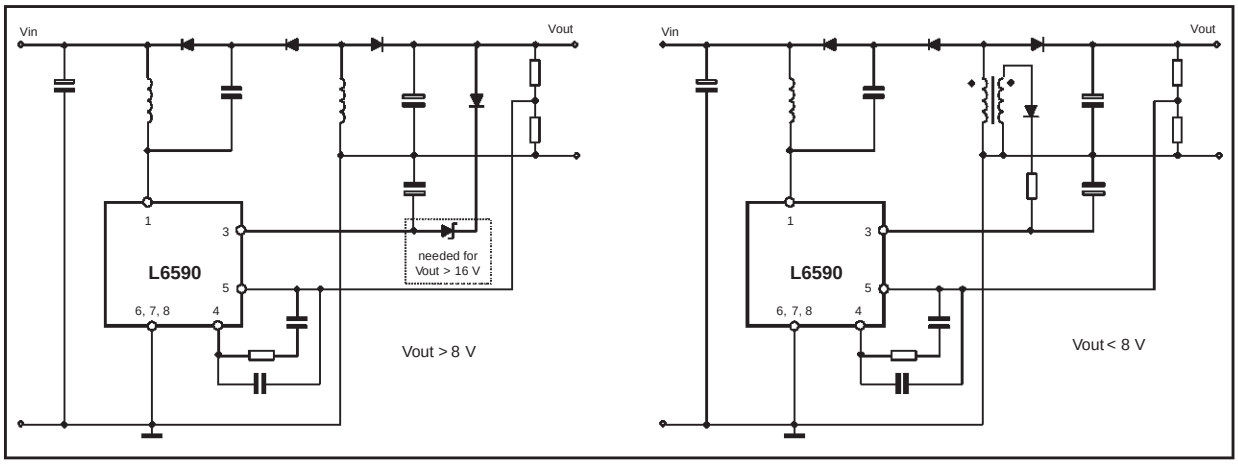


Figure 44. SEPIC converter

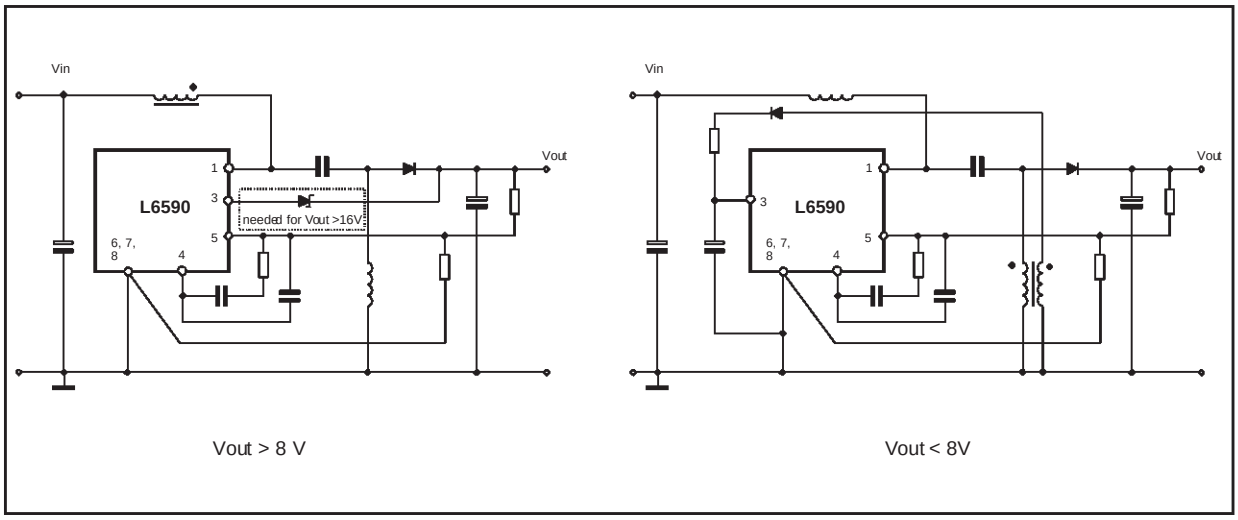
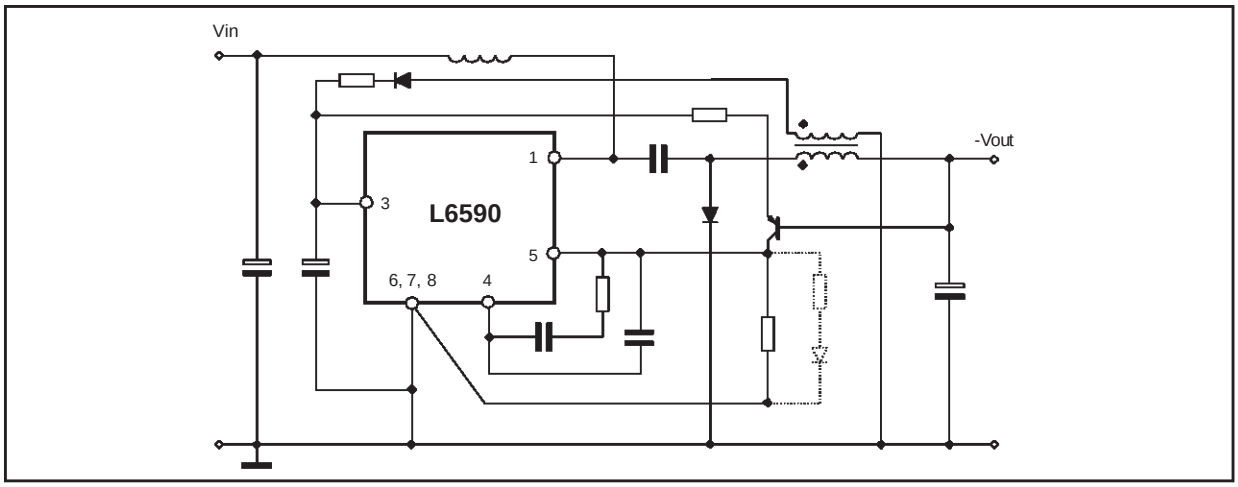


Figure 45. Cûk converter



The Forward converter of fig. 35 can use a smaller core than flyback because it does not store energy. This topology is suitable for generating low voltage, high current isolated output.

The Boost converter of fig. 36 provides an output voltage higher than the input voltage with no isolation. The maximum output voltage is limited at below 700V by the breakdown of the internal MOSFET and the maximum output-to-input voltage ratio cannot exceed 3.3 due to the maximum duty cycle of 70%.

The Voltage-boosted Boost converter of fig. 37 uses a tapped inductor to get an output voltage higher than the standard Boost converter. The price to pay for that is a reduced power capability. A clamp should be added to the drain pin to limit spikes due to the leakage inductance.

The Current-boosted Boost converter shown in fig. 38 uses a tapped inductor to increase the output power significantly, compared to the standard Boost. The price to pay is an increased peak drain voltage thus this configuration can be used if the output voltage is not too high. Also here a clamp should be added to the drain pin to limit spikes due to the leakage inductance.

The positive Buck converters in fig. 39 step a positive input voltage down to a lower output voltage. They use a special configuration with the ground pin of the device floating. This requires a bootstrapped supply voltage, thus a minimum load is required for a proper start-up and operation. Also the feedback is delivered with a bootstrap technique.

The negative Buck converters shown in fig. 40 step a negative input voltage down to a lower (absolute value) negative output voltage. The feedback uses a PNP as a level shifter and the optional diode and resistor can be used to compensate the temperature variation of V_{BE}.

The Positive-to-negative Buck-Boost converter in fig. 41 is a variant of the positive step-down of fig. 39 to generate a negative output from a positive input voltage. It can work as either step-up or step-down and requires a minimum load for a proper start-up and operation.

The Negative-to-positive Buck-Boost converter in fig. 42 is instead a variant of the negative step-down of fig. 40 to generate a positive output from a negative input voltage. It can work as either step-up or step-down and requires a minimum load for a proper start-up and operation.

The cascaded Flyback converters of fig. 43 work as a step-down and are useful for low power applications when isolation is not required and the input-to-output voltage ratio is very high. In fact it does not require as narrow duty cycles as the buck configuration does. The power capability attainable is however quite low.
Figures 44 and 45 show a SEPIC and a Cûk converter respectively. Both converters can be either step-down or step-up. The Cûk converter delivers a negative voltage, thus an additional winding is needed in any case for supplying the IC. Besides, the feedback uses a PNP as a level shifter. The optional diode and resistor can be used to compensate the temperature variation of V_{BE}.

REFERENCE

[1] ”Minimize Power Losses in a Lightly loaded Flyback Converter with the L5991 PWM Controller” (AN1049)

[2] ”Offline Flyback Converters Design Methodology with the L6590 Family” (AN1262)