

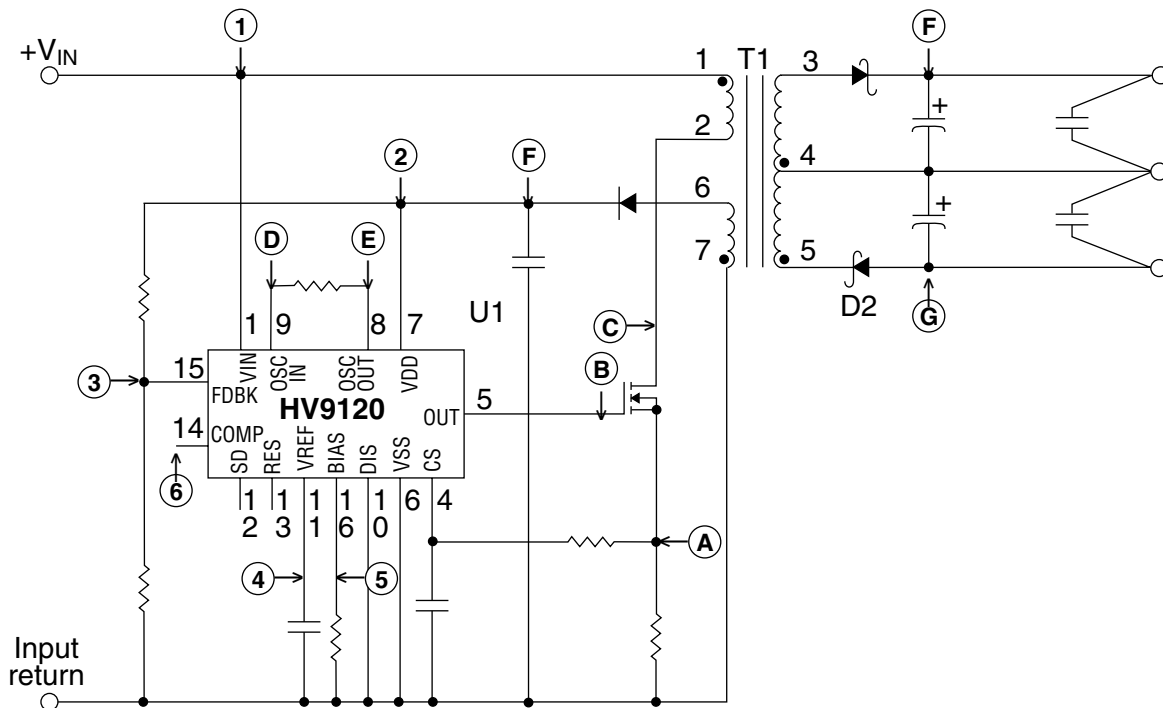
Expected Voltages and Waveforms from an HV9120-Controlled Flyback Converter

The following drawings provide details of the waveforms that one should expect to see at selected points around the converter circuit. For reference purposes, each voltage and time is defined only once across all drawings in the series. Thus, a T_7 or a V_3 means the same thing regardless of on which drawing it occurs.

In most circumstances, the waveforms will be as shown. However, it is possible that, because of certain circuit features of an individual converter, different waveforms may be observed.

Generally, though, if a waveform differs significantly from the ones shown here, it may be a symptom of a circuit which is not operating as expected, and a valuable clue as to what to do about correcting the improper operation.

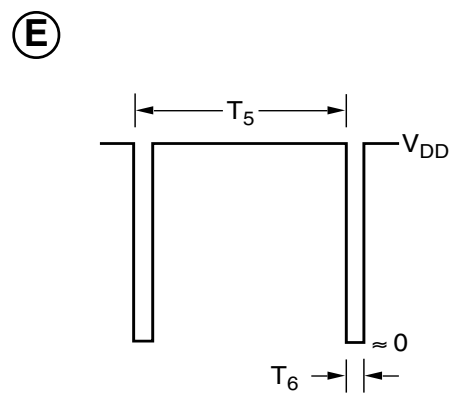
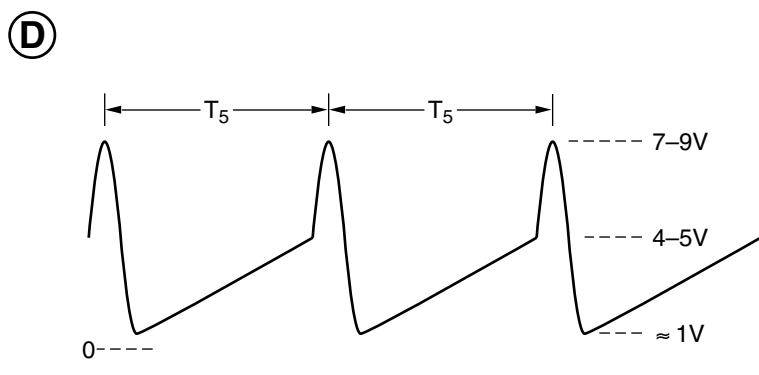
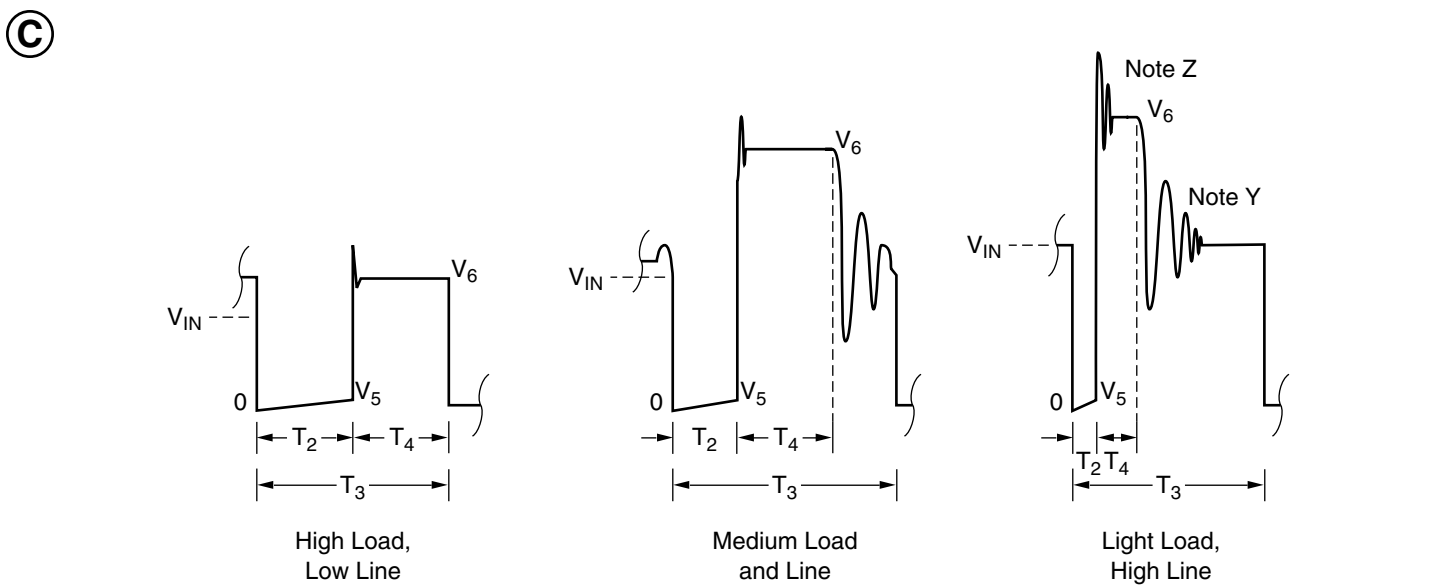
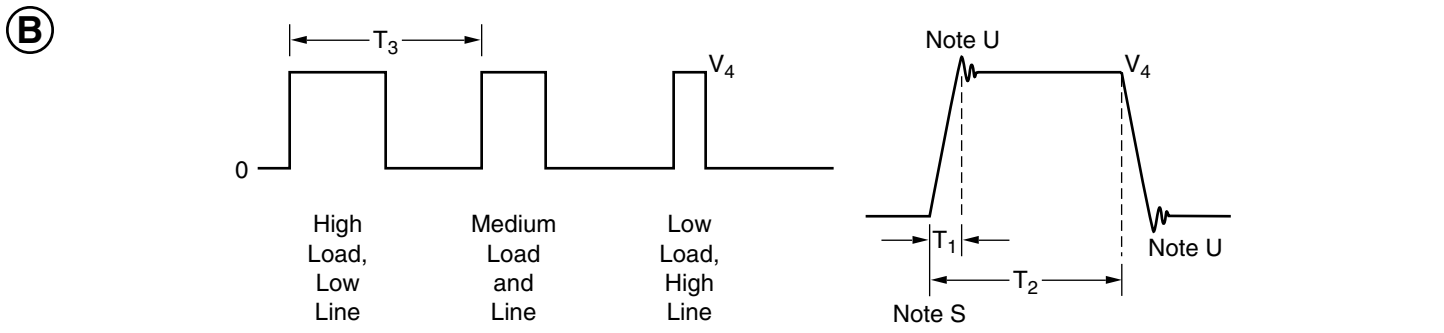
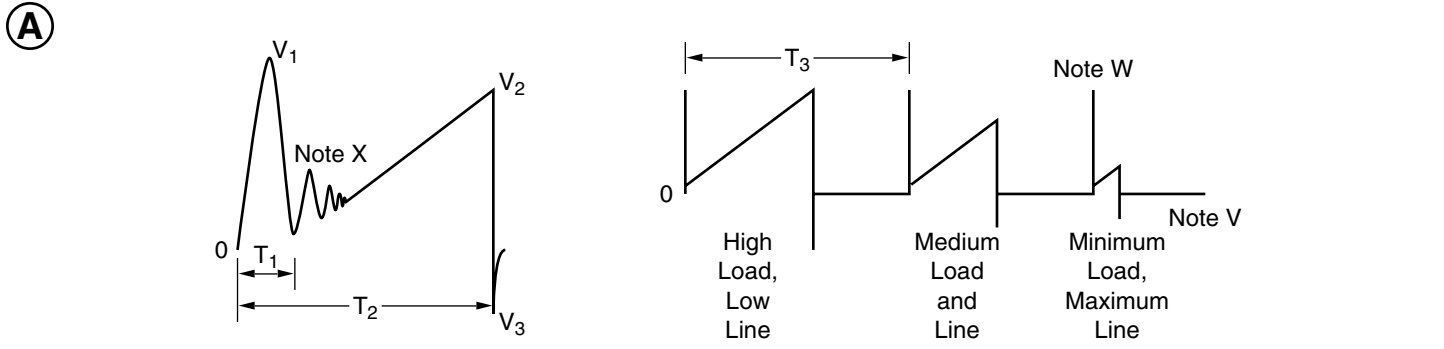
It should also be noted that, though the sketches were based on a converter using an HV9120, results will be very similar with any of the PWM ICs or SMPS ICs in the HV91 family of products.



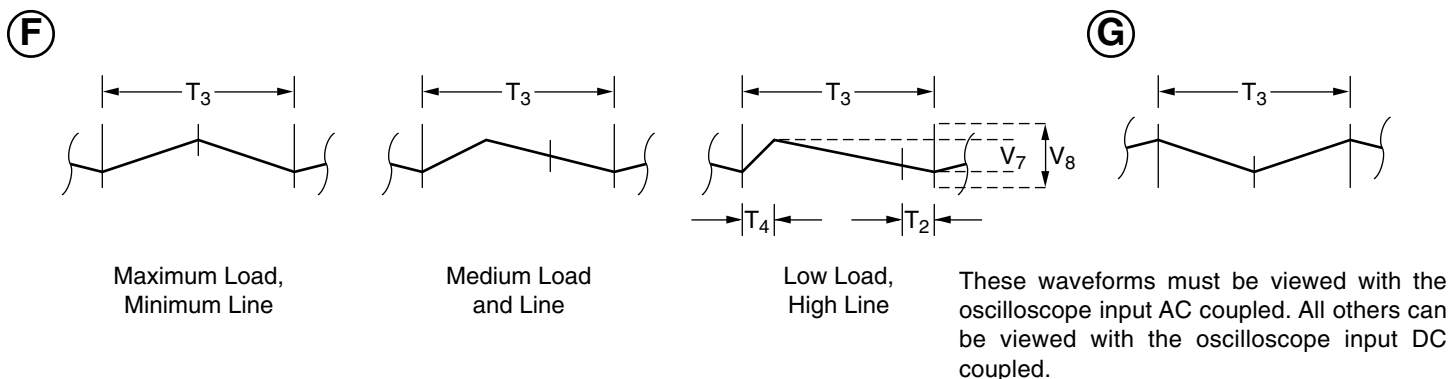
Expected Voltages

- 1 V_{IN}
- 2 If the converter is running, this will usually be $10V \pm 1\%$. For some converters, a different voltage may be used. If the converter is shut off or disabled (by removing the FET, for example), this will be $9V \pm 5V$.
- 3 With the converter running and regulating, this will be very close to $4.0V$. Be careful measuring 3. Pin 15 is a high impedance node and is very sensitive.
- 4 $4.00V \pm <2\%$.
- 5 $(V_{DD} - 0.9)$ to $(V_{DD} - 4)$ depending on the value of bias resistor chosen.
- 6 If V_{DD} is below its regulated value, this will be $6-8V$. If V_{DD} equals its regulated value, this will be between $1.8V$ and $3.2V$. If V_{DD} is greater than $10V$, this will be very close to zero. This last condition can only be observed as a transient, when a large load is removed from the output or when a large rise in V_{IN} occurs.

Expected Waveforms



Expected Waveforms (continued)



V₁ Can be any height. For best results, should be less than approximately 2.5V. Height is dependent on Q_G of MOSFET, transformer interwinding (not interwinding) capacitance, t_{RR} of output diodes, and board layout. Q_G of FET is usually main component, as can be shown by operating PWM with FET drain open.

V₂ Between 0 and 1V when unit is regulating. Actual value depends on the energy the regulator needs to provide to the load. May be as high as 1.4V during startup or overload.

V₃ Usually between .5 and .7 of V₁. If it is much less than half of V₁, check t_{RR} of output diodes.

V₄ V_{DD} (pin 7).

V₅ (R_{DS(ON)} • I_{PEAK}) + (R_{CURRENT SENSE} • I_{PEAK}). This is shown only to note that there is a small ramp at the bottom of the switch's on-time waveform.

$$V_6 \quad V_{IN} + (V_{OUT} \times \frac{N_{OUTPUT WINDING}}{N_{INPUT WINDING}}) \text{ or}$$

$$V_{IN} + (V_{OUT} \times \sqrt{\frac{L_{OUTPUT}}{L_{INPUT}}})$$

V₇ Output ripple voltage depends on size and particularly on ESR of output capacitors. Beware of cheap aluminum electrolytics!

V₈ This wouldn't exist if capacitors were perfect. The largest one is the main switch turning off. The next largest is the main switch turning on. The small one (which may not exist)

is the diodes turning off. To reduce these, parallel the main capacitors with ceramics, mylars, or both, with good high frequency characteristics. The noise is coupled into the outputs by the interwinding capacitance of the coupled inductor and the layout. Sometimes using a Faraday shield on the coupled inductor helps, but generally mylar capacitors are an easier way to deal with it.

T₁ Should be kept to ≤80nsec, or current sense will end cycle prematurely. Width is dependent on Q_G of FET, ESR, and size of the capacitor between pins 6 and 7 of the IC.

T₂ Anywhere from approximately 80nsec (minimum) to 1/2T₃ for HV9120 (for HV9123 can be >1/2T₃), depending on line and load. Length is directly proportional to load, and inversely proportional to line.

T₃ Determined by oscillator resistor value (= 1/F_{OPERATION}).

T₄ This is the section of t_{OFF} during which the coupled inductor is discharging into the load. Its actual width is dependent only on load. At maximum load it is close to 50% of T₃. At smaller loads it is less. During the time that the inductor is discharged into the output, the output waveform ramps up. The rest of the time it ramps down.

T₅ 1/2 of T₃ for HV9110, HV9120 and equal to T₃ for HV9113, HV9123.

T₆ 100nsec +100% -50%. Actual time depends on V_{DD}, the size of clock resistor, additional clock loading (if any), whether the part is an HV9110/20 (faster) or an HV9113/23 (slower), and process variation.

Notes

S — The rise time of T_1 is equal to the entire width of the leading edge spike on waveform A.

U — Due to the heavy capacitive load from the FET gate, and clamping by body diodes of the FETs in the IC driving the external FET, there is usually very little ringing on this waveform.

V — At extreme low load and/or extreme high input, the ramp section of the waveform can virtually shorten until it disappears. Current starts ramping up in the inductor, however, almost as soon as the leading edge spike starts rising.

W — The leading edge spike is caused when the PWM charges the gate capacitance of the FET. The trailing edge negative spike is caused by gate discharge.

X — A little ringing during the transition from leading edge spike to ramp sections is normal. If there is a lot of ringing here, check board layout.

Y — This ring looks horrific, huge, and ugly. It is unavoidable and innocuous—it contains almost no energy (not enough to forward bias a diode, anyway). What is ringing is the FET's drain capacitance and the coupled inductor's input side inductance. Eventually the ringing will die out, and the voltage level will return to V_{IN} .

Because this waveform appears on the MOSFET drain/coupled inductor interface, it will also be visible on all other windings of the coupled inductor (as shown or inverted).

Z — Ringing when the main switch turns off is unavoidable. The energy to do this comes from the leakage inductance in the coupled inductor. Leakage inductance should be minimized because too much of a spike here can overheat or damage the main switch.