Application Note AN-8005

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IGBT Power Electronics Teaching System
Principle for sizing power converters

Inside the box

Before unpacking, please ensure that the following elements are inside the box.
- The stack itself
- A test certificate, which is a guarantee of safe working of the stack
- The technical description

Very important safety recommendations

To avoid damage to the converter and for the safety of the operator, it is strongly recommended to follow these instructions:
Always monitor the voltage at the capacitor bank. It must never exceed the maximum value of 750 Vdc, as there is no protection against DC over-voltage embedded in the Power Electronics Teaching Unit. After the tests, the capacitors may remain charged for a couple of minutes. One must anticipate that the DC voltage limit shall never be exceeded when designing a control unit board. When powering the unit, a pre-charging device (a choke or a resistance) should be inserted to prevent very high charge currents. Never carry or move the device while it is electrically connected to anything. The error signal from the drivers must be taken into account in the control process. When connecting the command signals, it is preferable to use a anti-static protection bracelet. Never exceed the maximum allowed current (30 A). Connect a circuit breaker between the supply voltage and the converter. A thermal contact switch has been placed in the heat sink, close to the warmest point, to disconnect the circuit in case of abnormal heating of the heat sink. As a protection device, it should be connected in series with the driver power supply.

The interfaces / connectors

Preliminary remark

Even though this power electronics teaching system has been designed in order to avoid all risks of electrical contact, lethal high voltage can be present in the connectors. All connections should be made taking care that all security measures have been undertaken. In particular, the integrity of all cables should be checked prior to any exercise. For safety reasons, there is no direct access to the gate-emitter connections on the high-power level, which is the voltage triggering signal of the IGBT. If you intend to monitor this charge-discharge of the gate of the IGBT, please remove the side covers but **disconnect the power supply**. For safety reasons the covers should always be attached when power is applied. Please note, with the covers removed there is the risk of electrical shock. Only qualified people should work on the system with the covers removed.
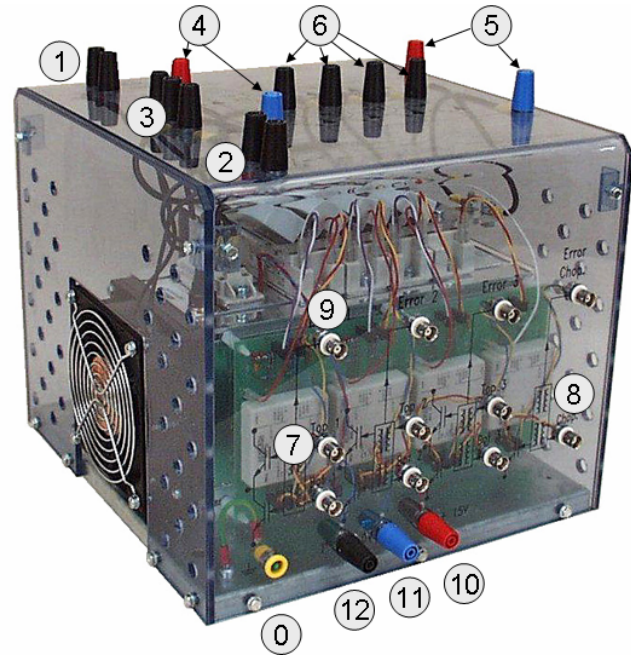
N°	Type	Function	Voltage level	Max Current level
0	Grounding panel socket	Earth connection	0V	30 A
1	Banana connector 4mm	Fan power supply	230V/50Hz	1 A
2	Banana connector 4mm	Thermal trip	15V	5 A
3	Banana connector 4mm	Rectifier input	230 / 400V	30 A
4	Banana connector 4mm	DC rectifier outputs	600 VDC (Red is positive, Blue is negative)	30 A
5	Banana connector 4mm	DC IGBT inverter inputs	600 VDC (Red is positive, Blue is negative)	30 A
6	Banana connector 4mm	AC IGBT inverter + chopper outputs	400 VAC / 600 VDC	30 A
7	BNC coaxial insulated, 50 Ω	PWM input of inverter	C-MOS logic 0/15 V (shield is internally connected to driver's 0V), 0V =open IGBT, 15 V = closed IGBT	1 A

8	BNC coaxial insulated, 50 Ω	PWM input of brake chopper	C-MOS logic 0/15V (shield is internally connected to driver's 0V), 0V =open IGBT, 15 V = closed IGBT	1 A
9	BNC coaxial insulated, 50 Ω	Error output	C-MOS logic 0/15V (shield is internally connected to driver's 0V)	1 A
10	Banana connector 4mm	15V driver power supply	15V	5 A
11	Banana connector 4mm	0V driver power supply	15V	5 A
12	Banana connector 4mm	Temperature sensor	0-5V	1 A

### How to integrate the stack in the application

The rectifier outputs are not directly connected to the capacitor bank, and it is not recommended to link them directly. To avoid high inrush current, which may be destructive for the capacitors, it is necessary to place a pre-charging resistor (that could be by-passed after charging the capacitors), or a choke between the rectifier and the capacitors. First, switch on the driver supply.

The error signal must indicate no error (i.e. +15 V). If this is not the case, there is a defect. Maybe the driver voltage is less than 13 V. Next, you should switch on the power. If possible, gradually increase the voltage using an auto-transformer. Otherwise, a passive element for charging should be placed between the rectifier and the capacitors bank.

The components of the power electronics teaching system

The heat sink and the fan

As explained later in more detail, it is of critical importance to dissipate the losses generated by the transfer of energy through the semiconductors. For this purpose, these are placed onto an aluminium heat sink (aluminium is a good trade-off of a thermally conductive metal, reasonable price, easy to industrialize), and the heat is dissipated from the power semiconductor to the aluminium by conduction. In most cases, for cost reasons, the heat sinks used in power electronics are of the extruded type. The heat sink used in this device is a P3/250, which means a profile of the extruded type P3, 250 mm long. The heat sink has one major thermal characteristic: its thermal resistance, defined as the level of elevation of temperature for a power dissipation of 1W. To dissipate the energy from the aluminium heat sink in the air, a fan creates air circulation on the fins for forced convection. The heat sink creates a pressure drop on the air flow, a function of the geometry of its profile and its length. The axial fan is defined by its pressure vs. flow curve characteristic. It can be supplied at 50 or 60 Hz, but its performance is slightly modified as can be seen from the curves. One can determine the approximate working point (air flow, working pressure) of the fan by crossing the pressure drop curve of the heat sink with the pressure vs. flow of the fan. The intersection gives an air flow estimation inside the fins of the heat sink. An additional safety margin should be

Figure 1 : Fan and heat sink characteristics
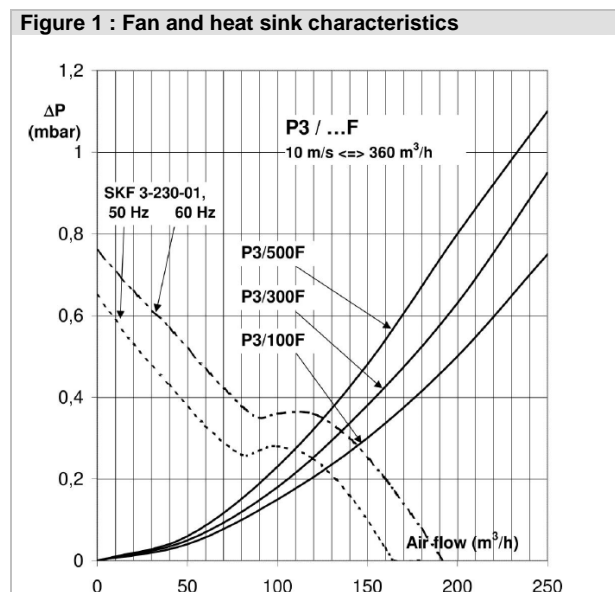
considered, for example if the air channel is obstructed by other elements which may add parasitic pressure drop, and reduce the fan output power.

The drivers

The driver is critical as it controls the IGBT, its protection, as well as the protection of the system and the user.
Its purpose is:
- Amplifying the logic signal ON/OFF and delivering high peak current (some amps) at switching to the gate. Noise suppression of the input signal is necessary for reliable performance. This current is delivered through the gate resistors (Ron and Roff), fixed by the user, and which determine the dynamic response of the IGBT.

- Monitoring the errors: power supply under-voltage, short-circuit. A short-circuit is detected by monitoring Vce, the voltage drop between collector and emitter of the IGBT. As the current increases,, the Vce(sat) (= at passing state) becomes higher. The two parameters (Rce, Cce) define the values and time delays for the comparison of an internal reference with the monitored value of Vce(sat). After detection of the error, the driver should have the appropriate answer, which is switching off the IGBT.

- Interfacing and isolating the primary circuit from the secondary directly connected to the high power. It prevents the high potential of the secondary side from affecting the primary side, which would be dangerous, yet allows the control signal to be transmitted between both parts. It is a matter of safety and reliability.

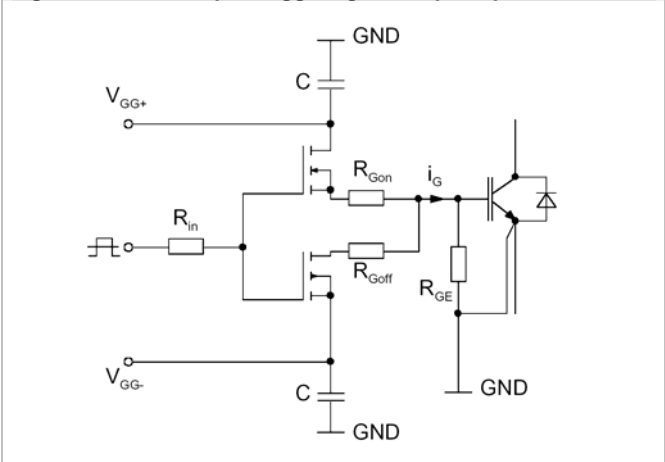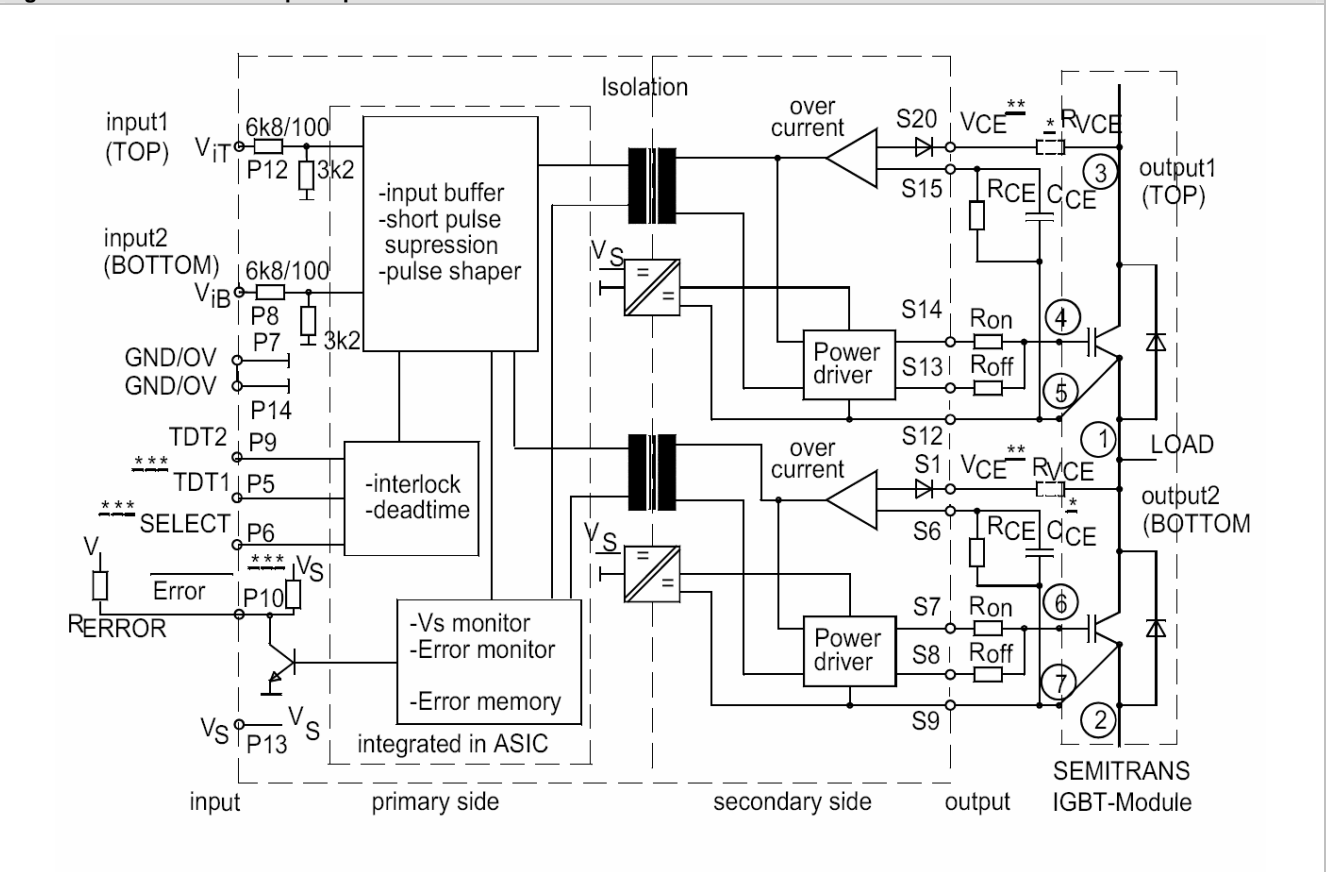**Figure 2 : Driver output, triggering circuit principle of the IGBT**

Figure 3 : Driver schematic principle of the SKHI 22A driver core

The drivers are based on 3 SKHI 22 A-R cores, each one controlling an inverter leg (both "Top" and "Bottom" IGBTs of one single module). One driver can control modules in parallel to increase the current capability, but that is not done in this application. The SKHI 22 A-R are described in detail at www.semikron.com. They must be powered with 0/15 V, and the power supply must be able to deliver a current above the drivers consumption (160 mA / driver max). The error signal is negative logic, i.e. it gives a +15 V signal when no error has occurred. You should integrate this monitoring in your command. If a fault condition is detected, the driver stops and the input pulses are ignored. The error latch is reset by forcing both inputs to 0, and removing the error cause. After 9µs, the error signal returns to 15V. Please note that the drivers are independent from each other. All the necessary precautions should be taken to shut the system off when an error condition is sensed. The SKHI 22 A-R is equipped with an internal 10 kΩ pull-up resistor versus Vs. Input signals to the driver: 0 / + 15 V stabilised power supply (banana-type connectors), C-MOS signal (0/15 V) for command (BNC connectors).

The rectifier SKD 51/14

This is a 3 phase diode-rectifier, isolated power module. It should not be used for a network higher than 440V_{AC}. This rectifier can be used in single phase configuration also, by leaving one branch of the rectifier disconnected.

The IGBT modules SKM 50 GB 123 D

Each of these modules is an inverter leg, and is made of 2 IGBTs with an anti-parallel diode, connected in series, of which the middle point is at terminal 1. The top IGBT collector is at terminal 3 and the bottom IGBT emitter is at terminal 2. The IGBTs are forced closed by a 15V signal between the gate (terminals 4 -resp 6) and the associated emitter (gate 5 –resp 7) and forced open by a –15 V order on the same terminals. These control signal voltages are delivered by the SKHI 22 AR, driver core through an additional gate resistor whose value is 30 Ohms. These resistors are soldered on the printed circuit board of the drivers. The purpose for this resistor is to limit the charging current of the gate, and consequently, the collector-emitter over-voltages commensurate to the parasitic inductance. Conversely a higher gate resistance increases the switching losses. The chosen value is always a trade-off between protection of the IGBT and the admissible losses. Moreover, the choice of this value will have a significant influence on the dV/dt spectrum, which has a real influence on the EMC characteristics of the converter. The choice of a gate resistor is of critical importance.

The filtering capacitors

The filtering capacitors are electrolytic capacitors, their individual value is 2200 µF/400 V, 2 connected in series, 2 in parallel. The equivalent capacitor of the complete DC bus is 1100µF/800 V. Theoretically, this value is to be determined by the desired filtering quality (capacitance / voltage) . Practically, for electrolytic technology, the RMS current admissible in the capacitors is the main sizing parameter, and manufacturers often place more capacitors than required just because of current limitation on the capacitors. The value of the current depends on the application, and the maximum allowed value by the capacitors is 19,1 A at 40°C or 8,2 A at 85°C. Our experience shows that this sizing fulfils almost all applications in the range of power addressed by the Power Electronics Teaching System.

Why is the current limited in the capacitors

The equivalent model of a capacitor is given below. For a given current, the losses are approximately Rs.I², and heat up the core of the capacitors.The LTE (Life Time Expectancy) is highly dependant on the hot spot temperature, according to a rule of the type,

$$K \cdot 2^{\frac{(T\max - Ths)}{10}}$$

where T_{Max} is the maximum temperature allowed, and T_{hs} the Hot Spot Temperature (inside temperature). Reaching an internal value of more than 85-90°C may not only considerably reduce the lifetime of the product, but may also lead to explosion risks. There are different capacitor technologies, but today the electrolytic type is the best fitted to the range of power and voltage of most applications in power electronics (from 1 kW to 1 MW and 200 V_{DC} to 1000

V_{DC}). This is due to their high capacitance, high voltage and medium current. Their main limitations come from a relatively high internal resistance R_{se}, which limits the RMS current – which has a direct effect on the lifetime. Some mounting technologies propose to dissipate the heat from inside the capacitor to a heat sink, or by creating an air circulation around the capacitors.

How to put capacitors in series

When forcing a constant voltage to ideal capacitors put in series, the capacitor can be considered as an open circuit, and the voltage should be equally shared between the capacitors. However, a parasitic leakage resistor (R_{leak}) causes a leakage current inside the capacitors at no load. In the case of 2 capacitors in series (or more), the equivalent model will then be a dividing bridge whose voltages are defined by the ratio of the leakage resistances in series. As the values R_{leak} are highly variable, since they are a consequence of imperfections in the capacitor and the manufacturing process, the voltages may vary widely, leading to a dangerous steady state DC voltage on one capacitor. Attention: Applying a DC voltage higher than its rated voltage to an electrolytic capacitor may lead to its destruction by explosion. To avoid differences in the voltage across capacitors, each capacitor must be connected in parallel to a balancing resistor, whose value must be much smaller than R_{leak} (about 1/10th). This resistor value is more accurate and stable, hence the voltage balance is much better. The principle of no-load charging is shown here below, using a realistic 50% internal parasitic resistance difference.
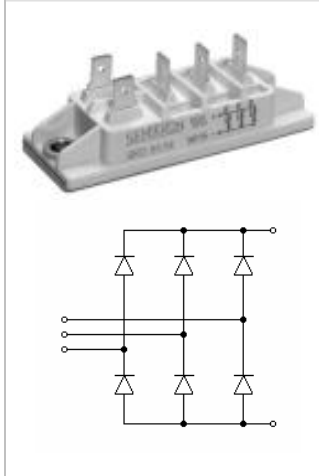

Figure 4 : The SKD 51 rectifier module

Figure 5 : SKM 50 GB 123 D, dual IGBT module

Figure 6 : 1st order equivalent electrical model of an electrolytic capacitor

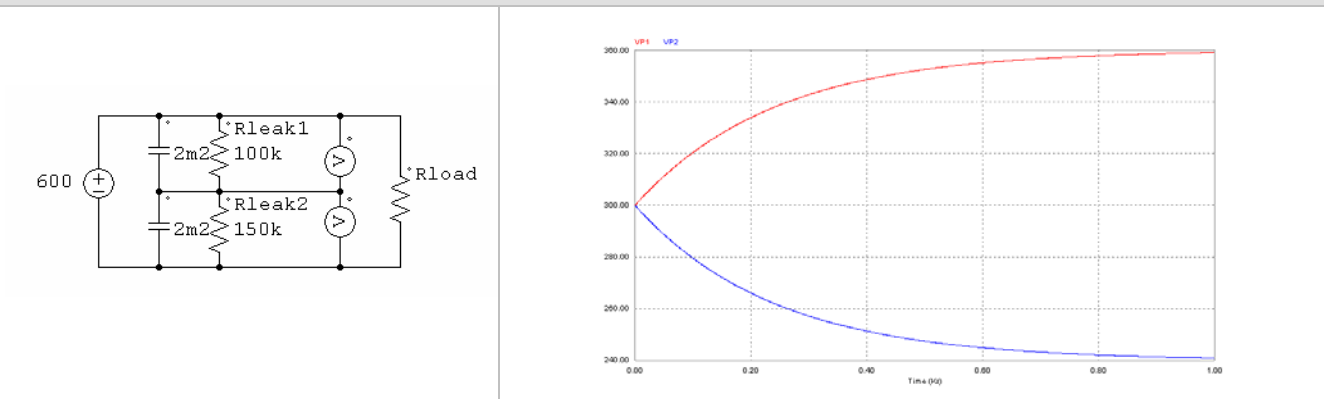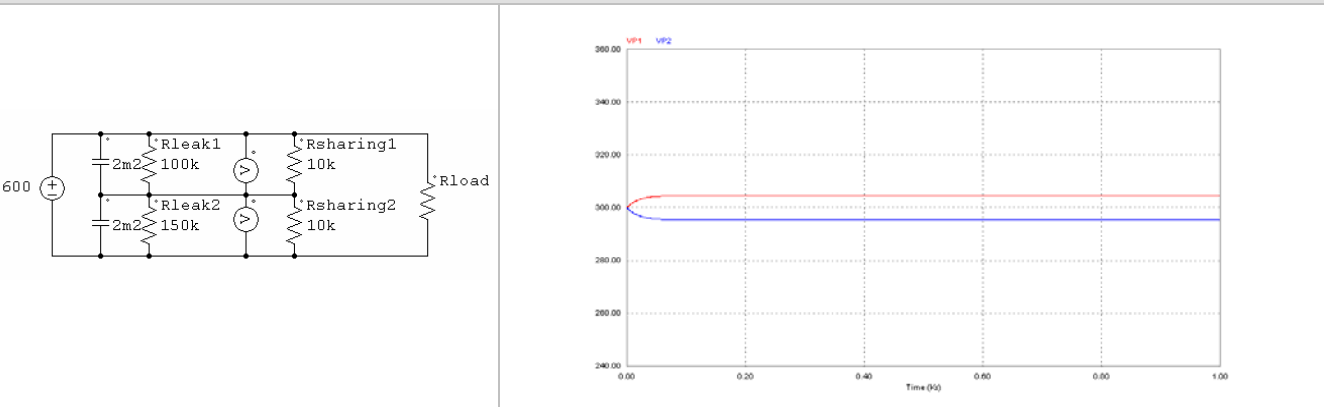**Figure7 : Voltage sharing without balancing resistors**

Figure 8 : With balancing resistors

Moreover, for safety purposes, these resistors discharge the capacitors when no energy is supplied to the capacitors from the network, or the load. However, it is highly recommended to have a discharging device, since the discharge time constant of the capacitor is 22 kΩ x 2200 µF = 46.2 s.

The switching cell

If high currents are switched fast then voltage overshoots occur which can destroy the switching power semiconductor if these overshoots exceed the maximum rated voltage (here 1200V).
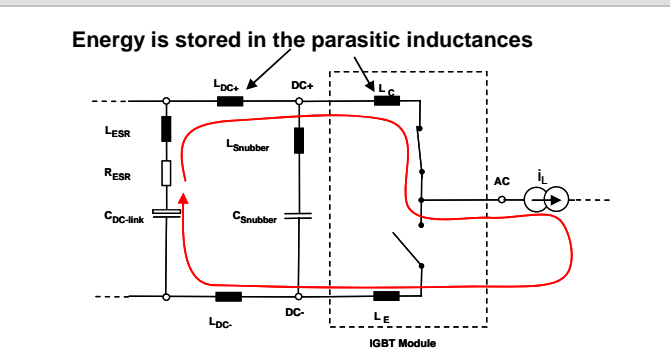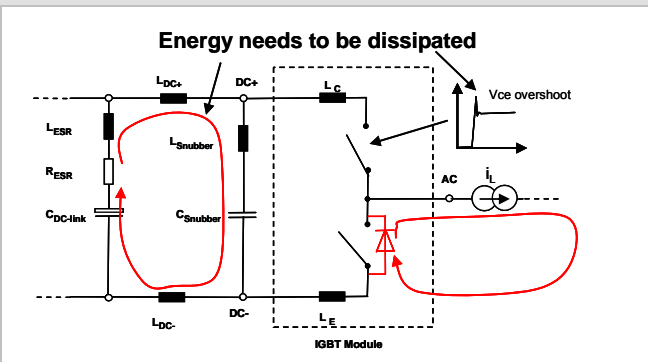
Figure 9 : Top IGBT ON

Energy is stored in the parasitic inductances

Figure 10 : Top IGBT turned OFF

Energy needs to be dissipated

This voltage overshoot is caused by the energy stored in the magnetic field of the current path (e.g. DC-link connections). It is linked by the value of the total parasitic inductance or stray inductance L_S (E=0,5*L_S*i²). L_S is the sum of all parasitic inductances. The voltage (V=L_S*di/dt) may exceed the maximum blocking voltage of the power semiconductor (V_{CES}, V_{RRM}…) because it is added to the DC link voltage. The first countermeasure is a good low inductive DC link design (the DC bus bar) to keep the voltage applied on the semiconductor low. This is done by means of a laminated bus bar system (sandwich of +DC, –DC metal sheets and an insulation layer between) and short connections between the voltage source (DC-link capacitor) and power semiconductor. In addition, snubber capacitors are recommended, which should be mounted directly on the DC-link terminals of each IGBT module. This snubber works as a low-pass filter and "suppresses" the voltage overshoot.

The snubber capacitors

They are placed as close to the IGBT module as possible to minimize the inductance between the switches and the capacitor. The waveform below shows a comparison of the voltage across an IGBT at turn-off, with and without snubber capacitor. The effect of voltage spike reduction can be clearly seen. The snubbers limit the over-voltages during commutations and as a consequence reduce the losses. They also protect the semiconductors against destructive overshoots during short-circuits cut-off.

Figure 11 : Typical waveform of VCE voltage on IGBT at switching off

Black line : Without snubber
Brown line : With snubber

$V_{CE} = 200V/dev$ $400ns/dev$
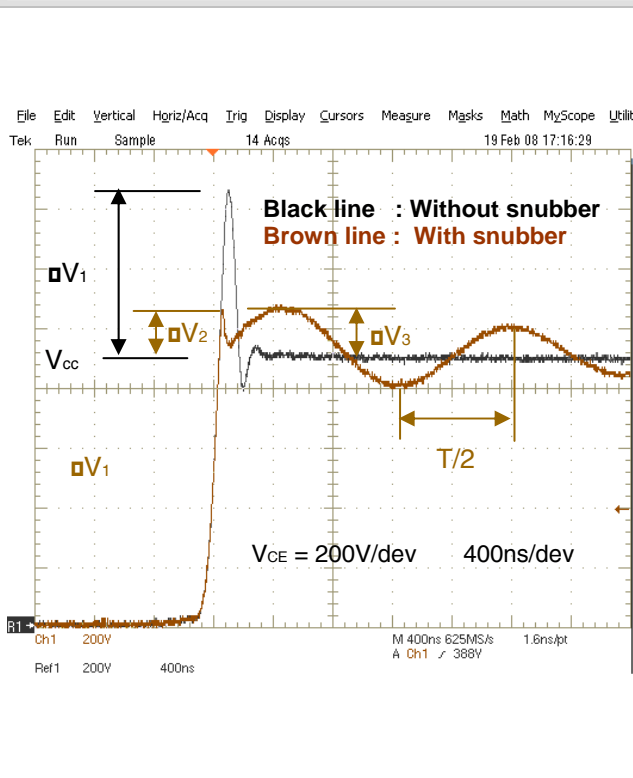
$$\Delta V_1 = \Sigma L \cdot di_c / dt$$

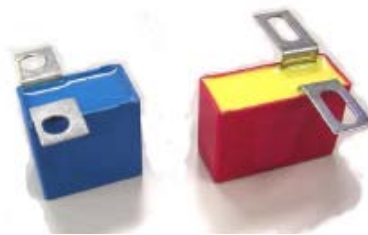$$\Delta V_2 = (L_C + L_E + L_{Snubber}) \cdot di_c / dt$$

$$\Delta V_3 \leq \sqrt{\frac{L_{DC-Link} \cdot i_c^2}{C_{Snubber}}}$$

$$f = \frac{1}{T} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{DC-Link} \cdot C_{Snubber}}}$$

$$\Sigma L = L_C + L_E + L_{DC+} + L_{DC-} + L_{ESR}$$

$$L_{DC-Link} = L_{DC+} + L_{DC-} + L_{ESR}$$

Figure 12 : Low inductance snubber capacitors for mounting on IGBT modules
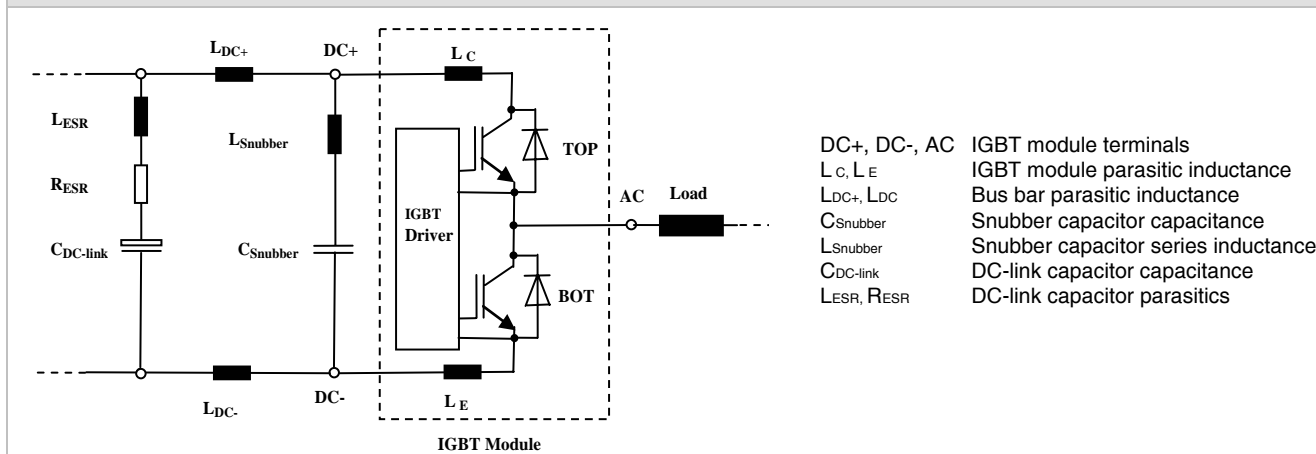

The bus bar

A low inductance laminated bus bar is used to connect the DC link capacitors to the inverter. The DC capacitors should be considered as a pure voltage source. Therefore the construction of the bus bar must have the minimum level of parasitic inductance. The laminated bus bar is made of 2 conductive metal plates (DC+ and DC-), with a large surface facing each other, separated by a thin isolating film, their inductance is much smaller than a wire connection.

In practice, the inductance of the bus bar can be derived from the overshoot of V_{CE} at switch-off.

Figure 13 : Equivalent circuit diagram of IGBT module connected to DC-link and snubber capacitor

|	
DC+, DC-, AC	IGBT module terminals
L_C, L_E	IGBT module parasitic inductance
L_{DC+}, L_{DC}	Bus bar parasitic inductance
$C_{Snubber}$	Snubber capacitor capacitance
$L_{Snubber}$	Snubber capacitor series inductance
$C_{DC-link}$	DC-link capacitor capacitance
L_{ESR}, R_{ESR}	DC-link capacitor parasitics

The thermal protection devices

The Normally-On thermal contact switch

Playing the role of a re-usable thermal fuse, this is an electrical contact, mechanically closed when its temperature is below the threshold temperature (71°C), and open when beyond. Practically, it is recommended to connect it in series with the driver power supply to stop the application in case of overheating. Its purpose is generally to detect the defect of the fan or abnormal long term current overload. After cooling down, it comes back to an ON position 20°C under its threshold value.
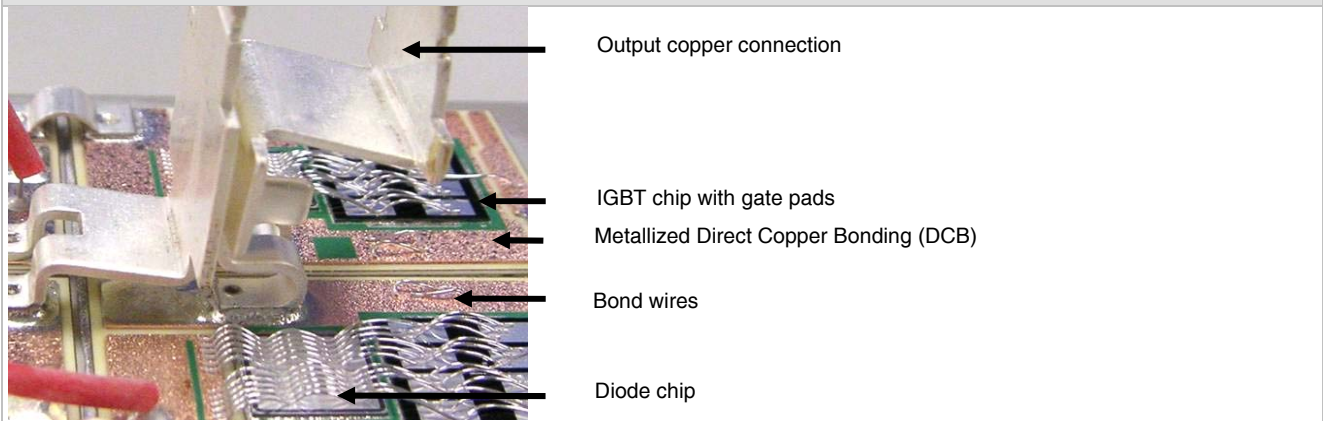
The temperature sensor

The LM335Z from National Semiconductor (see data-sheet link http://cache.national.com/ds/LM/LM335.pdf is an integrated circuit dedicated to precision temperature measurement. It is placed into the heat sink as close as possible to the heat source (the semiconductors). This measuring point serves as a reference point for heat sink temperature and it is referred to as Th. One possible application is to make an estimation of the power losses P, thanks to the formula $P = \Delta T \cdot Rth$, where ΔT is the temperature difference between the heat sink and the ambient air, and R_{th} is the thermal resistance of the heat sink P3/265F (96,2 K/kW). The voltage rise

Figure 14 : Temperature sensing principle and characteristic
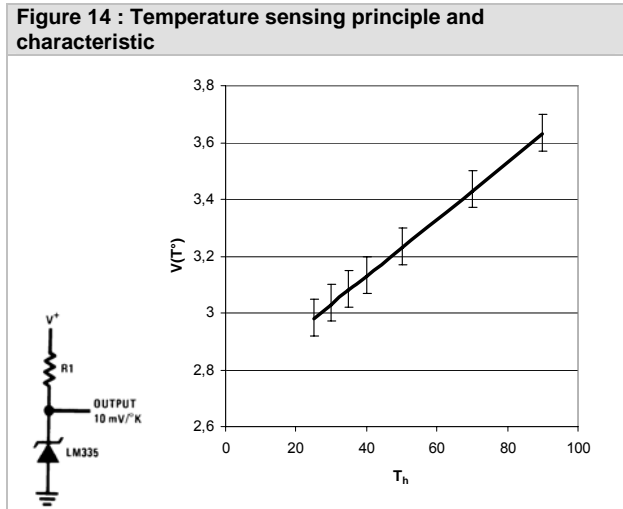
across the probe is proportional to the temperature, in the range of 10 mV/°C. The curve on **Figure** should be re-calibrated at 25°C for better accuracy. The test certificate gives the voltage value for a given temperature, so the temperature Th can be identified at any instant.

The IGBT (Insulated Gate Bipolar Transistor) module

Figure 15 : Internal construction of the power module

Output copper connection

IGBT chip with gate pads

Metallized Direct Copper Bonding (DCB)

Bond wires

Diode chip

As time passes, the IGBT is becoming the "all-purpose" component and prevails over all other technologies. In particular, its capabilities in voltage, current and frequency make it ideal for motor drive applications. The increase of its voltage range makes it suitable to replace the GTO in many traction applications, and the progress made in the reduction of the losses and improving the switching behaviour allows to replace the MOS – often used when high frequency is needed – e.g. in resonant inverters and Uninterruptible Power Supplies (UPS). They even tend to replace diodes and thyristors to realize controllable and low harmonics content rectifiers and motor-starters.

The reasons for its success come directly from its structure.

- It is relatively easy to drive. Similar to the MOSFET, the IGBT is controlled by a voltage, not a current, the drivers have become much simpler and cheaper compared with thyristors or BJTs for example.
- For a given voltage class (600 V for example) and a given current, the IGBT chip is smaller than the MOS's, as a consequence the internal gate capacitance is smaller, hence the driver power supply is cheaper. In addition, the saturation voltage (voltage drop between collector and emitter of the transistor) is lower than that of the MOS.
- The IGBT can be turned ON and OFF.
- Low firing current, average and instantaneous
- Good trade-off (High voltage, high current, high frequency)
- Short-circuit capability

Switching the IGBT

The IGBT is triggered by charging the gate, which is done by applying a voltage across the gate and the emitter (Figure). At first estimation, charging the IGBT can be approximated to charging an RC load, where R is roughly the gate resistor determined by the user and C is determined by the component structure. In power electronics, the IGBT transistor is used for switching, not for amplification, and especially for hard switching purposes. Therefore the IGBT works only in saturated mode. It is turned ON when the V_{GE} voltage becomes higher than a threshold value (typically 5.5 V for the SKM 50 GB 123D). These modules are optimized for a –15/+15 V control signal, which the SKHI 22 A (driver) is able to deliver, to ensure the best dynamic response from the IGBT.

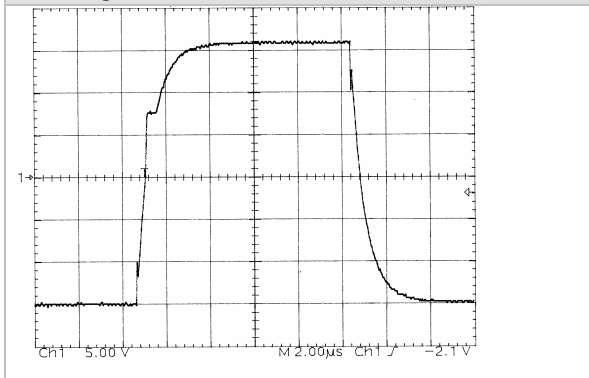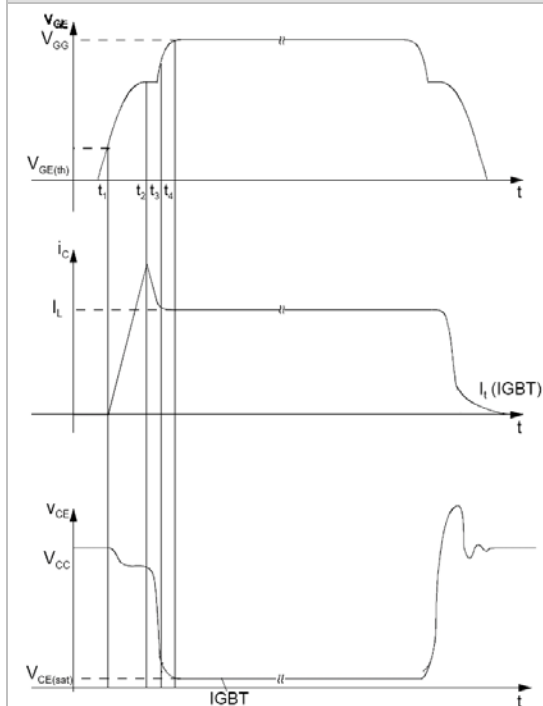**Figure 16 : gate charge and discharge Vge (t), switching ON and OFF**

Ch1 5.00 V   M 2.00µs Ch1 ↗ −2.1 V

Figure 19 : The gate charge characteristic

Turn-on: 0...t₁ (blocked transistor)
Gate current will be triggered by applying a control voltage. Up to the charge quantity Q_{G1} the current i_G solely charges the gate capacitance C_{GE}. The gate voltage V_{GE} rises. As V_{GE} is still below the threshold voltage $V_{GE(th)}$, no gate current will flow during this period.

Turn-on: t₁...t₂ (rise of gate current)
As soon as V_{GE} has reached $V_{GE(th)}$-level at t1, the transistor is turned on, first passing the active region. Gate current rises to I_L-level (ideal free-wheeling diode) or even exceeds I_L - as indicated in the switching pattern figure for a real free-wheeling diode. Similarly, V_{GE}, which is connected to the collector current in the active region by the transconductance g_{fc} with $I_D = g_{fc} * V_{GE}$, will increase up to the value $V_{GE1} = I_D/g_{fC}$ (time t₂). Since the free-wheeling diode can block the current only at t₂, V_{CE} will not drop considerably up to t₂. At t = t₂ charge Q_{G2} has flown into the gate.

Turn-on: switching interval t₂...t₃ (transistor during turn-on)
When the free-wheeling diode is turned off, V_{CE} will drop almost to on-state value $V_{CE(on)}$ by time t₃. Between t₂ and t₃ drain current and gate-source voltage are still coupled by transconductance; herefore, V_{GE} remains constant. While V_{CE} is decreasing, the Miller capacitance C_{GC} is recharged by the gate current i_G with the charge quantity (Q_{G3}-Q_{G2}). By t = t₃ charge Q_{G3} has flown into the gate.

Turn-on: t₃...t₄ (saturation region)
At t₃ the transistor is turned on, its curve has passed the pinch-off area to enter the ohmic area. V_{GE} and I_C are no longer coupled by gfs. The charge conducted to the gate (Q_{Gtot}-Q_{G3}) at this point affects a further increase of V_{GE} up to the gate control voltage V_{GG-}. Since the collector-emitter on-resistance $R_{CE(on)}$ depends on I_C and V_{GE}, the on-state voltage $V_{CE(on)} = I_C * R_{CE(on)}$ may be adjusted to the physical minimum by the total charge quantity Q_{Gtot} conducted to the gate. The higher the collector-emitter voltage V_{CE} (or commutation voltage), the bigger the charge Q_{Gtot} required to reach a certain gate-emitter voltage, see $V_{GE}(Q_G)$ curve.

Turn-off
During turn-off the described processes are running in reverse direction; the charge Q_{Gtot} has to be conducted out of the gate by the control current.
For approximations to determine the gate charge quantity required for turn-off, the gate charge characteristic in the $V_{GE}(Q_G)$ curve may be used.

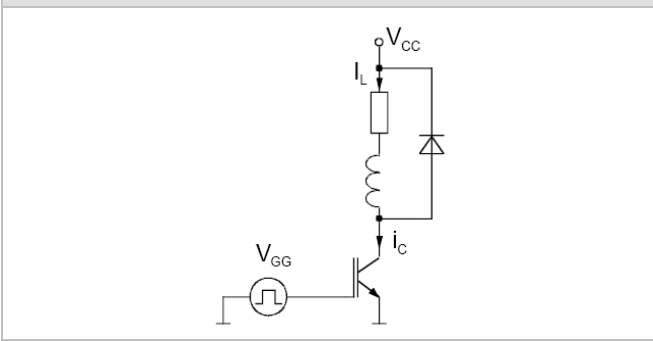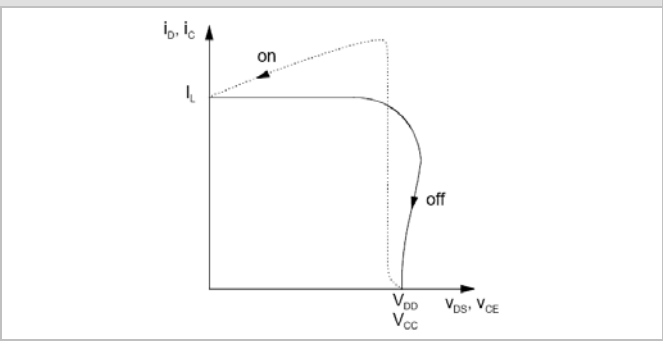| Figure 17 : Equivalent commutation cell	Figure 18 : Switching pattern of an IGBT (and a MOS)

Snubber or snubberless

As shown in Figure , the Safe Operating Area (SOA) of a switching IGBT is square, which means that there is no need to pull the voltage down to zero before reapplying the current or reverse voltage. This means that the IGBT can be switched at full current AND at full voltage. As far as switching characteristics of the IGBT alone are concerned, there is theoretically no need for a snubber, unless there is a drastic need for reducing the switching losses. However, as explained in 0, a snubber is required for dealing with short-circuit and the parasitic inductances of the complete switching loop. External elements force us to use a snubber, and the snubber will be designed according to the converter mechanical design. The capacitor snubber is only used for reducing the over voltages.

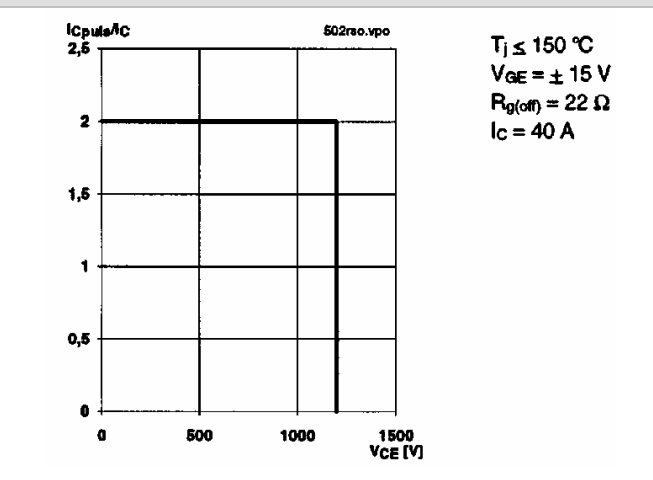### The IGBT in short-circuit

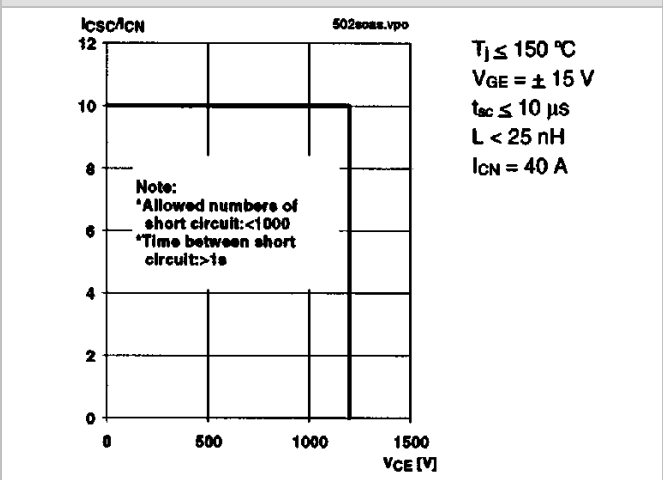| Figure 20 : Safe Operating Area of the IGBT	Figure 21 : Short-circuit SOA

Figure 21 shows the capability of the IGBT in short-circuit. The IGBT is able to withstand 10 times the rated current (10 x 50A for the SKM 50 GB 123 D) at full DC voltage. However, this short-circuit must be detected by the driver and last for less than 10 µs. Over this duration, there is a risk of thermal breakdown. The driver SKHI 22 A is aimed to detect it and to open the IGBT; the short-circuit is detected and cut-off within about 5 µs. As a comparison, the reaction of fuses would be hundreds of times slower. The current is self-limited due to the intrinsic structure of the IGBT to about 10 times the nominal current value. Once this current is reached, the IGBT starts to de-saturate, and the voltage across collector and emitter increases. The power absorbed by the IGBT can be calculated in such cases (some hundreds of Amps x some hundreds of Volts on a 30 mm² silicon chip). The very good short-circuit capabilities of the IGBT ensures good protection of the often very expensive connected equipment, in which the power converter price is small. The IGBT and its driver are very closely linked and the driver must be optimized.

The calculation of losses

The origin of losses

Losses are a heat power source generated by imperfections within the devices. We can identify different types of losses; dynamic and static, *switching and* *conduction losses* (Blocking losses are always neglected).
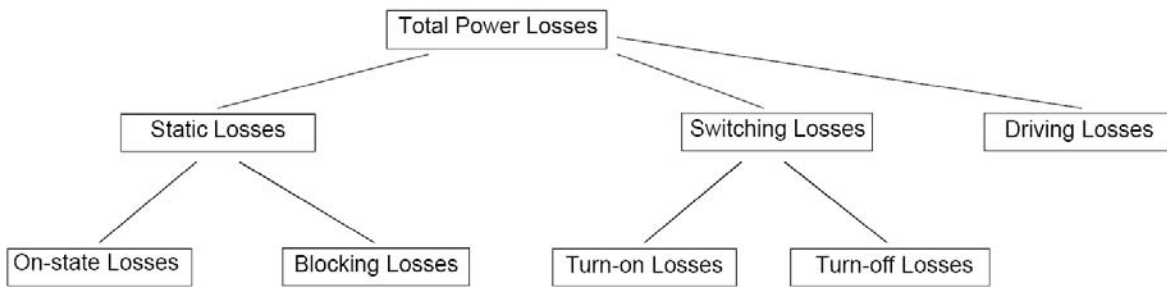
The losses can always be expressed as : $P = \dfrac{1}{T} \cdot \int_0^T V_{CE}(t) \cdot i(t) dt$,where T is the period of the signal.

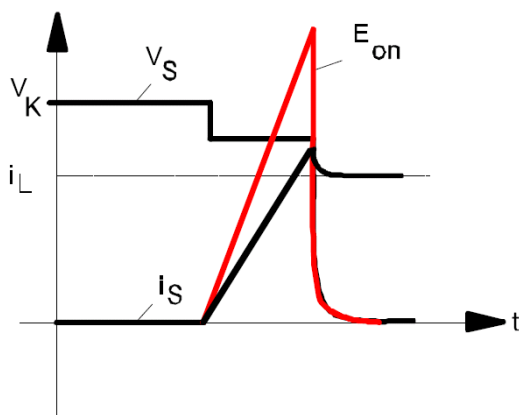**Figure 22 : Turn-On losses are the energy dissipated at each switching-on of the device**

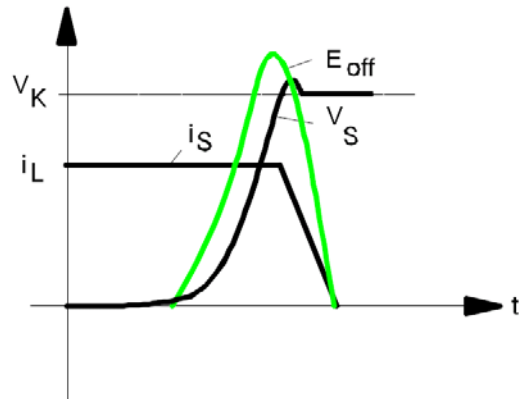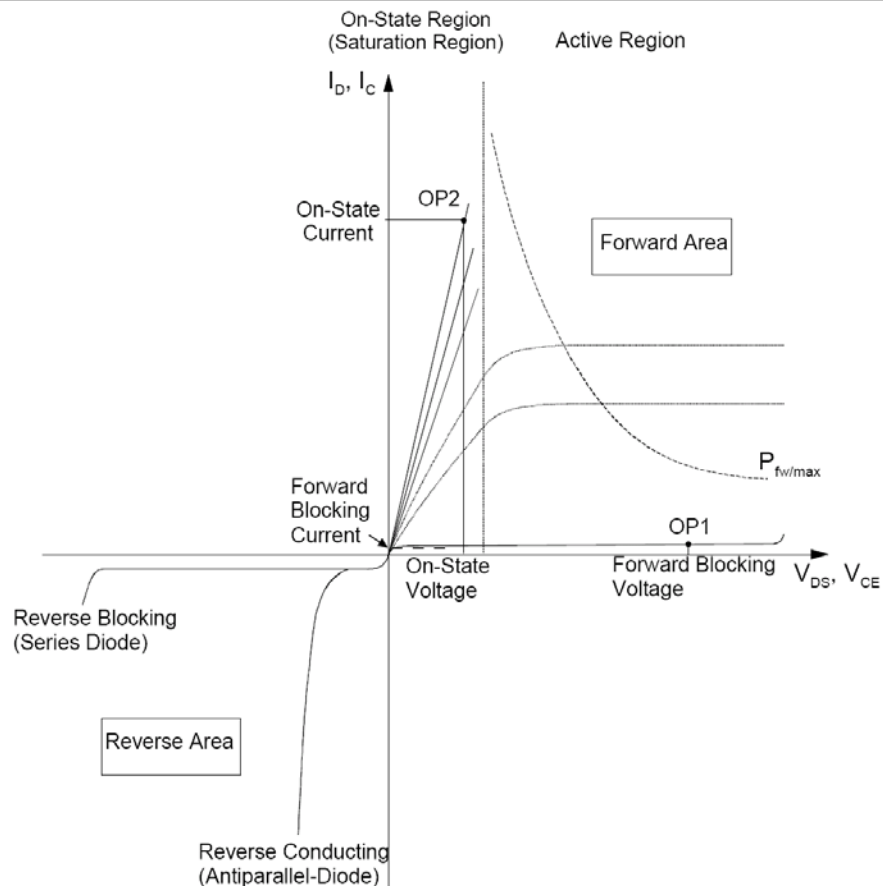**Figure 23 : Turn-Off losses are the energy dissipated at each switching-off of the device**

Figure 24 : Basic output characteristic of a power transistor module (diode + IGBT, blocked and conducting)

Why are power losses a problem

One of the main challenges for the power electronics designer is to deal with the thermal aspect. Due to semiconductor imperfections, a semiconductor can never be a pure switch (infinite resistance when OFF, zero when ON). When a device sees a voltage difference and a current circulates through it, power losses are generated which appear as heat, and must be removed as efficiently as possible. It is generally identified that the silicon temperature, called *junction temperature*, Tj, shall never reach or surpass the maximum allowed T$_{jmax}$. Beyond this T$_{jmax}$, there is a great risk of failure in the bond wire connections, also the electrical characteristics of the component can change (e.g. rise of the leakage

current in the open IGBT): there is also a risk of destruction. This T$_{jmax}$ is typically 150°C. Taking into account the disparity of components (although the process has become more and more reliable and some devices can reach today higher temperatures), one should respect a safety margin. On the other hand, taking too much safety margin is detrimental to the economic margin since it would mean more silicon, therefore higher cost. For the IGBTs, it is safe and economically viable to respect a 125°C maximum junction temperature. In addition to that, losses reduce the overall efficiency. It is usual to reach 95% to 98% efficiency with IGBT converters.

The conduction losses

They are the result of the product of current and voltage (collector-emitter) during the conduction period. The component static characteristics can be extrapolated from the curve. In our case, V$_{GE}$=+15 V, and the curves can be approximated by 2 half-lines (dot-lines). The half-line $V_{CE} = V_{CE0} + R_{ce} \cdot I_C$ is equivalent to considering the power dissipation of a voltage source and a series resistance.
The expression for forward power losses become:

$$P = \frac{1}{T} \int_0^{T1} V_{CE0} \cdot i(t) + R_{ce} \cdot i^2(t) dt$$

$$= \frac{1}{T} \left[V_{CE0} \int_0^T i(t) dt + R_{ce} \int_0^T {}^2 i(t) dt \right]$$

$$= V_{CE0} \cdot I_{av} + R_{ce} \cdot I_{rms}{}^2$$

V$_{ce0}$ and R$_{ce}$ can be determined graphically from the curves, and the currents depend on the application.

Figure 45 : Static characteristics

Application example: Buck Chopper with DC output current

If the output inductor of a step-down converter is large enough, it can be considered that the output current is almost DC. Neglecting the ripple current (i$_{LH}$-i$_{LL}$), one can affirm i(t)=i$_{Lavg}$. Therefore only V$_{CE}$(t) is variable.

$$P_{cond} = \frac{1}{T} \cdot \int_0^T V_{CE}(t) \cdot i(t) dt$$

$$I_{Tavg} = \alpha \cdot i_{Lavg}$$

$$I_{Trms} = \sqrt{\alpha} \cdot i_{Lavg}$$

Where $\alpha = \frac{t_1}{T}$

According to these results, we can conclude :

$$P_{Cond(igbt)} = R_{CE} \cdot \left(\sqrt{\alpha} \cdot i_{Lavg} \right)^2 + V_{CE0} \cdot \alpha \cdot i_{Lavg}$$
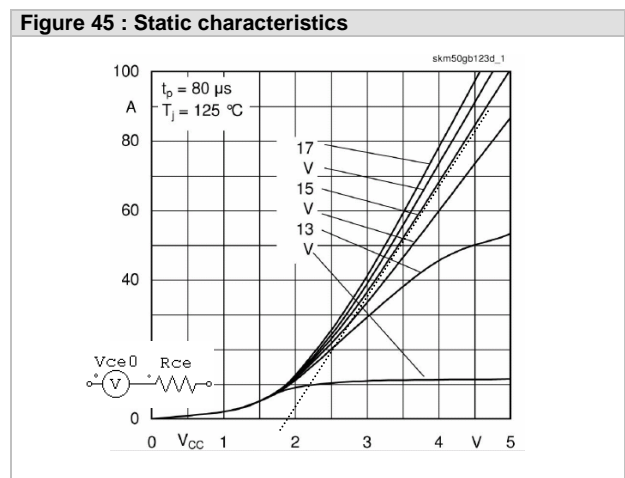

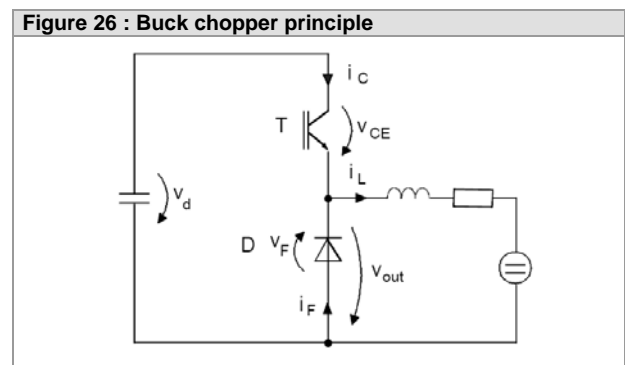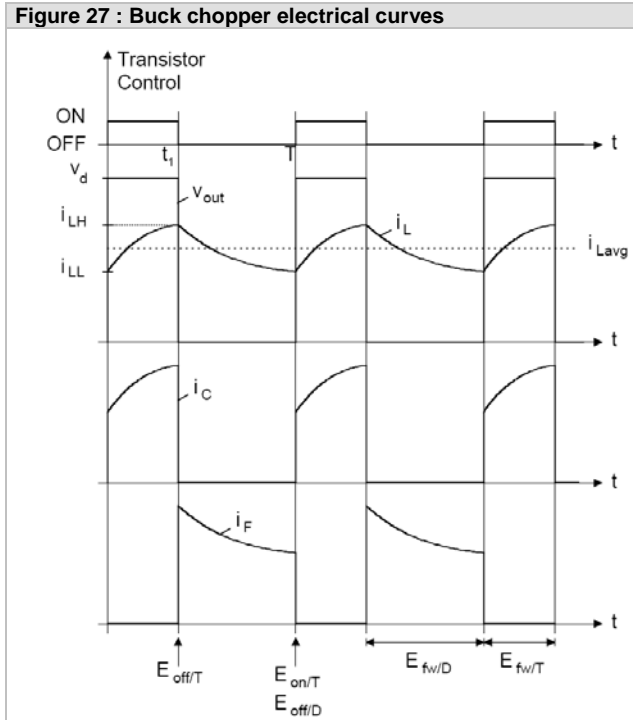Figure 26 : Buck chopper principle

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Figure 27 : Buck chopper electrical curves

Application example: 3 phase PWM inverter

Let's call *m* the degree of modulation, which can be understood as the voltage utilization of the converter.

$$m = 2 \cdot \frac{\sqrt{3}}{3} \cdot \frac{U_{peak}}{U_d}$$

In case of a pure sinusoidal reference voltage, the degree of linear modulation will be $0 \leq m \leq 1$

Under the following assumptions,
- transistor and diode switching times are neglected;
- Thermally constant junction temperatures (valid for f = 50 Hz);
- Linear modulation of the converter;
- Switching frequency ripple of the AC current is negligible;
- Forward characteristics of semiconductors are linear $V_{CE}=V_{CE0}+rI$,

one can prove that for a 3 phase inverter the conduction losses are expressed by

$$P_{cond}(IGBT) = \frac{1}{2}\left(V_{ce0} \cdot \frac{I}{\pi} + r \cdot \frac{I^2}{4}\right) + m \cdot \cos\varphi \cdot \left(V_{ce0} \cdot \frac{I}{8} + \frac{rI^2}{3\pi}\right)$$

And

$$P_{cond}(Diode) = \frac{1}{2}\left(V_{d0} \cdot \frac{I}{\pi} + r \cdot \frac{I^2}{4}\right) - m \cdot \cos\varphi \cdot \left(V_{d0} \cdot \frac{I}{8} + \frac{rI^2}{3\pi}\right)$$

The switching losses

During the commutations, losses appear due to the switching pattern, as explained on Figure . Please note the overvoltage when turning the IGBT OFF, which must be kept under the maximum value of the component class (1200 V). Measurements performed in the SEMIKRON laboratory to evaluate these losses resulted in the curves of Figure , showing the energy dissipated during the commutations ON and OFF in the semiconductor (IGBT in this case). This figure shows the energy involved when switching ON (E_{ON}) and OFF (E_{OFF}), at a given voltage (600 V), and gate resistor (22 Ohms), as a function of the current. In our case, the measures of current dependence show that the switching energy can be approximated as a linear (even proportional) function of the current, which means for a first approach that these energies are proportional to the current. The expression of the switching energies can be expressed :

Figure 28 : Eon, Eoff versus current

$$(Eon + Eoff)_{(U,Rg)}(I) = k \cdot I$$

Using the same principle, it has been measured and we can approximate that, for this chip technology:

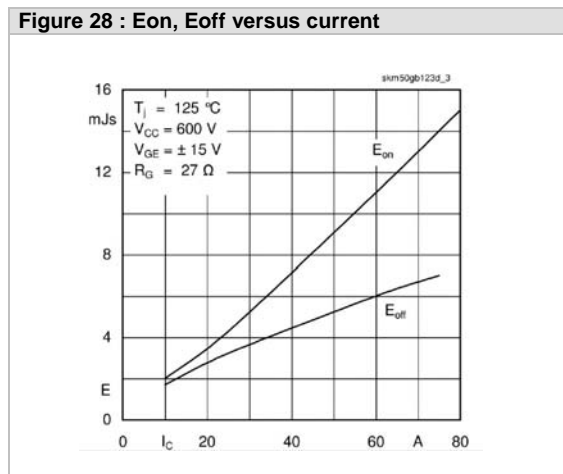$$(Eon + Eoff)_{(I,Rg)}(U) = k' \cdot U$$

Therefore for a constant current,

$$P = f_{sw} \cdot (Eon + Eoff)$$
$$= f_{sw} \cdot I \cdot U \cdot K$$

where the reference K is given by $K = \dfrac{(Eon+Eoff)(50A,600V)}{50A \cdot 600V}$ for our semiconductors

Application example: Buck Chopper with DC output current

As expressed earlier, if we consider I_{Lavg} as constant,

$$P = f_{sw} \cdot (Eon + Eoff)$$
$$= f_{sw} \cdot I_{Lavg} \cdot U \cdot K$$

Application example: 3 phase PWM inverer

Based on the same principle, only the current varies in the previous expressions, replaced by the averaged commutated

value : $P_{ON+OFF(IGBT)} = \dfrac{\sqrt{2} \cdot I_{rms}}{\pi} \cdot f_{sw} \cdot U \cdot K$

From losses calculation to temperature estimation

The losses must be dissipated to keep the component at a safe temperature. This is why a cooling device, or *heat sink,* is used. When a material is submitted to a heat transfer, we can define the *thermal resistance* between 2 points of this material as the ratio of the temperature rise between these 2 points and the heat power. This property can be seen as the equivalent of electrical resistance to the current. In thermal/electrical equivalence,

- Temperature (K) ⇔ voltage (V)
- Power losses (W) ⇔ current (A)
- Thermal resistance (K/W) ⇔ resistance (Ω)

As for the electrical voltages, we will evaluate the temperature drops

- ambient to heat sink, ΔT_{ha}
- heat sink to case, ΔT_{ch}
- case to junction. ΔT_{jc}

All the internal construction materials have a thermal resistance, and all interfaces between them add another thermal resistance. In order for it to be as small as possible, and therefore to improve the heat transfer from the chip to the heat sink and to the ambient, the following principles are used:

- From the thermal perspective, all material interfaces should be as thin as possible as the thermal resistance is proportional to the thickness of the material. The new SkiiP and MiniSKiiP products from SEMIKRON have addressed this problem by removing the 3 mm copper base plate and pressing the ceramic directly onto the heat sink.
- Thermal grease reduces the contact thermal resistance between the module and the heat sink, by filling the irregularities between both surfaces.
- The heat sink must be optimized: a large exchange surface with the ambient will improve the exchange coefficient with air. A bigger mass will have a greater capacitance for storing the heat, reducing the temperature ripples, but will have a higher gradient of temperature.

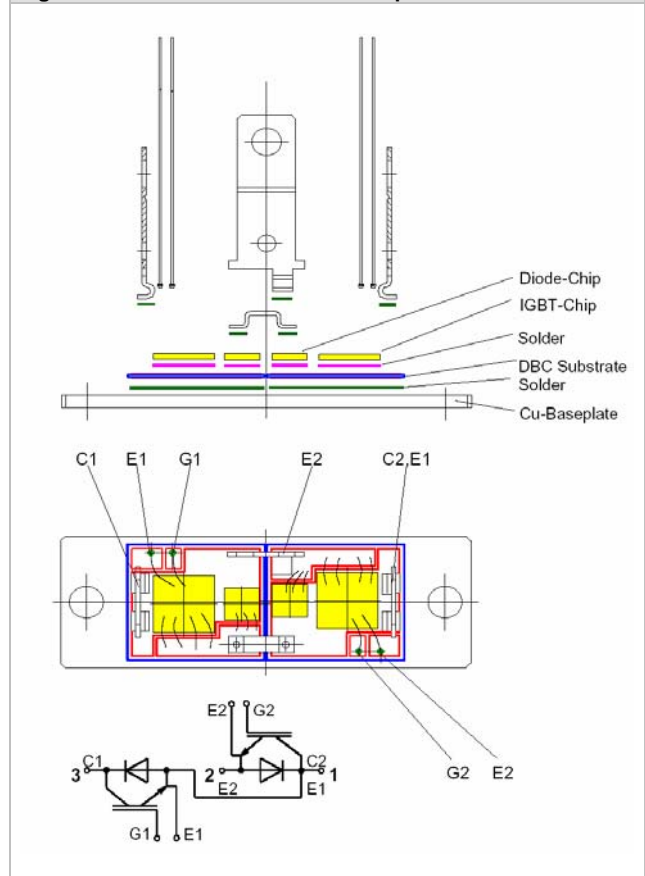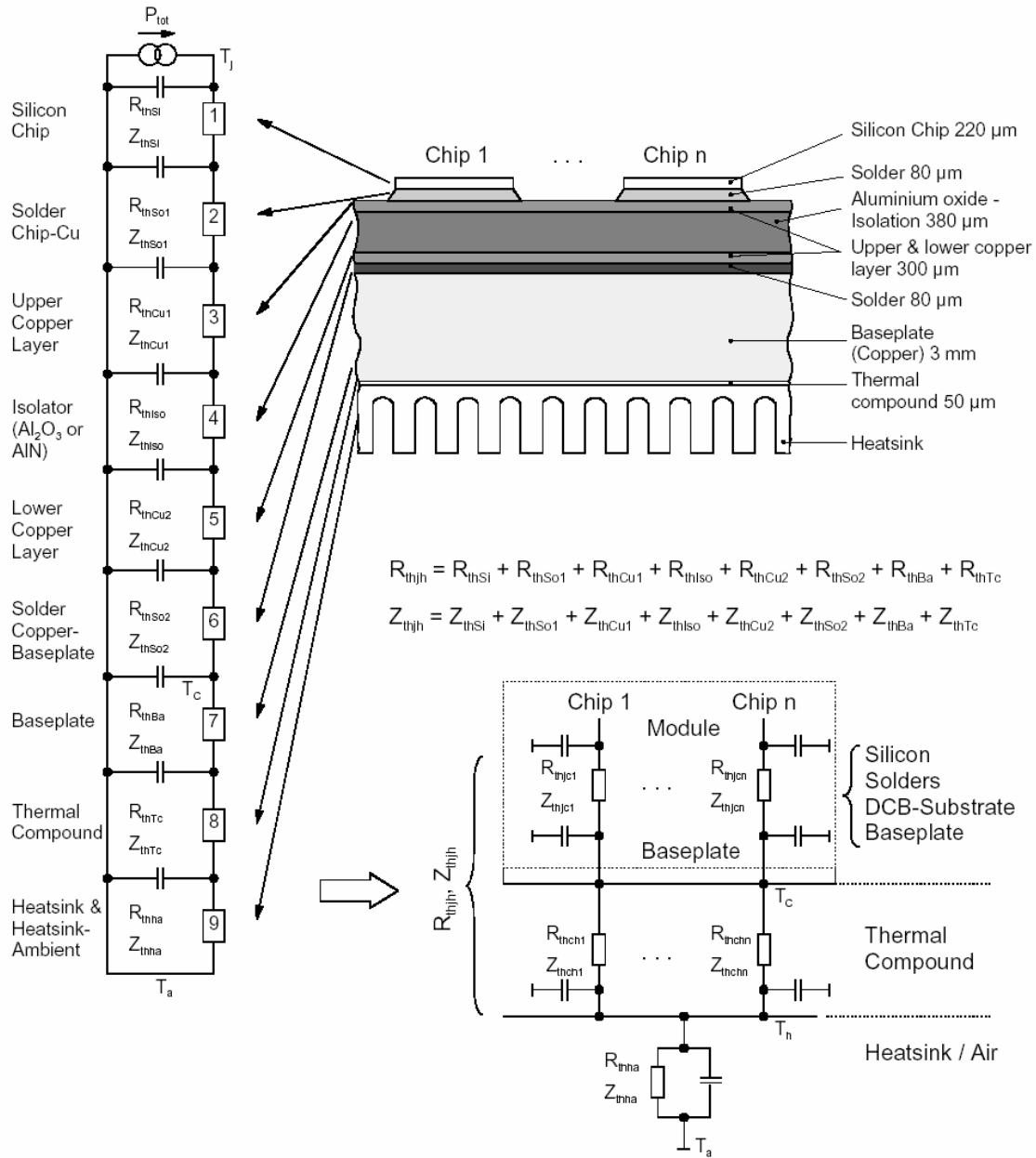Figure 29 : internal construction of a power module

Figure 30 : Complete thermal cascade model

Modelling – thermal-electrical equivalence

Figure 31 : thermal impedance

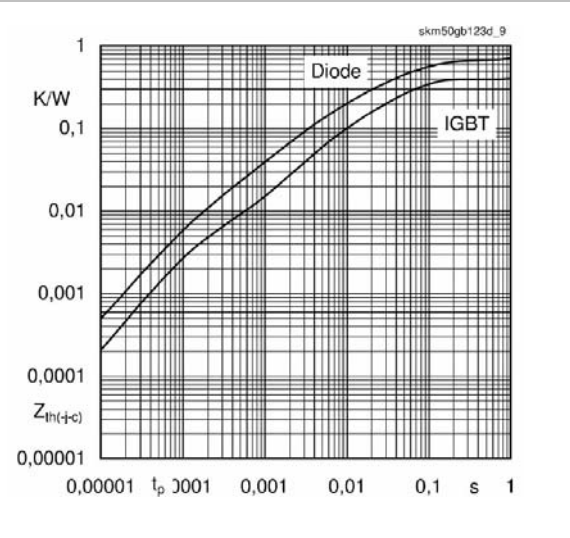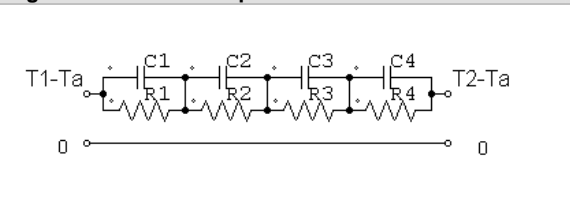Figure 31 : thermal impedance

Figure 32 : electrical equivalent model

The component on its heat sink can be modelled as a succession of thermal resistances, as indicated before:

- Junction-case thermal resistance ($R_{th\ jc}$)
- case-heat sink thermal resistance ($R_{th\ ch}$)
- heat sink-ambient thermal resistance ($R_{th\ ha}$)

However, this model is only an approximation for steady state. Because of the material property, from **Figure 31**, it can be noted that the thermal impedance is time-dependant. We can model each transient thermal impedance curve as a RC network cascade, such as the one displayed Figure 31 : thermal impedance. Thanks to the values given in the data-book, it is possible to determine with good accuracy all temperatures, even for very short transients. For times greater than 0.5 s, it's not relevant any more to consider the impedances of the semiconductors, only resistances. This approach is fundamental for the heat sink, as the time constants are much longer for this big mass of aluminium. Here are the values for the heat sink of the Power Electronics Teaching System:

τ_i (s)	0.5	70	180	2000
$R_{ha\text{-}i}$ (K/W)	$3.44 \cdot 10^{-3}$	$1.6 \cdot 10^{-2}$	$7.08 \cdot 10^{-2}$	$5.95 \cdot 10^{-3}$

At any time, the thermal impedance can be approached with the formula

$$Z_{th-ha}(t) = \sum_i R_{ha-i}\left(1 - e^{-\frac{t}{\tau_i}}\right)$$

References

(1) SEMIKRON DATA BOOK : www.semikron.com
(2) Application Manual, Power Modules, First Edition, U. Nicolaï, T. Reimann, J. Petzoldt, J. Lutz, Ed P. Martin, SEMIKRON International, 2000. ISBN 3-932633-46-6. Available from the Internet www.semikron.com under the application link.
(3) Application Note, First Edition 1998, Power Electronics Teaching System, SEMIKRON
(4) Application Note, AN 7006, 2008, J. Lamp, SEMIKRON

Important Note:

Annex : SKHI 22 AR data-sheet

SKHI 22 A / B H4 (R) ...

SEMIDRIVER™

Hybrid Dual IGBT Driver

SKHI 22 A / B H4 (R)

Preliminary Data

Features

- Double driver for halfbridge IGBT modules
- SKHI 22A H4 is compatible to old SKHI 22 H4
- SKHI 22B H4 has additional functionality
- CMOS compatible inputs
- Short circuit protection by V_{CE} monitoring and switch off
- Drive interlock top / bottom
- Isolation by transformers
- Supply under voltage protection (13V)
- Error latch / output

Typical Applications

- Driver for IGBT modules in bridge circuits in industrial applications
- DC bus voltage up to 1200 V

1) see fig. 6
2) At R_{CE} = 36 kΩ, C_{CE} = 470 pF, R_{VCE} = 1 kΩ

Absolute Maximum Ratings

Symbol	Conditions	Values	Units
V_S	Supply voltage prim.	18	V
V_{iH}	Input signal volt. (High) SKHI 22A H4	V_S + 0,3	V
	SKHI 22B H4	5 + 0,3	V
$Iout_{PEAK}$	Output peak current	8	A
$Iout_{AVmax}$	Output average current	40	mA
f_{max}	max. switching frequency	50	kHz
V_{CE}	Collector emitter voltage sense across the IGBT	1700	V
dv/dt	Rate of rise and fall of voltage secondary to primary side	50	kV/µs
V_{isolIO}	Isolation test voltage input - output (2 sec. AC)	4000	Vac
V_{isol12}	Isolation test voltage output 1 - output 2 (2 sec. AC)	1500	V
R_{Gonmin}	Minimum rating for R_{Gon}	3	Ω
$R_{Goffmin}$	Minimum rating for R_{Goff}	3	Ω
$Q_{out/pulse}$	Max. rating for output charge per pulse	4[1]	µC
T_{op}	Operating temperature	- 40 ... + 85	°C
T_{stg}	Storage temperature	- 40 ... + 85	°C

Characteristics — T_a = 25 °C, unless otherwise specified

Symbol	Conditions	min.	typ.	max.	Units
V_S	Supply voltage primary side	14,4	15	15,6	V
I_{SO}	Supply current primary side (no load)		80		mA
	Supply current primary side (max.)			290	mA
V_i	Input signal voltage SKHI 22A H4 on/off		15 / 0		V
	SKHI 22B H4 on/off		5 / 0		V
V_{iT+}	Input threshold volt. (High) SKHI 22A H4	10,9	11,7	12,5	V
	SKHI 22B H4	3,5	3,7	3,9	V
V_{iT-}	Input threshold volt. (Low) SKHI 22A H4	4,7	5,5	6,5	V
	SKHI 22B H4	1,5	1,75	2,0	V
R_{in}	Input resistance SKHI 22A H4		10		kΩ
	SKHI 22B H4		3,3		kΩ
$V_{G(on)}$	Turn on gate voltage output		+ 15		V
$V_{G(off)}$	Turn off gate voltage output		- 7		V
R_{GE}	Internal gate-emitter resistance		22		kΩ
f_{ASIC}	Asic system switching frequency		8		MHz
$t_{d(on)IO}$	Input-output turn-on propagation time	0,85	1	1,15	µs
$t_{d(off)IO}$	Input-output turn-off propagation time	0,85	1	1,15	µs
$t_{d(err)}$	Error input-output propagation time		0,6		µs
$t_{pERRRESET}$	Error reset time		9		µs
t_{TD}	Top-Bot Interl. Dead Time SKHI 22A H4	3,3		4,3	µs
	SKHI 22B H4	no interlock		4,3	µs
V_{CEsat}	Reference voltage for V_{CE}-monitoring		5[2]	10	V
C_{ps}	Coupling capacitance primary secondary		12		pF
MTBF	Mean Time Between Failure T_a = 40°C		2,0		10^6 h
w	weight		45		g

This technical information specifies semiconductor devices but promises no characteristics. No warranty or guarantee expressed or implied is made regarding delivery, performance or suitability.