

### 3.7 Modèle 8255 - Référence 33xx

Révision : 1 du 8 mai 1995

Révision : 2 du mai 2001

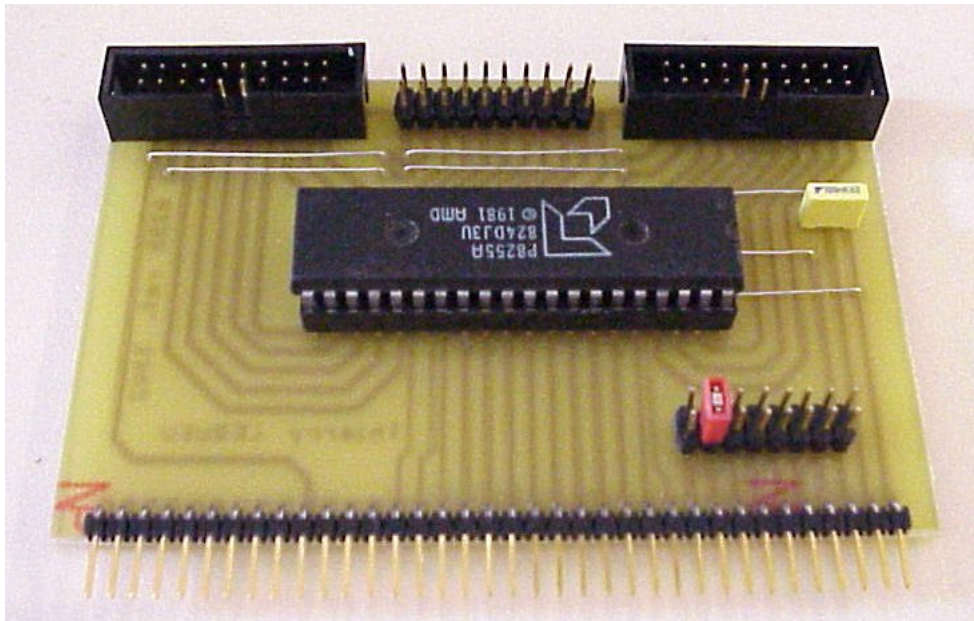


Figure 3.11. Photos de la carte (images-maquettes\pio8255-33-1.jpg).

### 3.8 Liste des documents

- Prix du montage.
- Schéma électronique.
- Circuit imprimé.
- Implantation des composants.

Tableau 3.3. Liste des composants 8255 - Ref 33xx.

Réf.	Désignation	Qu.	Fournisseur	Date	Code Cde	Page	Prix U.H.T.	Prix T.H.T.
C1	100 nF 63 V MKT	1					1.20 F	1.20 F
U1	8255	1					25.00 F	25.00 F
JP1	Barrette coudée dorée x points	1					17.80 F	17.80 F
JP3	Barrette droite dorée x points	1					4.00 F	4.00 F
JP3,JP4,JP5	Barrette droite dorée x points	3					5.00 F	15.00 F
Divers	Support double-lyre 40 broches	1					5.60 F	5.60 F
Divers	Cavalier	1					1.20 F	1.20 F
Divers	Circuit imprimé S.F. x mm ref	55					0.15 F	8.25 F

TOTAL H.T. :	78.05 F
dont T.V.A. 19.60%	15.30 F
TOTAL T.T.C. :	93.35 F

### 3.9 Câblage des connecteurs HE11 de sortie

E=+15V	1	2	GND
E=+5V	3	4	GND
PB7	5	6	GND
PB6	7	8	GND
PB5	9	10	GND
PB4	11	12	GND
PB3	13	14	GND
PB2	15	16	GND
PB1	17	18	GND
PB0	19	20	GND

Figure 3.12. Connecteur JP3 - port B.

E=+15V	1	2	GND
E=+5V	3	4	GND
PC3	5	6	GND
PC2	7	8	GND
PC1	9	10	GND
PC0	11	12	GND
PC4	13	14	GND
PC5	15	16	GND
PC6	17	18	GND
PC7	19	20	GND

Figure 3.13. Connecteur JP5 - port C.

E=+15V	1	2	GND
E=+5V	3	4	GND
PA0	5	6	GND
PA1	7	8	GND
PA2	9	10	GND
PA3	11	12	GND
PA4	13	14	GND
PA5	15	16	GND
PA6	17	18	GND
PA7	19	20	GND

Figure 3.14. Connecteur JP4 - port A.

# Projet 3 - PIO8255 / Extension PIO 8255, réf. 3Yxx.

Projet : ES\_PC

Info : [DATA103]

## 3.1 Documentation du 82C55A

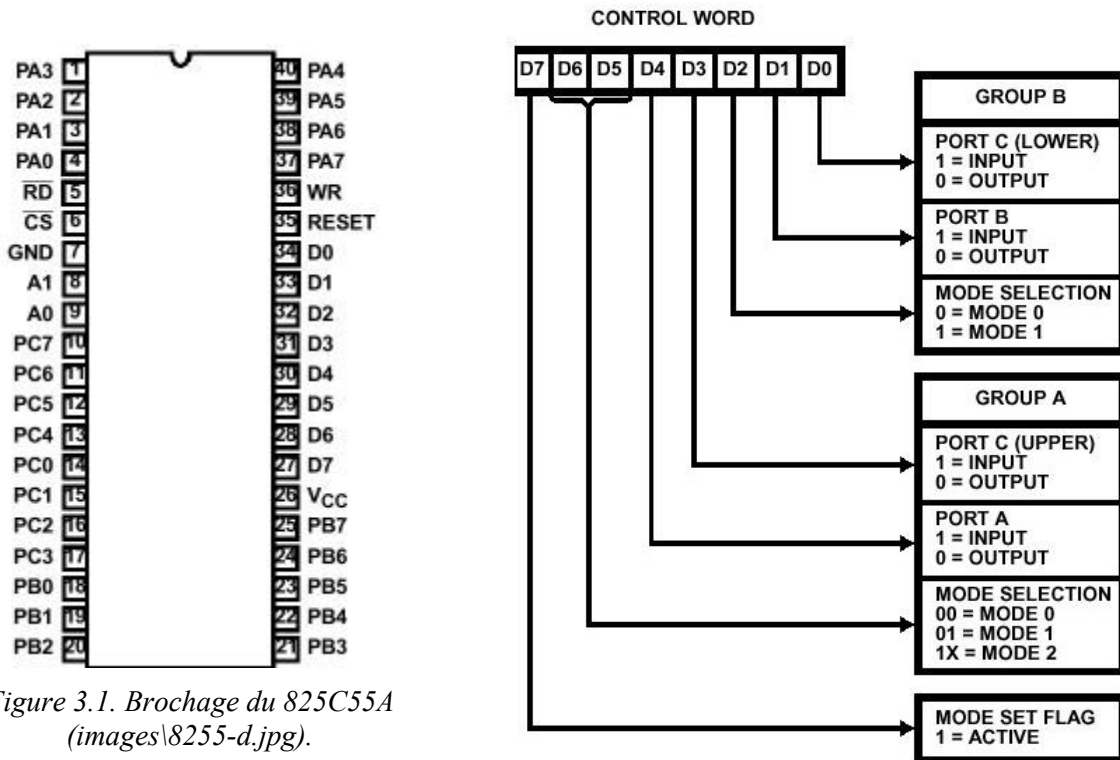


Figure 3.1. Brochage du 8255A (images\8255-d.jpg).

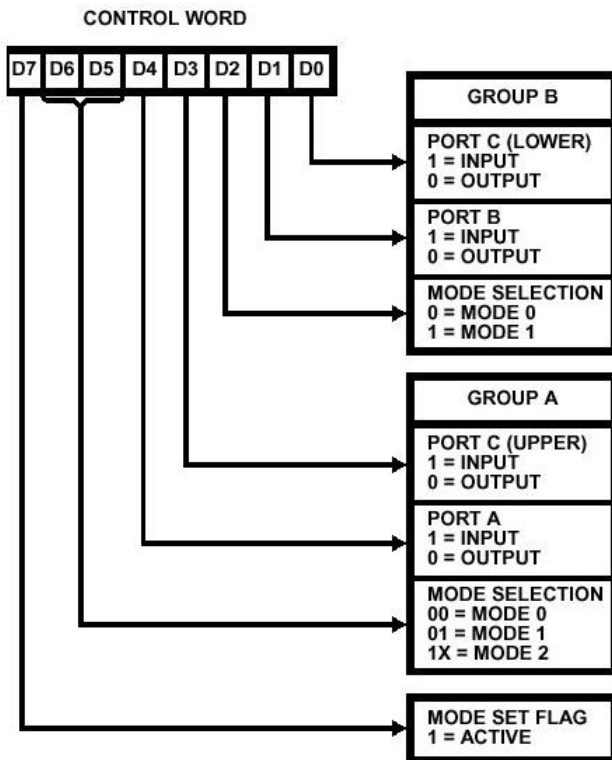


Figure 3.2. Mot de contrôle du 8255A (images\8255-c.jpg).

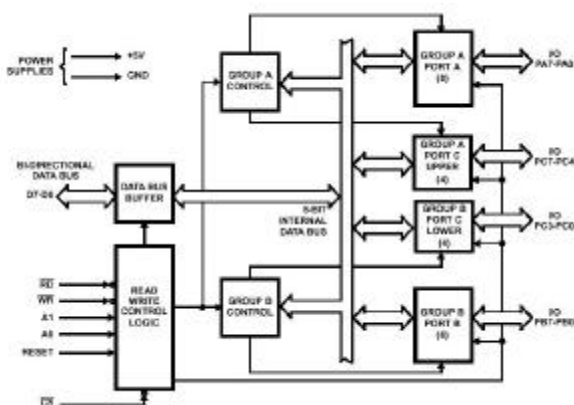
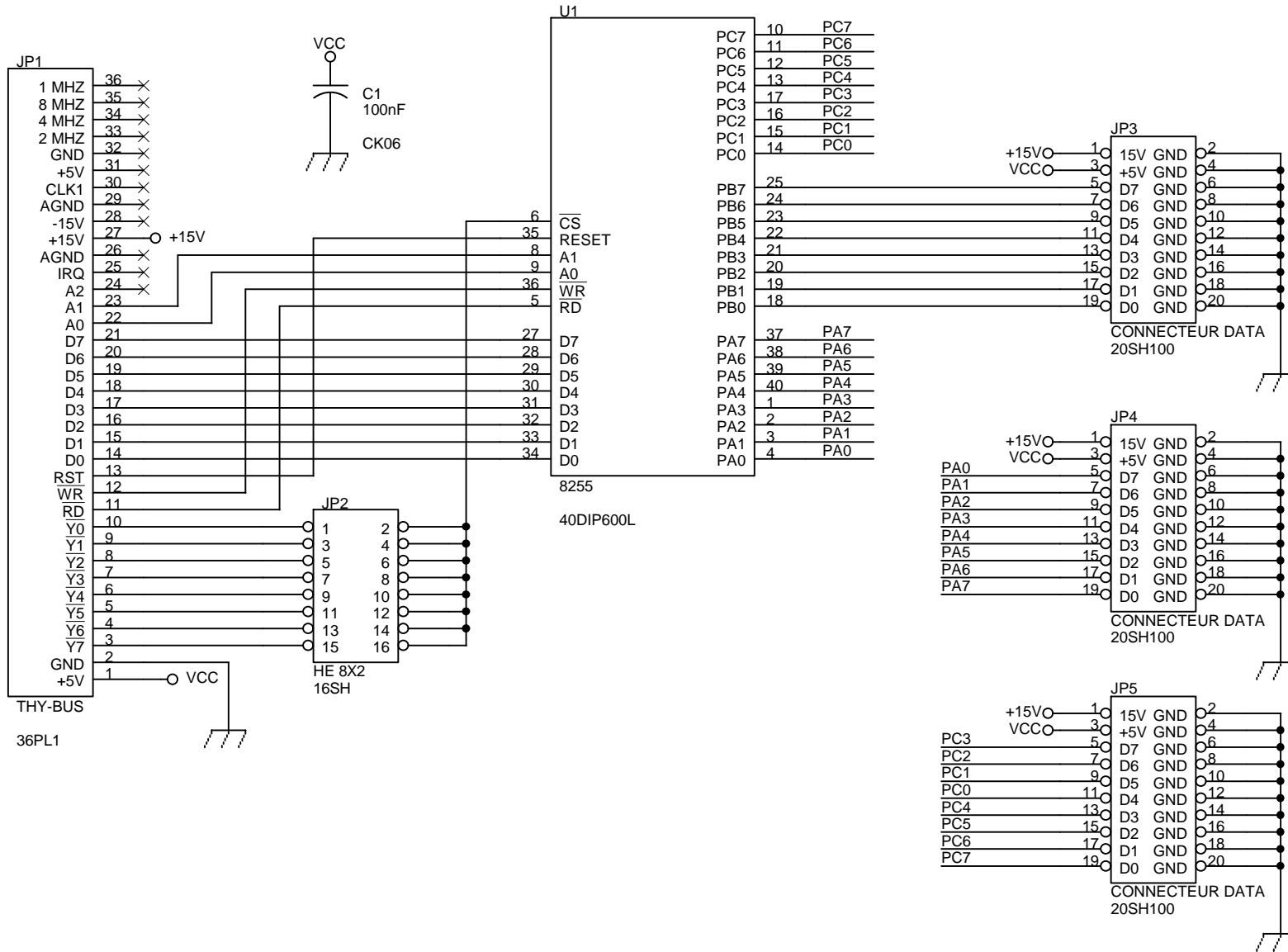


Figure 3.3. Organisation interne du 8255A (images\8255-a.jpg).

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V <sub>CC</sub>	26		V <sub>CC</sub> : The +5V power supply pin. A 0.1µF capacitor between pins 26 and 7 is recommended for decoupling.
GND	7		GROUND
DATA BUS	27-34	IO	DATA BUS: The Data Bus lines are bidirectional tri-state pins connected to the system data bus.
RESET	35	I	RESET: A high on this input sets the control register and all ports (A, B, C) are set to the input mode with the "Bus Hold" output latched as
CS	6	I	CHIP SELECT: Chip select or an active low input used to enable the 82C55A onto the Data Bus for CPU communications.
RD	5	I	READ: Read is an active low input control signal used by the CPU to read status information or data via the data bus.
WR	36	I	WRITE: Write is an active low input control signal used by the CPU to load control words and data into the 82C55A.
AO/A1	8, 9	I	ADDRESS: These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control-word register. AO and A1 are normally connected to the least significant bits of the Address Bus A0, A1.
PA0-PA7	1-4, 37-40	IO	PORT A: 8-bit input and output port. Both bus hold tri-state and bus hold low output are present on this port.
PB0-PB7	18-25	IO	PORT B: 8-bit input and output port. Bus hold high output is present on this port.
PC0-PC7	10-17	IO	PORT C: 8-bit input and output port. Bus hold output is present on this port.

Figure 3.4. Définition des broches du 8255A (images\8255-b.jpg).



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