3.5 Modèle 8255 - Référence 32xx

Révision : 1 du 5 avril 1994

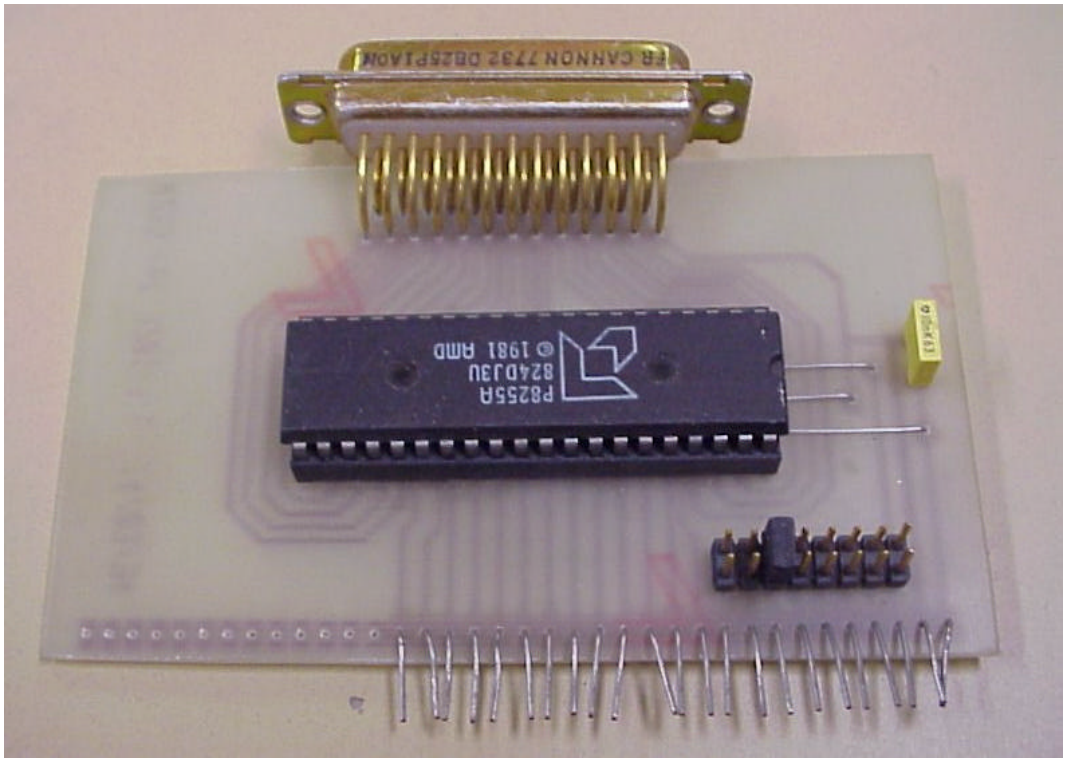

Figure 3.10. Photos de la carte (images-maquettes\8255-32-1.jpg).

3.6 Liste des documents

- Prix du montage.
- Schéma électronique.
- Circuit imprimé.
- Implantation des composants.

Tableau 3.2. Liste des composants 8255 - Ref 32xx.

Réf.	Désignation	Qu.	Fournisseur	Date	Code Cde	Page	Prix U.H.T.	Prix T.H.T.
C1	10 nF 63 V MKT	1					1.20 F	1.20 F
CI1	8255	1					25.00 F	25.00 F
Divers	Support double-lyre 40 broches	1					5.60 F	5.60 F
Divers	Barrette coudée dorée x points	1					17.80 F	17.80 F
Divers	Barrette droite dorée x points	1					6.00 F	6.00 F
Divers	Cavalier	1					1.20 F	1.20 F
Divers	Prise DB coudée sur C.I.	1					25.00 F	25.00 F
Divers	Circuit impriméS.F. x mm ref	35					0.15 F	5.25 F

TOTAL H.T. :		87.05 F
dont T.V.A.	19.60%	17.06 F
TOTAL T.T.C. :		104.11 F

Projet 3 - PIO8255 / Extension PIO 8255, réf. 3Yxx.

Projet : ES_PC

Info : [DATA103]

3.1 Documentation du 82C55A

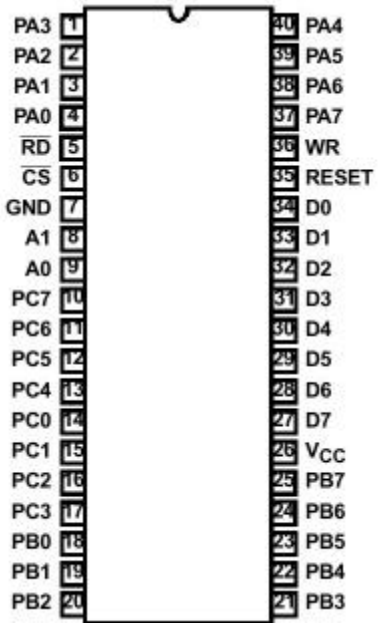

Figure 3.1. Brochage du 825C55A (images\8255-d.jpg).

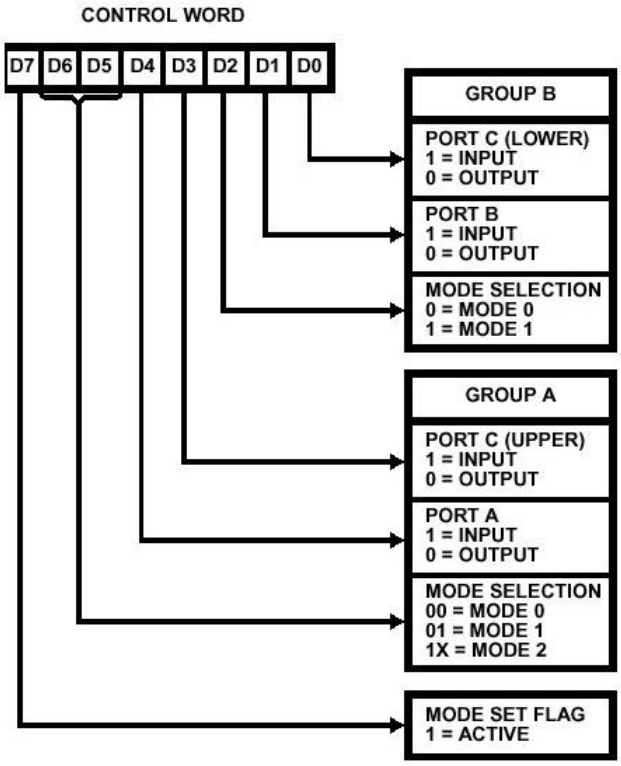

Figure 3.2. Mot de contrôle du 825C55A (images\8255-c.jpg).

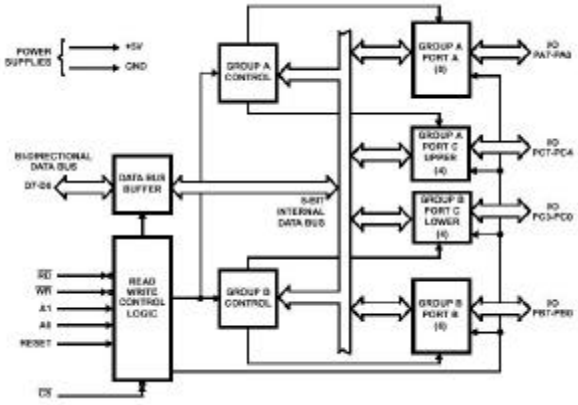

Figure 3.3. Organisation interne du 825C55A (images\8255-a.jpg).

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	26		V_{CC}: The +5V power supply pin. A 0.1μF capacitor between pins 26 and 7 is recommended for decoupling.
GND	7		GROUND
D0-D7	27-34	I/O	DATA BUS: The Data Bus lines are bidirectional three-state pins connected to the system data bus.
RESET	35	I	RESET: A high on this input clears the control register and all ports (A, B, C) are set to the input mode with the "Bus Hold" circuitry turned on.
$\overline{CS}$	6	I	CHIP SELECT: Chip select is an active low input used to enable the 82C55A onto the Data Bus for CPU communications.
$\overline{RD}$	5	I	READ: Read is an active low input control signal used by the CPU to read status information or data via the data bus.
$\overline{WR}$	36	I	WRITE: Write is an active low input control signal used by the CPU to load control words and data into the 82C55A.
A0-A1	8, 9	I	ADDRESS: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word register. A0 and A1 are normally connected to the least significant bits of the Address Bus A0, A1.
PA0-PA7	1-4, 37-40	I/O	PORT A: 8-bit input and output port. Both bus hold high and bus hold low circuitry are present on this port.
PB0-PB7	18-25	I/O	PORT B: 8-bit input and output port. Bus hold high circuitry is present on this port.
PC0-PC7	10-17	I/O	PORT C: 8-bit input and output port. Bus hold circuitry is present on this port.

Figure 3.4. Définition des broches du 825C55A (images\8255-b.jpg).