3.2 Modèle 8255 - Référence 31xx

Révision : du 3102 du 5 mars 1994.

Révision : du 3103 du 3 juin 2001.

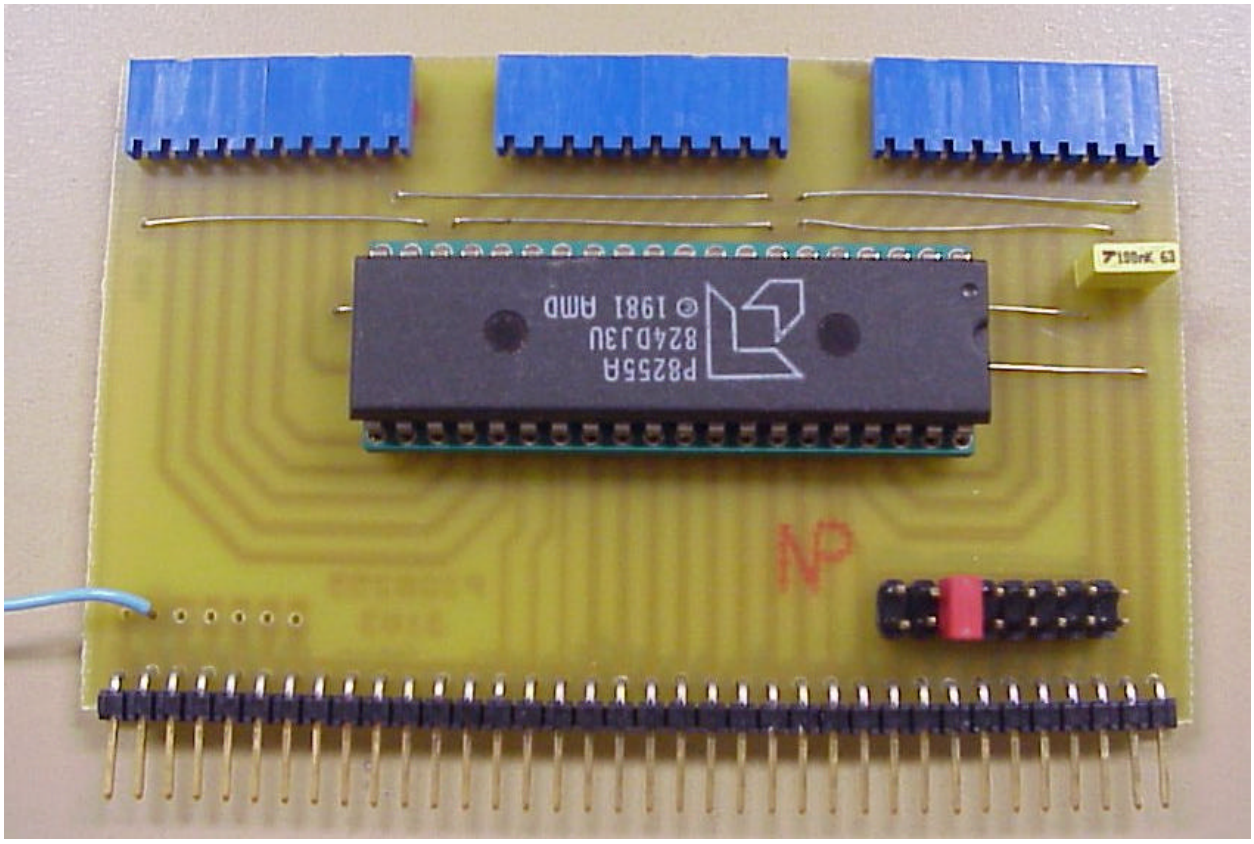


Figure 3.5. Photos de la carte (images-maquettes\pio8255-31-1.jpg).

3.3 Liste des documents

- Prix du montage.
- Schéma électronique.
- Circuit imprimé.
- Implantation des composants.

Tableau 3.1. Liste des composants 8255 - Ref 31xx.

N°	Quantité	Référence	Désignation	Empreinte
1	1	C1	100nF	CK06
2	1	JP1	THY-BUS	36PL1
3	1	JP2	HE10	16SH
4	3	JP3,JP4,JP5	HE14	20DIP300L
5	1	JP6	CLOCK	07PL1
6	1	U1	82C55A	40DIP600L

3.4 Câblage des connecteurs HE14 femelle de sortie

GND	1	1	GND
PB7	2	2	PB7
PB6	3	3	PB6
PB5	4	4	PB5
PB4	5	5	PB4
PB3	6	6	PB3
PB2	7	7	PB2
PB1	8	8	PB1
PB0	9	9	PB0
+5V	10	10	+5V

Figure 3.6. Connecteur PORT B.

GND	1	1	GND
PC3	2	2	PC3
PC2	3	3	PC2
PC1	4	4	PC1
PC0	5	5	PC0
PC4	6	6	PC4
PC5	7	7	PC5
PC6	8	8	PC6
PC7	9	9	PC7
+5V	10	10	+5V

Figure 3.7. Connecteur PORT C.

GND	1	1	GND
PA0	2	2	PA0
PA1	3	3	PA1
PA2	4	4	PA2
PA3	5	5	PA3
PA4	6	6	PA4
PA5	7	7	PA5
PA6	8	8	PA6
PA7	9	9	PA7
+5V	10	10	+5V

Figure 3.8. Connecteur JP4 - port A.

25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10		9	8	7	6	5	4	3	2	1
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PC3	PC2	PC1	PC0	PC4	PC5	PC6	PC7		PA0	PA1	PA2	PA3	PA4	PA5	PA6	PA7	GND

Figure 3.9. Câblage du connecteur de sortie - Réf. 3101.

Projet 3 - PIO8255 / Extension PIO 8255, réf. 3Yxx.

Projet : ES_PC

Info : [DATA103]

3.1 Documentation du 82C55A

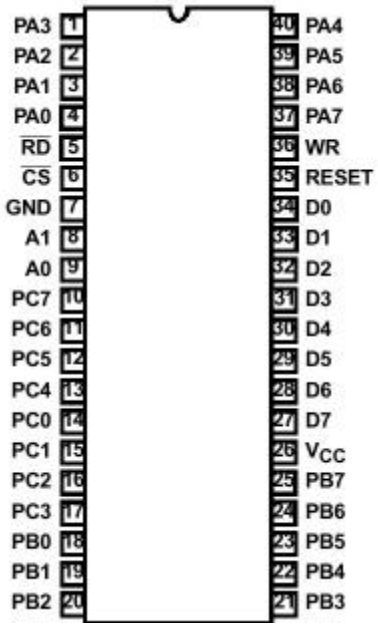


Figure 3.1. Brochage du 825C55A (images\8255-d.jpg).

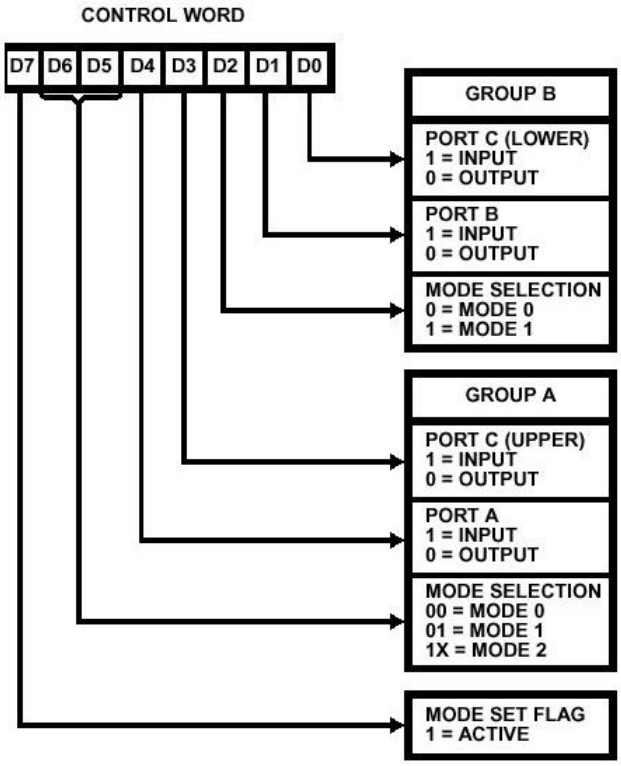


Figure 3.2. Mot de contrôle du 825C55A (images\8255-c.jpg).

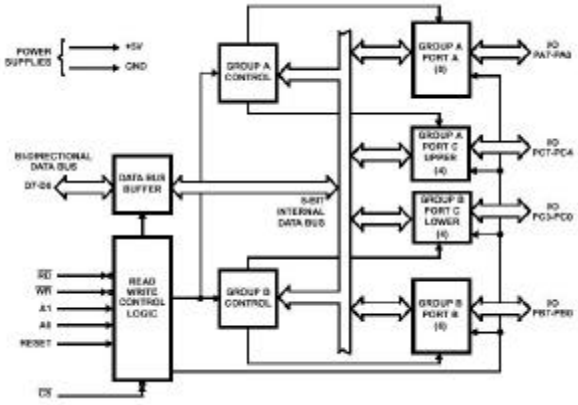
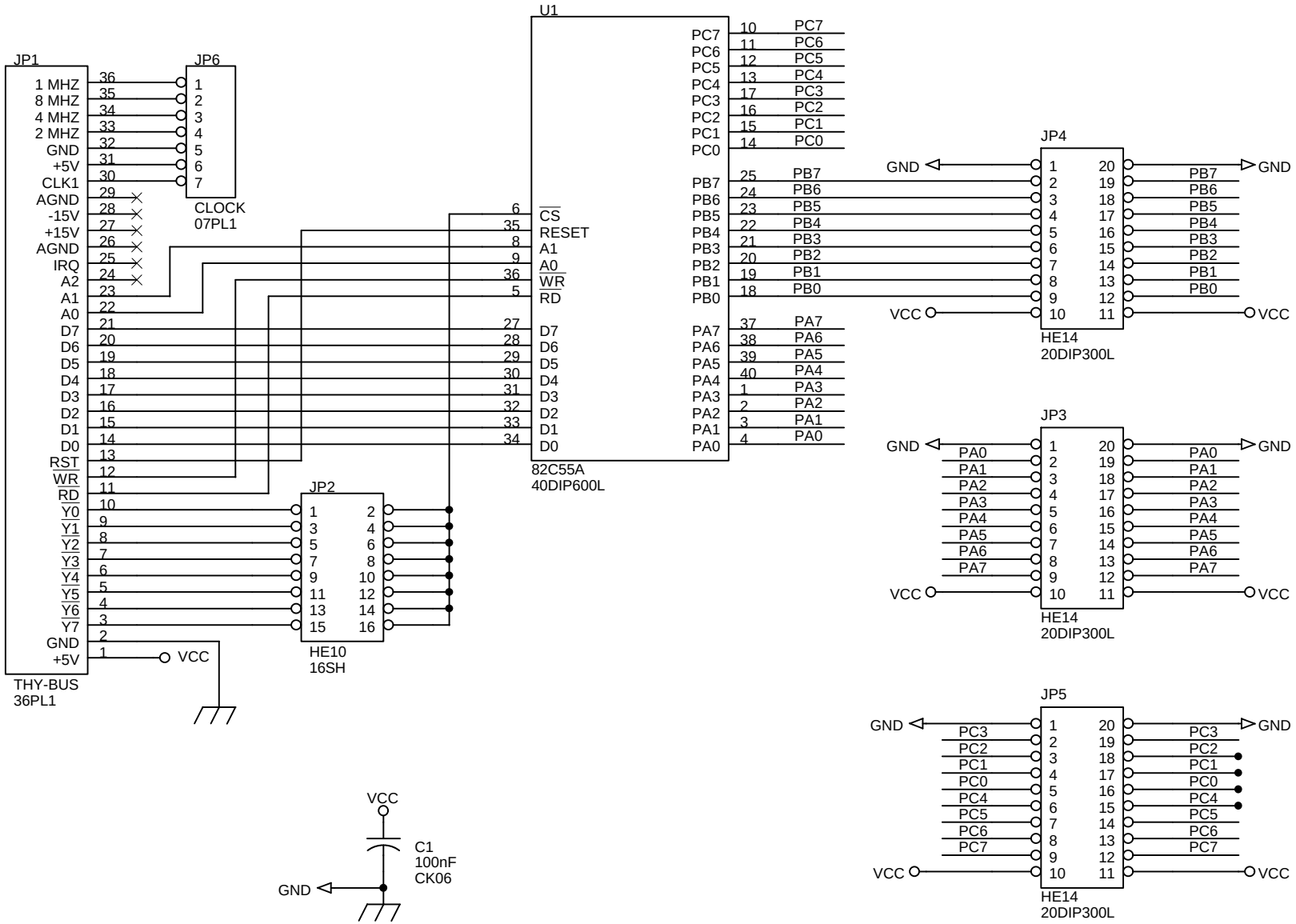


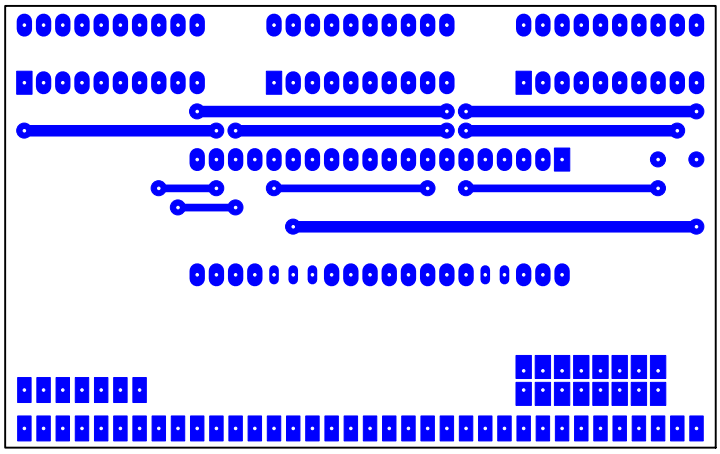
Figure 3.3. Organisation interne du 825C55A (images\8255-a.jpg).

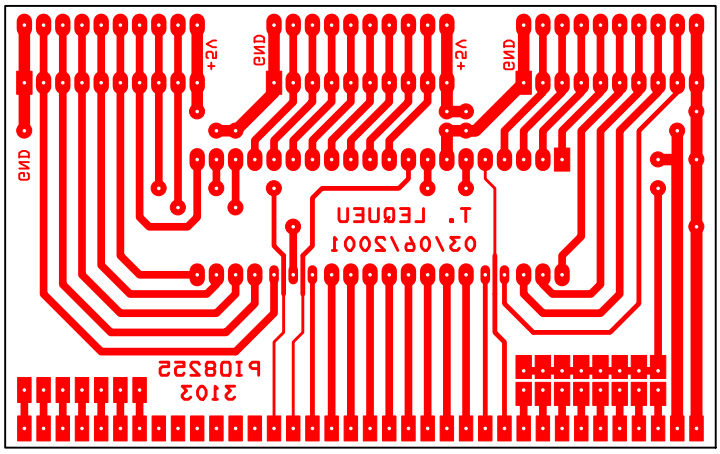
SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	26		V_{CC}: The +5V power supply pin. A 0.1μF capacitor between pins 26 and 7 is recommended for decoupling.
GND	7		GROUND
D0-D7	27-34	I/O	DATA BUS: The Data Bus lines are bidirectional three-state pins connected to the system data bus.
RESET	35	I	RESET: A high on this input clears the control register and all ports (A, B, C) are set to the input mode with the "Bus Hold" circuitry turned on.
$\overline{CS}$	6	I	CHIP SELECT: Chip select is an active low input used to enable the 82C55A onto the Data Bus for CPU communications.
$\overline{RD}$	5	I	READ: Read is an active low input control signal used by the CPU to read status information or data via the data bus.
$\overline{WR}$	36	I	WRITE: Write is an active low input control signal used by the CPU to load control words and data into the 82C55A.
A0-A1	8, 9	I	ADDRESS: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word register. A0 and A1 are normally connected to the least significant bits of the Address Bus A0, A1.
PA0-PA7	1-4, 37-40	I/O	PORT A: 8-bit input and output port. Both bus hold high and bus hold low circuitry are present on this port.
PB0-PB7	18-25	I/O	PORT B: 8-bit input and output port. Bus hold high circuitry is present on this port.
PC0-PC7	10-17	I/O	PORT C: 8-bit input and output port. Bus hold circuitry is present on this port.

Figure 3.4. Définition des broches du 825C55A (images\8255-b.jpg).



Auteur : Thierry LEQUEU		
Title: Carte d'extension THY-BUS 8255		
Size: A	Document Number: ES_PC / [DATA103] / PIO8255 - Référence 3103	Rev: 3
Date: Sunday, June 17, 2001	Sheet 1 of 1	

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GND
+5v
GND
GND
T. LEQUEU
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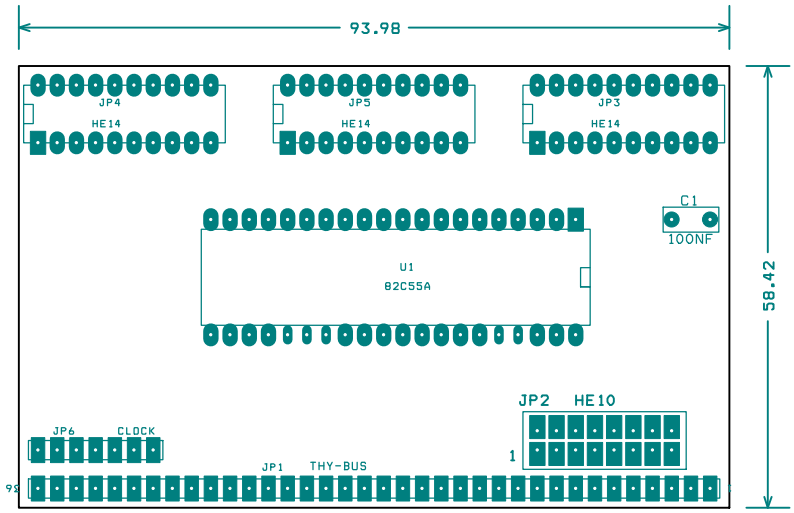
P10B255
3103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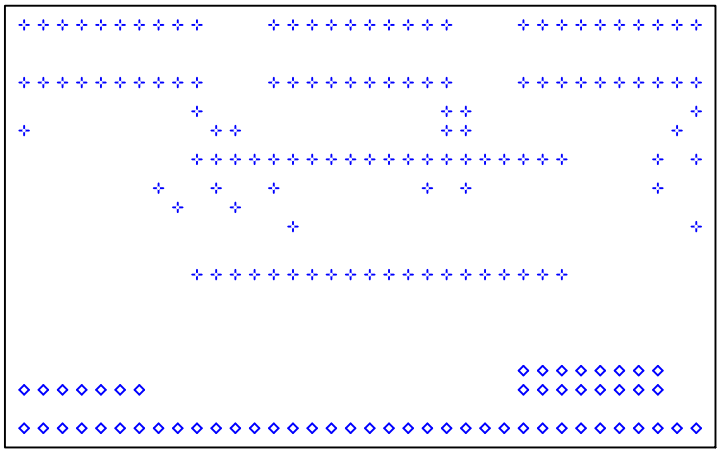
58.42
JP4
HE14
JP5
HE14
JP3
HE14
C1
100NF
U1
82C55A
JP2 HE10
1
JP6 CLOCK
JP1 THY-BUS
98



DRILL CHART				
SYM	DIAM	TOL	QTY	NOTE
+	0.031		122	
◇	0.039		59	
TOTAL			181	