# OKI Semiconductor

# MSM82C53-2RS/GS/JS

## CMOS PROGRAMMABLE INTERVAL TIMER

### GENERAL DESCRIPTION

The MSM82C53-2RS/GS/JS is programmable universal timers designed for use in microcomputer systems. Based on silicon gate CMOS technology, it requires a standby current of only 100 μA (max.) when the chip is in the nonselected state. During timer operation, power consumption is still very low only 8 mA (max.) at 8 MHz of current required.

The device consists of three independent counters, and can count up to a maximum of 8 MHz (MSM82C53-2). The timer features six different counter modes, and binary count/BCD count functions. Count values can be set in byte or word units, and all functions are freely programmable.
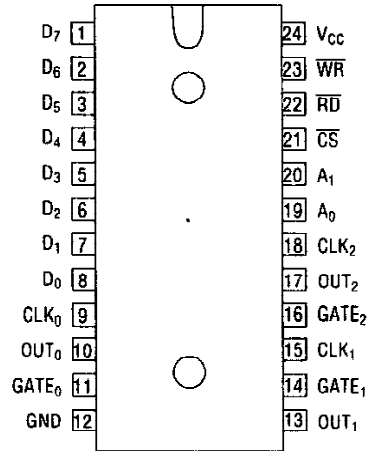
### FEATURES

- Maximum operating frequency of 8 MHz (MSM82C53-2)
- High speed and low power consumption achieved through silicon gate CMOS technology
- Completely static operation
- Three independent 16-bit down-counters
- 3 V to 6 V single power supply
- Six counter modes available for each counter
- Binary and decimal counting possible
- 24-pin Plastic DIP (DIP24-P-600): MSM82C53-2RS
- 28-pin Plastic QFJ (QFJ28-P-S450): MSM82C53-2JS
- 32-pin Plastic SSOP(SSOP32-P-430-K): MSM82C53-2GS-K
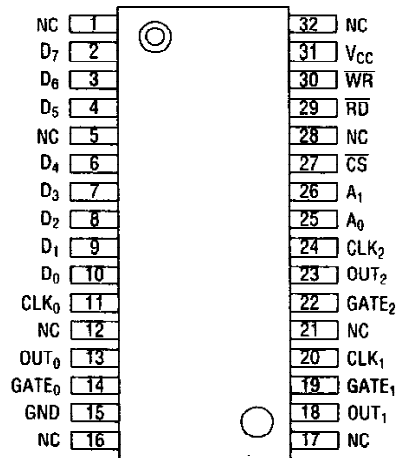
## FUNCTIONAL BLOCK DIAGRAM
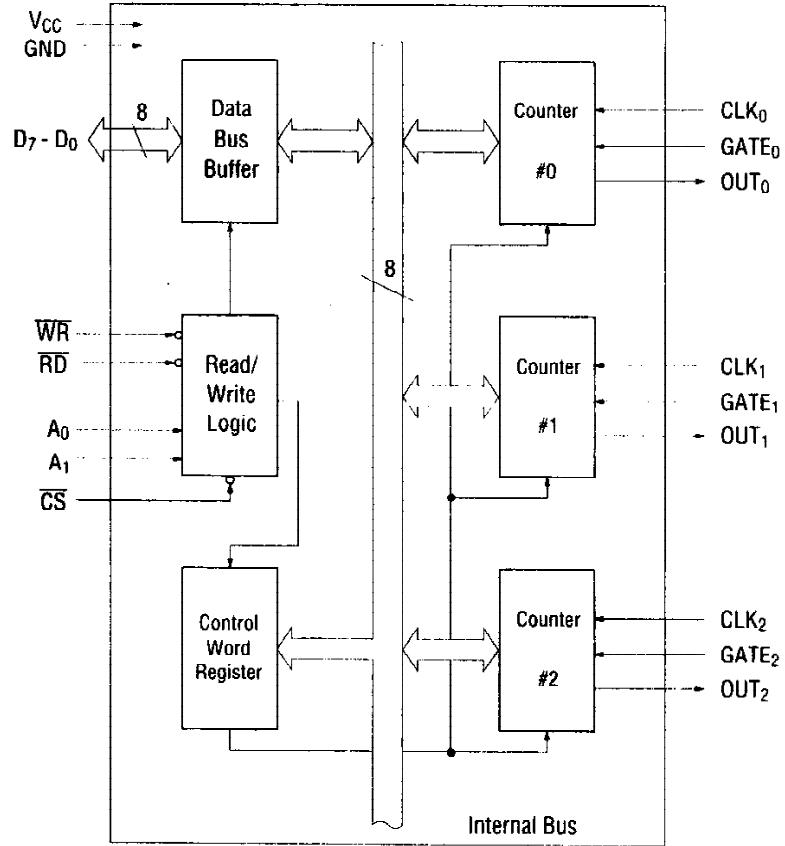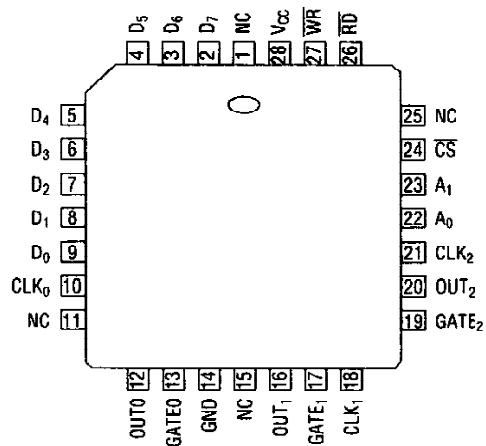
## PIN CONFIGURATION (TOP VIEW)

**24 pin Plastic DIP**

| | |
|---|---|
| $D_7$ [1] | [24] $V_{CC}$ |
| $D_6$ [2] | [23] $\overline{WR}$ |
| $D_5$ [3] | [22] $\overline{RD}$ |
| $D_4$ [4] | [21] $\overline{CS}$ |
| $D_3$ [5] | [20] $A_1$ |
| $D_2$ [6] | [19] $A_0$ |
| $D_1$ [7] | [18] $CLK_2$ |
| $D_0$ [8] | [17] $OUT_2$ |
| $CLK_0$ [9] | [16] $GATE_2$ |
| $OUT_0$ [10] | [15] $CLK_1$ |
| $GATE_0$ [11] | [14] $GATE_1$ |
| GND [12] | [13] $OUT_1$ |

**32 pin Plastic SSOP**

| | |
|---|---|
| NC [1] | [32] NC |
| $D_7$ [2] | [31] $V_{CC}$ |
| $D_6$ [3] | [30] $\overline{WR}$ |
| $D_5$ [4] | [29] $\overline{RD}$ |
| NC [5] | [28] NC |
| $D_4$ [6] | [27] $\overline{CS}$ |
| $D_3$ [7] | [26] $A_1$ |
| $D_2$ [8] | [25] $A_0$ |
| $D_1$ [9] | [24] $CLK_2$ |
| $D_0$ [10] | [23] $OUT_2$ |
| $CLK_0$ [11] | [22] $GATE_2$ |
| NC [12] | [21] NC |
| $OUT_0$ [13] | [20] $CLK_1$ |
| $GATE_0$ [14] | [19] $GATE_1$ |
| GND [15] | [18] $OUT_1$ |
| NC [16] | [17] NC |

(NC denotes "not connected")

**28 pin Plastic QFJ**

Top pins (left to right): $D_5$ [4], $D_6$ [3], $D_7$ [2], NC [1], $V_{CC}$ [28], $\overline{WR}$ [27], $\overline{RD}$ [26]

Left pins (top to bottom): $D_4$ [5], $D_3$ [6], $D_2$ [7], $D_1$ [8], $D_0$ [9], $CLK_0$ [10], NC [11]

Bottom pins (left to right): $OUT_0$ [12], $GATE_0$ [13], GND [14], NC [15], $OUT_1$ [16], $GATE_1$ [17], $CLK_1$ [18]

Right pins (top to bottom): NC [25], $\overline{CS}$ [24], $A_1$ [23], $A_0$ [22], $CLK_2$ [21], $OUT_2$ [20], $GATE_2$ [19]

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | | | Units |
|---|---|---|---|---|---|---|
| | | | MSM82C53-2RS | MSM82C53-2GS | MSM82C53-2JS | |
| Supply Voltage | $V_{CC}$ | Respect to GND | −0.5 to +7 | | | V |
| Input Voltage | $V_{IN}$ | | −0.5 to $V_{CC}$ + 0.5 | | | V |
| Output Voltage | $V_{OUT}$ | | −0.5 to $V_{CC}$ + 0.5 | | | V |
| Storage Temperature | $T_{STG}$ | — | −55 to +150 | | | °C |
| Power Dissipation | $P_D$ | Ta = 25°C | 0.9 | 0.7 | 0.9 | W |

## OPERATING RANGES

| Parameter | Symbol | Condition | Range | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | $V_{IL}$ = 0.2 V, $V_{IH}$ = $V_{CC}$ −0.2 V, Operating Frequency 2.6 MHz | 3 to 6 | V |
| Operating Temperature | $T_{op}$ | | −40 to +85 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5 | 5.5 | V |
| Operating Temperature | $T_{op}$ | −40 | +25 | +85 | °C |
| "L" Input Voltage | $V_{IL}$ | −0.3 | — | +0.8 | V |
| "H" Input Voltage | $V_{IH}$ | 2.2 | — | $V_{CC}$ + 0.3 | V |

## DC CHARACTERISTICS

| Parameter | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| "L" Output Voltage | $V_{OL}$ | $I_{OL}$ = 4 mA | | — | — | 0.45 | V |
| "H" Output Voltage | $V_{OH}$ | $I_{OH}$ = −1 mA | | 3.7 | — | — | V |
| Input Leak Current | $I_{LI}$ | $0 \le V_{IN} \le V_{CC}$ | $V_{CC}$ = 4.5 V to 5.5 V Ta = −40°C to +85°C | −10 | — | 10 | μA |
| Output Leak Current | $I_{LO}$ | $0 \le V_{OUT} \le V_{CC}$ | | −10 | — | 10 | μA |
| Standby Supply Current | $I_{CCS}$ | $\overline{CS} \ge V_{CC}$ - 0.2 V $V_{IH} \ge V_{CC}$ - 0.2 V $V_{IL} \le 0.2$ V | | — | — | 100 | μA |
| Operating Supply Current | $I_{CC}$ | $t_{CLK}$ = 125 ns $C_L$ = 0 pF | | — | — | 8 | mA |

1 (x)

## AC CHARACTERISTICS

(V$_{CC}$ = 4.5 V to 5.5 V, Ta = −40 to +85°C)

| Parameter | Symbol | MSM82C53-2 | | Unit | Condition |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Address Set-up Time before Reading | t$_{AR}$ | 30 | — | ns | Read Cycle |
| Address Hold Time after Reading | t$_{RA}$ | 0 | — | ns | |
| Read Pulse Width | t$_{RR}$ | 150 | — | ns | |
| Read Recovery Time | t$_{RVR}$ | 200 | — | ns | |
| Address Set-up Time before Writing | t$_{AW}$ | 0 | — | ns | Write Cycle |
| Address Hold Time after Writing | t$_{WA}$ | 20 | — | ns | |
| Write Pulse Width | t$_{WW}$ | 150 | — | ns | |
| Data Input Set-up Time before Writing | t$_{DW}$ | 100 | — | ns | |
| Data Input Hold Time after Writing | t$_{WD}$ | 20 | — | ns | |
| Write Recovery Time | t$_{RVW}$ | 200 | — | ns | |
| Clock Cycle Time | t$_{CLK}$ | 125 | D.C. | ns | C$_L$ = 150 pF |
| Clock "H" Pulse Width | t$_{PWH}$ | 60 | — | ns | |
| Clock "L" Pusle Width | t$_{PWL}$ | 60 | — | ns | Clock and Gate Timing |
| "H" Gate Pulse Width | t$_{GW}$ | 50 | — | ns | |
| "L" Gate PUlse Width | t$_{GL}$ | 50 | — | ns | |
| Gate Input Set-up Time before Clock | t$_{GS}$ | 50 | — | ns | |
| Gate Input Hold Time after Clock | t$_{GH}$ | 50 | — | ns | |
| Output Delay Time after Reading | t$_{RD}$ | — | 120 | ns | Delay Time |
| Output Floating Delay Time after Reading | t$_{DF}$ | 5 | 90 | ns | |
| Output Delay Time after Gate | t$_{ODG}$ | — | 120 | ns | |
| Output Delay Time after Clock | t$_{OD}$ | — | 150 | ns | |
| Output Delay Time after Address | t$_{AD}$ | — | 180 | ns | |

Note: Timing measured at V$_L$ = 0.8 V and V$_H$ = 2.2 V for both inputs and outputs.
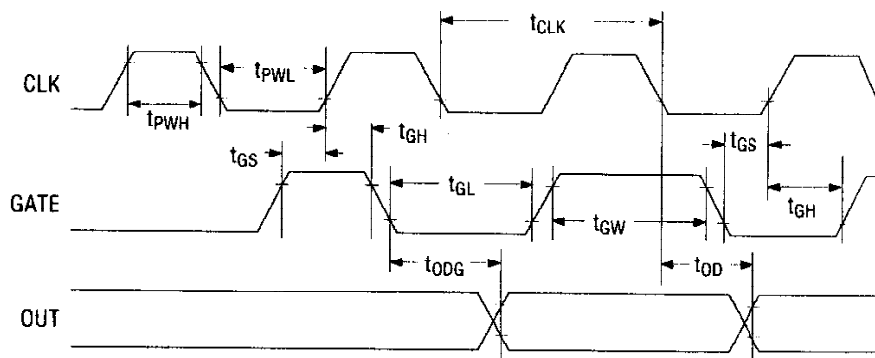
## TIMING CHART

### WriteTiming
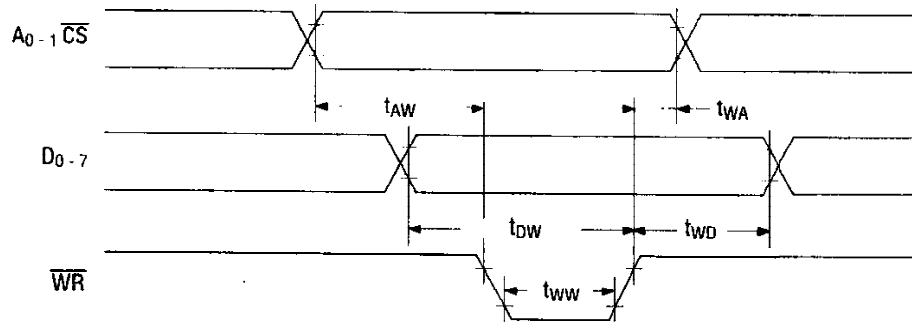


### Read Timing
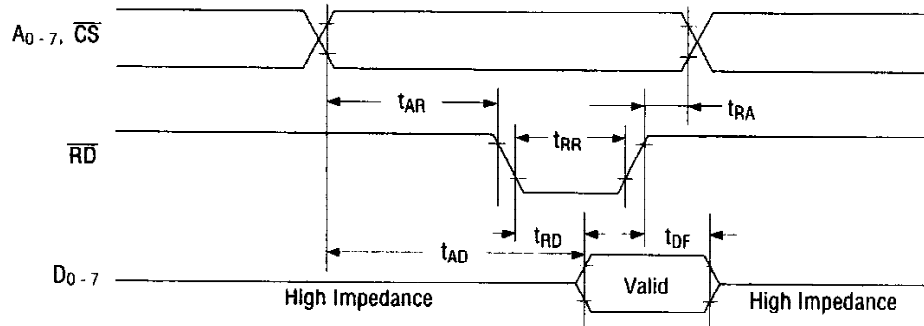


### Clock & Gate Timing

## DESCRIPTION OF PIN FUNCTIONS

| Pin Symbol | Name | Input/Output | Function |
|---|---|---|---|
| $D_7 - D_0$ | Bidirectional Data Bus | Input/Output | Three-state 8-bit bidirectional data bus used when writing control words and count values, and reading count values upon reception of $\overline{WR}$ and $\overline{RD}$ signals from CPU. |
| $\overline{CS}$ | Chip Select Input | Input | Data transfer with the CPU is enabled when this pin is at low level. When at high level, the data bus ($D_0$ thru $D_7$) is switched to high impedance state where neither writing nor reading can be executed. Internal registers, however, remain unchanged. |
| $\overline{RD}$ | Read Input | Input | Data can be transferred from MSM82C53-2 to CPU when this pin is at low level. |
| $\overline{WR}$ | Write Input | Input | Data can be transferred from CPU to MSM82C53-2 when this pin is at low level. |
| $A_0 - A_1$ | Address Input | Input | One of the three internal counters or the control word register is selected by $A_0/A_1$ combination. These two pins are normally connected to the two lower order bits of the address bus. |
| $CLK_{0-2}$ | Clock Input | Input | Supply of three clock signals to the three counters incorporated in MSM82C53-2. |
| $GATE_{0-2}$ | Gate Input | Input | Control of starting, interruption, and restarting of counting in the three respective counters in accordance with the set control word contents. |
| $OUT_{0-2}$ | Counter Output | Output | Output of counter output waveform in accordance with the set mode and count value. |

## SYSTEM INTERFACING
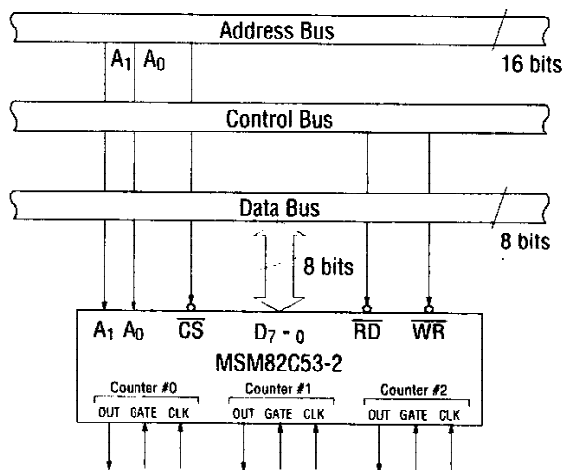
## DESCRIPTION OF BASIC OPERATIONS

Data transfers between the internal registers and the external data bus is outlined in the following table.

| $\overline{CS}$ | $\overline{RD}$ | $\overline{WR}$ | $A_1$ | $A_0$ | Function |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | Data Bus to Counter #0 Writing |
| 0 | 1 | 0 | 0 | 1 | Data Bus to Counter #1 Writing |
| 0 | 1 | 0 | 1 | 0 | Data Bus to Counter #2 Writing |
| 0 | 1 | 0 | 1 | 1 | Data Bus to Control Word Register Writing |
| 0 | 0 | 1 | 0 | 0 | Data Bus from Counter #0 Reading |
| 0 | 0 | 1 | 0 | 1 | Data Bus from Counter #1 Reading |
| 0 | 0 | 1 | 1 | 0 | Data Bus from Counter #2 Reading |
| 0 | 0 | 1 | 1 | 1 | Data Bus High Impedance Status |
| 1 | × | × | × | × | Data Bus High Impedance Status |
| 0 | 1 | 1 | × | × | Data Bus High Impedance Status |

× denotes "not specified".

## DESCRIPTION OF OPERATION

MSM82C53-2 functions are selected by a control word from the CPU. In the required program sequence, the control word setting is followed by the count value setting and execution of the desired timer operation.

### Control Word and Count Value Program

Each counter operation mode is set by control word programming. The control word format is outlined below.

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| SC1 | SC0 | RL1 | RL0 | M2 | M1 | M0 | BCD |
| Select Counter | | Read/Load | | Mode | | | BCD |

($\overline{CS}$=0, $A_0$, $A_1$=1, 1, $\overline{RD}$=1, $\overline{WR}$=0)

• **Select Counter (SC0, SC1):** Selection of set counter

| SC1 | SC0 | Set Contents |
|-----|-----|--------------|
| 0 | 0 | Counter #0 Selection |
| 0 | 1 | Counter #1 Selection |
| 1 | 0 | Counter #2 Selection |
| 1 | 1 | Illegal Combination |

• **Read/Load (RL1, RL0):** Count value Reading/Loading format setting

| RL1 | RL0 | Set Contents |
|-----|-----|--------------|
| 0 | 0 | Counter Latch Operation |
| 0 | 1 | Reading/Loading of Least Significant Byte (LSB) |
| 1 | 0 | Reading/Loading of Most Significant Byte (MSB) |
| 1 | 1 | Reading/Loading of LSB Followed by MSB |

• **Mode (M2, M1, M0):** Operation waveform mode setting

| M2 | M1 | M0 | Set Contents |
|-----|-----|-----|--------------|
| 0 | 0 | 0 | Mode 0 (Interrupt on Terminal Count) |
| 0 | 0 | 1 | Mode 1 (Programmable One-Shot) |
| × | 1 | 0 | Mode 2 (Rate Generator) |
| × | 1 | 1 | Mode 3 (Square Wave Generator) |
| 1 | 0 | 0 | Mode 4 (Software Triggered Strobe) |
| 1 | 0 | 1 | Mode 5 (Hardware Triggered Strobe) |

× denotes "not specified".

• **BCD:** Operation count mode setting

| BCD | Set Contents |
|-----|--------------|
| 0 | Binary Count (16-bit Binary) |
| 1 | BCD Count (4-decade Binary Coded Decimal) |

After setting Read/Load, Mode, and BCD in each counter as outlined above, next set the desired count value. (In some Modes, counting is started immediately after the count value has been written). This count value setting must conform with the Read/Load format set in advance. Note that the internal counters are reset to 0000H during control word setting. The counter value (0000H) can't be read.

If the two bytes (LSB and MSB) are written at this stage (RL0 and RL1 = 1,1), take note of the following precaution.

Although the count values may be set in the three counters in any sequence after the control word has been set in each counter, count values must be set consecutively in the LSB - MSB order in any one counter.

● **Example of control word and count value setting**

Counter #0:  Read/Load LSB only, Mode 3, Binary count, count value 3H
Counter #1:  Read/Load MSB only, Mode 5, Binary count, count value AA00H
Counter #2:  Read/Load LSB and MSB, Mode 0, BCD count, count value 1234

```
MVI  A, 1EH
OUT  n3
```
Counter #0 control word setting

```
MVI  A, 6AH
OUT  n3
```
Counter #1 control word setting

```
MVI  A, B1H
OUT  n3
```
Counter #2 control word setting

```
MVI  A, 03H
OUT  n0
```
Counter #0 control value setting

```
MVI  A, AAH
OUT  n1
```
Counter #1 control value setting

```
MVI  A, 34H
OUT  n2
MVI  A, 12H
OUT  n2
```
Counter #2 count value setting (LSB then MSB)

**Notes:**  n0: Counter #0 address
n1: Counter #1 address
n2: Counter #2 address
n3: Control word register address

● **The minimum and maximum count values which can be counted in each mode are listed below.**

| Mode | Min. | Max. | Remarks |
|------|------|------|---------|
| 0 | 1 | 0 | 0 executes 10000H count (ditto in other modes) |
| 1 | 1 | 0 | — |
| 2 | 2 | 0 | 1 cannot be counted |
| 3 | 2 | 1 | 1 executes 10001H count |
| 4 | 1 | 0 | — |
| 5 | 1 | 0 | — |

## Mode Definition

### • Mode 0 (terminal count)

The counter output is set to "L" level by the mode setting. If the count value is then written in the counter with the gate input at "H" level (that is, upon completion of writing the MSB when there are two bytes), the clock input counting is started. When the terminal count is reached, the output is switched to "H" level and is maintained in this status until the control word and count value are set again.

Counting is interrupted if the gate input is switched to "L" level, and restarted when switched back to "H" level.

When Count Values are written during counting, the operation is as follows:

1-byte Read/Load. ............... When the new count value is written, counting is stopped immediately, and then restarted at the new count value by the next clock.

2-byte Read/Load ............... When byte 1 (LSB) of the new count value is written, counting is stopped immediately. Counting is restarted at the new count value when byte 2 (MSB) is written.

### • Mode 1 (programmable one-shot)

The counter output is switched to "H" level by the mode setting. Note that in this mode, counting is not started if only the count value is written. Since counting has to be started in this mode by using the leading edge of the gate input as a trigger, the counter output is switched to "L" level by the next clock after the gate input trigger. This "L" level status is maintained during the set count value, and is switched back to "H" level when the terminal count is reached.

Once counting has been started, there is no interruption until the terminal count is reached, even if the gate input is switched to "L" level in the meantime. And although counting continues even if a new count value is written during the counting, counting is started at the new count value if another trigger is applied by the gate input.

### • Mode 2 (rate generator)

The counter output is switched to "H" level by the mode setting. When the gate input is at "H" level, counting is started by the next clock after the count value has been written. And if the gate input is at "L" level, counting is started by using the rising edge of the gate input as a trigger after the count value has been set.

An "L" level output pulse appears at the counter output during a single clock duration once every n clock inputs where n is the set count value. If a new count value is written during while counting is in progress, counting is started at the new count value following output of the pulse currently being counted. And if the gate input is switched to "L" level during counting, the counter output is forced to switch to "H" level, the counting being restarted by the rising edge of the gate input.

### • Mode 3 (square waveform rate generator)

The counter output is switched to "H" level by the mode setting. Counting is started in the same way as described for mode 2 above.

The repeated square wave output appearing at the counter output contains half the number of counts as the set count value. If the set count value (n) is an odd number, the repeated square wave output consists of only (n+1)/2 clock inputs at "H" level and (n-1)/2 clock inputs at "L" level.

If a new count value is written during counting, the new count value is reflected immediately after the change ("H" to "L" or "L" to "H") in the next counter output to be executed. The counting operation at the gate input is done the same as in mode 2.

* **Mode 4 (software trigger strobe)**

   The counter output is switched to "H" level by the mode setting. Counting is started in the same way as described for mode 0. A single "L" pulse equivalent to one clock width is generated at the counter output when the terminal count is reached.

   This mode differs from 2 in that the "L" level output appears one clock earlier in mode 2, and that pulses are not repeated in mode 4. Counting is stopped when the gate input is switched to "L" level, and restarted from the set count value when switched back to "H" level.

* **Mode 5 (hardware trigger strobe)**

   The counter output is switched to "H" level by the mode setting. Counting is started, and the gate input used, in the same way as in mode 1.

   The counter output is identical to the mode 4 output.

   The various roles of the gate input signals in the above modes are summarized in the following table.

| Mode \ Gate | "L" Level Falling Edge | Rising Edge | "H" Level |
|---|---|---|---|
| 0 | Counting not possible | | Counting possible |
| 1 | | (1) Start of counting<br>(2) Retriggering | |
| 2 | (1) Counting not possible<br>(2) Counter output forced to "H" level | Start of counting | Counting possible |
| 3 | (1) Counting not possible<br>(2) Counter output forced to "H" level | Start of counting | Counting possible |
| 4 | Counting not possible | | Counting possible |
| 5 | | (1) Start of counting<br>(2) Retriggering | |

**Mode 0**
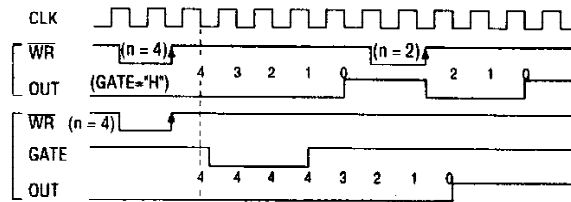


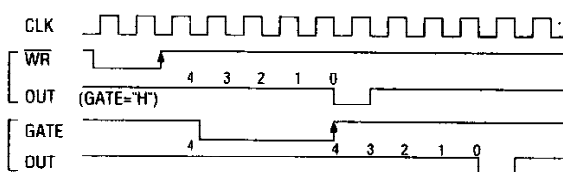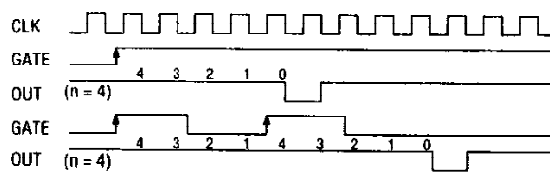**Mode 1**
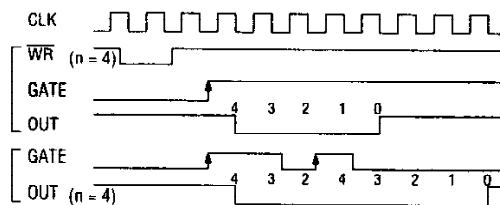


**Mode 2**
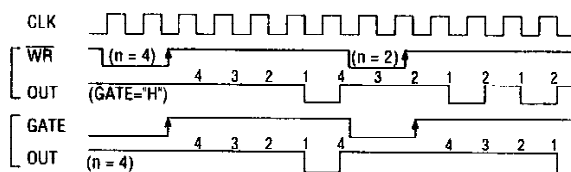


**Mode 3**
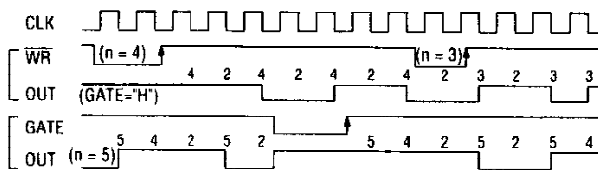


**Mode 4**



**Mode 5**



**Note:** "n" is the value set in the counter.
Figures in these diagrams refer to counter values.

### Reading of Counter Values

All MSM82C53-2 counting is down-counting, the counting being in steps of 2 in mode 3. Counter values can be read during counting by (1) direct reading, and (2) counter latching ("read on the fly").
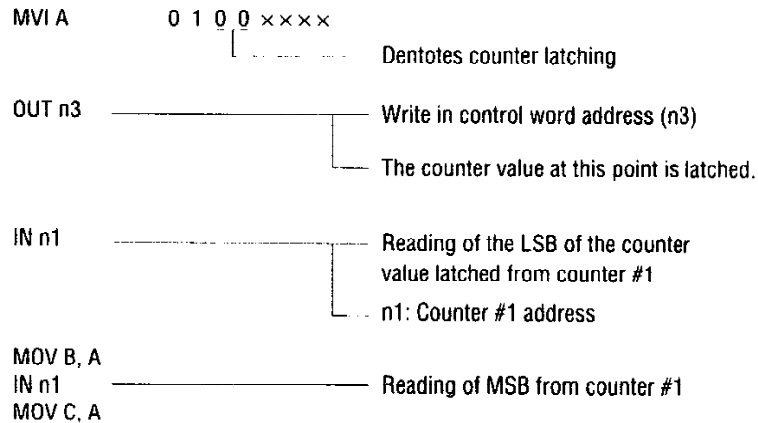
* **Direct reading**
  Counter values can be read by direct reading operations.
  Since the counter value read according to the timing of the $\overline{RD}$ and CLK signals is not guaranteed, it is necessary to stop the counting by a gate input signal, or to interrupt the clock input temporarily by an external circuit to ensure that the counter value is correctly read.
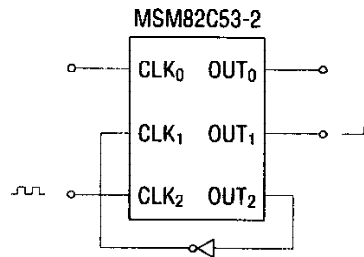
* **Counter latching**
  In this method, the counter value is latched by writing counter latch command, thereby enabling a stable value to be read without effecting the counting in any way at all. An example of a counter latching program is given below.
  Counter latching executed for counter #1 (Read/Load 2-byte setting)

```
MVI A        0 1 0 0 × × × ×
                 └ ‥ ‥ ‥ Dentotes counter latching

OUT n3       ─────────────── Write in control word address (n3)
                             └── The counter value at this point is latched.

IN n1        ─────────────── Reading of the LSB of the counter
                             │  value latched from counter #1
                             └── n1: Counter #1 address

MOV B, A
IN n1        ─────────────── Reading of MSB from counter #1
MOV C, A
```

### Example of Practical Application
* **MSM82C53-2 used as a 32-bit counter.**

MSM82C53-2

```
CLK0   OUT0
CLK1   OUT1
CLK2   OUT2
```

Use counter #1 and counter #2
   Counter #1: mode 0, upper order 16-bit counter
               value
   Counter #2: mode 2, lower order 16-bit counter
               value
This setting enables counting up to a maximum of $2^{32}$.