Optimizing the Design of a High Power Factor Switching Preregulator

by Lloyd Dixon

TOPIC 7

High Power Factor Switching Preregulator Design Optimization

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Summary:

Design of a high power factor active preregulator is optimized to achieve less than 3% harmonic distortion and power factor better than .995 without a sample/hold. The circuit operates over a line voltage range exceeding 3:1 and at loads approaching zero. Under these wide-ranging conditions, the loop gain is constant and the dynamic response to large transient changes in line and load is excellent.

General Perspective

Off-line switching power supplies have historically used full wave rectifier bridges with simple capacitor input filters to power the DC input bus. The line current waveform is a narrow pulse resulting in notoriously poor power factor (0.5–0.6) and harmonic distortion (>100% of the fundamental). Line circuit breakers trip prematurely, and line noise causes a variety of problems.

Among the wide variety of active methods for improving power factor and harmonic distortion, the circuit of Fig. 1 is remarkably effective. An earlier version of this circuit was discussed in detail in Ref. [1].

Summarizing the operation of Fig. 1, the block labeled "High Power Factor Switching Preregulator" contains a power circuit (boost, flyback or buck) and an *input* current control circuit. The preregulator is controlled by current programming signal I_{CP} to draw input current in a nearly perfect rectified sine waveform in phase with the input voltage.

The current programming signal I_{CP} is generated by multiplying a full-wave rectified "pattern" i_{AC} derived from V_{IN} by a control level that varies inversely with output voltage deviation. This voltage control loop crudely regulates the output bus voltage.

A voltage V_{FF} proportional to rms input volts is squared and divided into the control level. This feature is essential to operation over a wide range of input and output conditions with constant loop gain and good response.

Although the circuit appears complex, all of the control functions shown in Fig. 1, including current control within the preregulator block, have been incorporated into a single integrated circuit–the UC3854 [3].

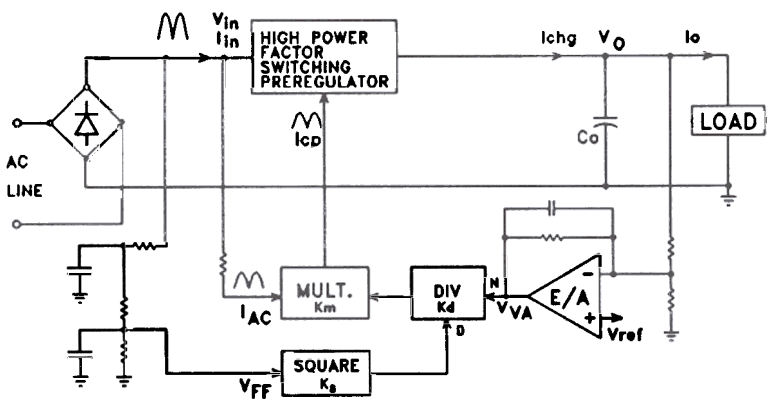

Fig. 1 - High Power Factor Preregulator

Confusion can easily occur between line frequency and switching frequency values - peak 60 Hz current is average 100kHz, peak 100kHz may be much higher than the 60 Hz peak.

To simplify the discussion, 60 Hz line frequency and 100kHz switching frequency is normally assumed.

Sources of Harmonic Distortion:

In high power factor preregulator circuits similar to the ones discussed in this paper, input current distortion is mainly 3rd harmonic, arising from two sources: (1) Input current fails to track perfectly with the sine wave programming signal. (2) The current programming signal is distorted by 2nd harmonics from the output voltage feedback and from the feedforward voltage.

Input Current Control Accuracy: The various input current control methods used historically leave much to be desired in control accuracy, making it difficult obtain low distortion:

1. Conventional current mode control (CMC) actually controls peak inductor current. In the boost topology the inductor is in the input circuit, so that CMC is well suited to control input current. The most serious problem with peak CMC is the error between peak current (which is the basis of control) and the 100kHz state-space averaged current (which it is desired to control). At low 60 Hz current levels, at high line voltage and/or light loads, the peak/avg error becomes much worse. If the current goes below the mode boundary into the discontinuous mode, the error becomes huge. A large inductance value is required to reduce the tracking error to an acceptable level for less critical applications, and it is near impossible to achieve really low harmonic distortion. Also, peak CMC is very noise sensitive, and plenty of noise is generated in this application.

2. Hysteretic CMC control methods can eliminate peak/avg error in a boost converter by "bracketing" the average value. Some hysteretic CMC methods avoid the discontinuous mode by making the hysteresis band proportional to the instantaneous 60 Hz current level. With hysteretic control, the switching frequency varies widely and it is also noise sensitive.

3. Neither peak nor hysteretic CMC is well suited for flyback or buck input current control because the controlled (inductor) current is *not* the input current. In these topologies, input current equals inductor current times duty cycle, and duty cycle changes greatly as the input voltage traverses the sine wave from zero to peak.

4. Discontinuous flyback circuits are simple to control. By fixing the duty cycle throughout each 60Hz half-period, the 100kHz averaged current will track the 60 Hz voltage waveform (crudely).

5. The technique called Average Current Mode Control [4] overcomes these difficulties. The input current is directly sensed and averaged, then compared to the current programming signal. Tracking errors are corrected quickly and accurately by a high gain-bandwidth current loop using a dedicated operational amplifier. Less than 1% distortion due to tracking error is easy to achieve.

Average CMC works with any topology, continuous or discontinuous. It has excellent noise immunity. Best of all, the inductor value can be much smaller because there is no peak/average error and because discontinuous operation is not a problem. Average CMC is discussed in detail in a separate paper published in this Seminar Manual–see Ref. [4].

Distortion Arising from Second Harmonics on the Voltage Error Amplifier Output: With a practical, finite bulk filter capacitor, there will be a few volts of ripple across the output bus, at the second harmonic of the line frequency. This 2nd harmonic feeds back through the voltage error amplifier *VEA*, and causes input 3rd harmonic distortion. (This creates a dilemma: higher *VEA* gain improves dynamic response but worsens distortion.)

The voltage error amplifier *VEA* has a small but finite gain at the 2nd harmonic frequency, 120Hz. The second harmonic ripple voltage present across output capacitor C_O is inverted through the *VEA* and appears at its output as a percentage of the DC control voltage V_{VEA}. Fig. 2(b) shows a 2nd harmonic component of V_{VEA} with peak value 10% of the DC level.

The ripple voltage across C_O lags the ripple current by 90°. If the amplifier gain is flat (as

suggested in [1]) then the 2nd harmonic ripple component of V_{VEA} will lag by a total of 90°. (It is also inverted through the error amplifier.) The 2nd harmonic will be phased with respect to the rectified V_{IN} as shown in Fig. 2(a),(b).

V_{VEA} is multiplied by the sine wave current "pattern" derived from the rectified V_{IN} of Fig. 2(a). The 2nd harmonic component produces distortion in the current programming signal, I_{CP}, and therefore in the input current. Fig. 2(c) shows the ideal and actual rectified input current waveforms resulting from the 10% 2nd harmonic component of V_{VEA}. Subtracting the ideal from the actual reveals the distortion components in Fig. 2(d). Fig. 2(c) and (d) translate into (e) and (f) on the line side of the rectifiers. Note that the ±0.1A scale of (f) corresponds to 10% of the 1A peak ideal line current in (e).

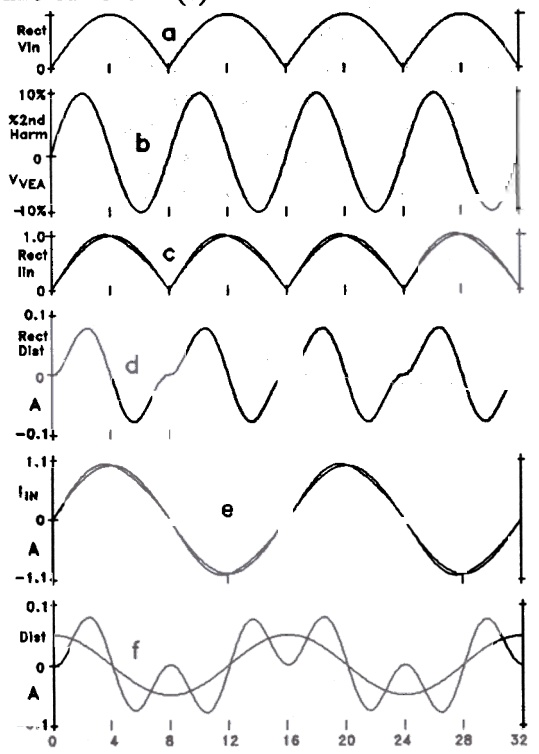

Fig. 2 - 5% 3rd Harmonic Distortion (90° 2nd Harmonic Phase Lag)

The solid line in Fig. 2(e) is the total deviation between the actual and ideal input current waveforms. *The dash line shows that there are two distinct components-a 3rd harmonic component and a 90° leading fundamental component. These two components are equal in amplitude, and are both exactly 5% of the ideal input current sine wave.* The phase-shifted fundamental component is not distortion, but it does hurt the power factor. Note that only the 3rd harmonic is generated. *The line current % 3rd harmonic distortion always equals half the % 2nd harmonic on the VEA output.*

In the preceding example with a flat gain *VEA*, the overall voltage control loop has a single pole characteristic. Performance can be enhanced considerably by adding a pole to the *VEA* below 120Hz at the voltage loop crossover frequency, f_C. This second pole reduces the phase margin at f_C to an ideal 45°. For the same *VEA* gain at 120Hz (and the same input current distortion), the gain at lower frequencies is much higher. This greatly reduces the conflict between low distortion and acceptable dynamic behavior. It is not difficult to achieve less than 3% harmonic distortion and yet handle wide-ranging instantaneous changes in line and load with V_O excursions of only 1-2%.

With the additional pole resulting in a -2 slope at 120Hz, the phase relationships of the distortion components change. As shown in Fig. 3, the 2nd harmonic (still 10%) lags an

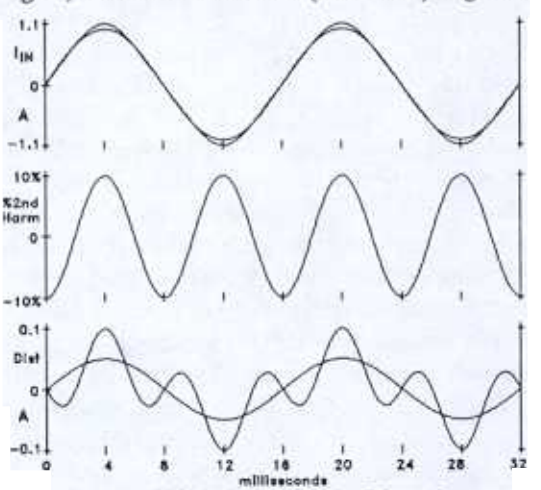

Fig. 3 - 5% 3rd Harmonic Distortion (180° Second Harmonic Phase Lag)

additional 90° through the *VEA*, for a total lag of 180°. The positive peaks of the 2nd harmonic waveform now coincide with the line peaks, distorting the line current waveform by increasing its peak value and taking it toward a triangular shape. Note that the deviation between ideal and actual still has equal 3rd harmonic and fundamental components–both 5%, half the 2nd harmonic–but the fundamental component is now in phase with the line voltage waveform so it is neither distortion nor does it hurt the power factor as it did with the single-pole loop. The fundamental component increases the output power by 5%, but the voltage loop quickly adjusts the *VEA* output downward by 5% to maintain the correct power. The peak current is then only 5% higher than the ideal sine wave, due to the 3rd harmonic peak.

Using a second pole placed at f_C to achieve low distortion with excellent voltage loop bandwidth is only practical when a technique such as voltage feed-forward is used to provide constant control loop gain. Otherwise, loop gain and f_C vary with the V_{IN}^2, making placement of the second pole practically impossible.

Distortion Arising from Second Harmonics on the Feedforward Signal: The feedforward signal V_{FF} is proportional to the rms line voltage. It is obtained by averaging the rectified input voltage, as shown in Fig. 1. The rectified input voltage has a large 2nd harmonic component (66% of the average value). The 2nd harmonic is greatly attenuated through the averaging network, but some 2nd harmonic will exist with the DC feedforward signal, V_{FF}. As an example, 5% 2nd harmonic on V_{FF} is doubled through the squaring circuit to 10%. It remains at 10% through the divider and ultimately results in 5% 3rd harmonic distortion plus 5% fundamental. This process is the same as the distortion caused by 2nd harmonics through the *VEA* shown in Fig. 3 except the V_{FF} harmonics are doubled through the squarer. To summarize: *Line current % 3rd harmonic distortion equals the % 2nd harmonic on* V_{FF}.

Unfortunately, the % 2nd harmonic from V_{VEA} and V_{FF} are in phase at the input of the multiplier and effectively add together. For example, 2% harmonic on V_{FF} plus 2% on $V_{VEA}(/2)$ = 3% 3rd harmonic on the input line current.

The feedforward time constant should be short to get fast correction for sudden line voltage changes, but this increases the 2nd harmonic on V_{FF}. As single pole V_{FF} averaging network with adequate response time produces quit a bit of distortion (see Ref [1]). The 2-pole system shown in Fig. 1 is a great improvement. Fig. 4 shows the improved response of a 2-pole network compared to a 1-pole network with the same % second harmonic output.

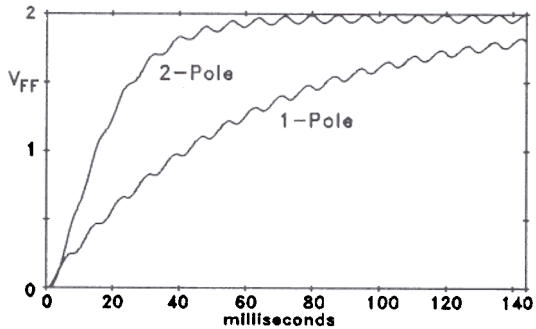

Fig. 4 -- 2-Pole vs. 1-Pole Feedforward

Other even harmonics are present on the rectified V_{IN} waveform, but they are initially much lower amplitude than the 2nd harmonic and are attenuated much more through the feedforward averaging network, so they contribute a negligible amount of input distortion. As a practical matter, only 3rd harmonic distortion is generated through the feedback and feedforward paths. Other harmonic frequencies will be generated if input current tracking is poor, however.

In Ref [1] the statement is made that 3% harmonic distortion is impossible to achieve without a technique such as a sample/hold. But with 2-pole characteristics in the feedback and feedforward paths, this statement is not correct.

Designing the Power Circuit:

Selection of the Power Circuit Topology: Historically, the boost converter operated in the continuous mode has been the most popular configuration. At least part of the reason is that the chopped input current waveforms of the flyback and buck topologies have been difficult to control adequately using peak or hysteretic CMC.

Much greater freedom of choice is possible with average CMC. Input current is directly sensed, averaged and controlled: inductor current with the boost topology, chopped switch current with flyback or buck circuits. Using average CMC, the external characteristics of the closed current loop are identical for all topologies–a flat gain characteristic with single pole roll-off at the current loop crossover frequency.

In addition, any of these topologies can cross the mode boundary and operate effectively in the discontinuous mode. This eliminates concerns regarding minimum loads. For the same reason, the inductance value can be reduced considerably, diminishing cost and weight. Minimum inductance is determined only by considerations of max. peak current in the switch and rectifier at low line voltage. At high line, the full load current might be entirely discontinuous.

With average CMC, the choice of the power circuit can be made on the basis of the application, not the control method. See p4, Ref.[1] for a discussion of the various topologies. Contrary to the statement of unsuitability made in [1], the buck regulator might be the best choice for low voltage outputs such as battery charging or 48V telephone power supplies. The buck regulator will cease functioning as the instantaneous line voltage moves below the output voltage as it approaches zero crossing. This puts a step in the input current waveform. A power factor of 0.98 is easily achievable, however, but not 3% harmonic distortion.

Designing the Boost Converter:

This analysis of a 1kW boost converter power stage shown in Fig. 5will use the following application to demonstrate the design approach:

Input Volts, V_{IN} : 80 - 270 V rms
Output Volts, V_O : 380Vdc
10% Overload Power Limit : 1100W
Switching Frequency, f_S : 100 kHz

Selecting the inductor value: The inductor value determines the amount of switching frequency ripple that rides upon the line current sine wave. One consideration is input noise, the other is peak current through the transistor switch and rectifier. With average CMC, discontinuous operation and minimum loads are not a concern. Peak current is worst case at low line (80Vrms, 113Vpk) and full power (1000W). The max. peak 60Hz current is:

$$I_{60pk} = \frac{P_{OL}\sqrt{2}}{V_{INmin}} = \frac{1000\sqrt{2}}{80} = 17.7\text{A} \quad (1)$$

The overload peak 60 Hz current limit should be set at 18A.

The inductance value determines the 100kHz ripple. Half the peak-peak ripple is added to the peak 60 Hz current. The amount tolerable depends on how comfortable the switch and rectifier will be at the higher instantaneous peak current levels. 4A pp ripple will increase the max. peak 100kHz current to 20A, while 8A pp will take the peak current to 22A. The inductance can then be calculated at the peak low line input voltage:

$$D = \frac{V_O - V_{IN}}{V_O} = \frac{380 - 113}{380}$$

$$L = \frac{V_{IN} D}{\Delta I \, f_S} = \frac{113 \times 0.7}{4 \times 100K} = 0.198\,\text{mH} \quad (2)$$

Allowing a ripple current of 8A pp would reduce L to .099 mH.

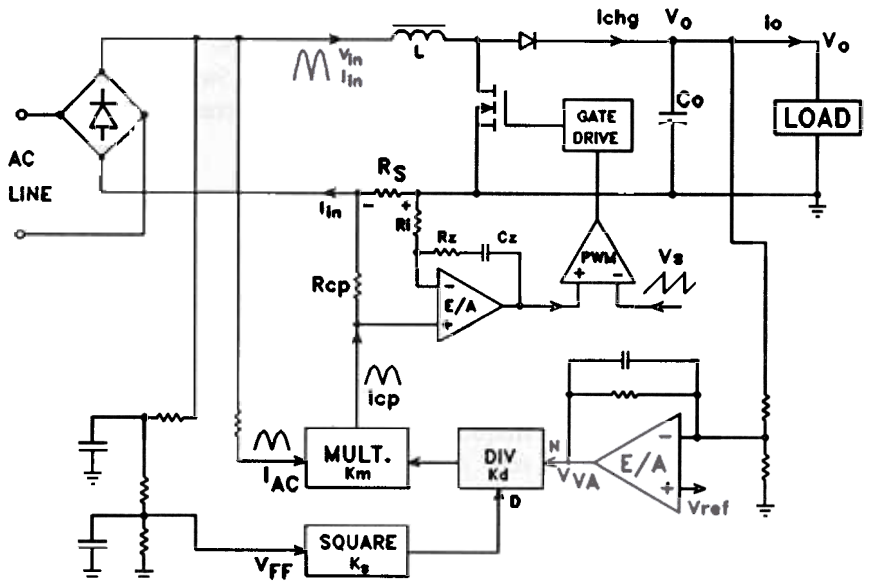

Fig. 5 - Boost Regulator Circuit

Selecting the Bulk Energy Storage Capacitor Value: The output bulk filter capacitor C_O is essentially a 60 Hz filter and energy storage component (although it does filter 100kHz current as well). C_O stabilizes the output bus by storing the excess of energy provided by the line near the sine wave peaks, then providing this energy to the output when the energy available from the line is low, near zero crossing. The waveforms in Fig. 6 show the manner in which power is processed through the preregulator. NOTE: The following discussion applies to *any* properly functioning and efficient high power factor preregulator, regardless of its topology or method of current programming.

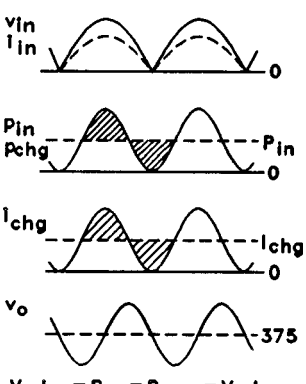

Fig. 6 - HPF Waveforms

Assuming the power factor is reasonably high, the input voltage and current waveforms are in-phase sine waves. The input power is the product of these waveforms which is a $\sin^2$ function at line frequency, equivalent to (1-cos) at twice line frequency.

With high efficiency, preregulator power input equals power output to the bulk capacitor, p_{CHG}. Because V_O is essentially a DC voltage, the current waveform i_{CHG} out of the preregulator has the same shape as the power waveform, with a frequency twice the line frequency. The amplitude of the AC component of the current waveform is equal to the DC component:

$$I_{CHGpk} = P_{INavg}/V_O \qquad (3)$$

With an average power of 1kW and a 380V output bus, the DC and peak 120Hz AC charging current is 2.63A. The ripple voltage v_O across C_O is:

$$v_{Opk} = I_{CHGpk}/X_C \qquad (4)$$

In practice, the bulk filter capacitance value is often determined by the holdup requirements of the supply, not by ripple voltage considerations. This means that starting from an initial bus voltage, V_O, the capacitor must store enough energy to maintain the output above a specified minimum voltage, V_{MIN}, after the line voltage has been absent for a specified number of milliseconds, often one or two full cycles at the line frequency.

$$P_O t_H = \frac{1}{2} C_O V_O^2 - \frac{1}{2} C_O V_{MIN}^2$$

$$C_O = \frac{2P_O t_H}{V_O^2 - V_{MIN}^2} \quad (6)$$

For example, at a nominal V_O of 380V, a capacitance of 2μF/Watt will reach 353V after 20 msec, or 323V after 40 msec.

With 2μF/Watt and 380V bus, Eqs. (3) and (4) indicate an output ripple voltage v_O of 3.5Vpp (1.74Vpk). The larger the capacitance, the easier it is to achieve low distortion. With 2μF/Watt and V_O = 380V, it is not difficult to achieve 3% harmonic distortion with excellent dynamic behavior using the design approach discussed herein.

The Current Sense Resistor:

There is a great deal of flexibility in setting the value of current sense resistor R_S. If .05Ω is used to directly sense input current as shown in Fig. 5, the max peak 60 Hz current of 18A corresponds to 0.9Vpk across R_s. Power dissipation at full load, low line is 7.8W. If R_S is reduced to .01Ω, 18A peak 60 Hz equates to 0.18 volts across R_S with 1.6W dissipation. At this level, noise problems may be more severe and 4-terminal Kelvin connections may be desirable. 1 or 2% resistor accuracy is desirable throughout the current control system, otherwise tolerances may conspire to clip the current waveform at low line and full power.

For a 1kW preregulator, the best approach is probably to use current transformers (CTs) to sense the input current–see Ref [1]. In a boost preregulator, a single CT cannot be used to directly sense input (inductor) current because the DC value is lost through the CT. As discussed in [1], two CTs must be used–one senses switch current, the other senses rectifier current. The CTs reset while these discontinuous waveforms are at zero, so that the average value is retained on the secondary side. These two waveforms are applied through diodes to a common sense resistor, thereby reconstituting the input current including its average value. For example, with 200:1 turns ratio CTs (Pulse Engineering #51688 current sense inductor) a 10Ω sense resistor provides the same 0.9V with 18A max peak 60 Hz line current as the direct .05Ω current sense resistor, but the power dissipation in R_S is only 39mW. Overall preregulator efficiency is improved by almost 1%!

Setting Up the Multiplier/Divider:

The multiplier/divider must be set up so that overload power limits and independent overload current limits function properly over the entire range of input voltages and do not conflict with each other. The specifics of how to accomplish this depends on the control system used. This discussion will focus on the UC3854 control IC. Refer to Fig. 5, which shows most of the UC3854 circuitry.

The equation governing the UC3854 multiplier/divider/squarer circuits is:

$$i_{CP} = \frac{K_M i_{AC} (V_{VEA} - 1)}{V_{FF}^2} \quad (7)$$

The power input to the preregulator is set by the error amplifier output V_{VEA}. Feedforward causes power input to remain constant at a specific V_{VEA} level regardless of line voltage changes. (Suppose line voltage doubles. I_{AC} doubles, V_{FF}^2 quadruples. i_{CP} and line current are halved, maintaining constant power input.) A very important aspect is: *The divider input in the UC3854 does not function beyond 5.6V. This V_{VEA} value corresponds to the max. overload power limit and must be set up appropriately.* It is convenient to establish 5.0V as the full load V_{VEA} value, with 5.6V for the overload power limit.

The overload power limit governs when the line voltage is in the normal operating range causing the effective current limit to vary inversely with line voltage. But with line undervoltage, or during startup or following line voltage dropout, an independent current limit is necessary. This independent peak 60Hz limit should be set at the peak 60Hz current level corresponding to full power at low line. This independent current limit is set in the UC3854 by resistor R_{SET} (not shown in Fig. 5).

Another rule that must be observed with the UC3854 is that i_{CP} cannot exceed twice i_{AC}.

There is a minimum value of V_{FF} that will satisfy this requirement at full power (V_{VEA}=5.0V). Solving Eq (7) for V_{FF} with i_{CP} set at twice i_{AC} and V_{VEA}=5V:

$$\min V_{FF} = \sqrt{\frac{K_M i_{AC}(V_{VEA}-1)}{i_{CP}}} \quad (8)$$

$$= \frac{\sqrt{1(5-1)}}{2} = 1.414\,V$$

The procedure for setting up the UC3854 multiplier is:

1. Determine the feedforward divider ratio that provides a little more than min. V_{FF} (1.414V). at low line voltage (0.9 is DC to rms form factor of rectified sine wave):

$$\max Div.\ Ratio = 0.9\times 80V/1.414 = 51{:}1$$

Referring to Fig. 5, in this example the three resistors in the divider are: 820K at the top, then 75K, with 20K at the bottom of the divider string. The divider ratio is 45.75. V_{FF} is 1.57V at 80v rms input, rising to 5.3V at 270V input.

2. The definition of i_{AC} is somewhat arbitrary. A 680K resistor from the rectified line will dissipate only 0.1W at high line. Peak i_{AC} at low line is 80•1.414/620K = .182mA pk.

3. Using values of V_{FF} and peak i_{AC} at low line, and V_{VEA}=5V at full power, use Eq. (7) to calculate the max peak current programming signal, i_{CP}:

$$\max i_{CPpk} = \frac{1 \bullet .182(5-1)}{1.57^2} = 0.295\,mA \quad (9)$$

4. Finally, set the independent i_{CP} current limit to the same value found in (9):

$$R_{SET} = 3.75V/i_{CP} = 3.75/.295 = 12.7\,K \quad (10)$$

Designing the Average Current Mode Control Loop:

The maximum peak current programming value i_{CP} at full power and low line from Eq.(9) must now be equated to the actual peak 60 Hz current under these same conditions I_{60pk} from Eq.(1) -- 17.7A:

$$i_{CP}R_{CP} = I_{60pk}R_S/n \quad (11)$$

where n is the CT turns ratio, if used. Solving for R_{CP} and using the values previously established:

$$R_{CP} = \frac{17.7\,A \bullet 10\Omega/200}{0.295} = 3\,K \quad (12)$$

See Ref. [1] for the details on designing the current loop.

Once the average CMC loop is closed around the buck and flyback topologies, their characteristics appear identical to the outer voltage loop. Except for the design of the power stage, the techniques presented here apply to all topologies using average CMC.

Designing the Voltage Control Loop:

As mentioned earlier, the bulk filter capacitor size has a significant effect on the trade-off between low input harmonic distortion and acceptable excursions of the output bus voltage with rapid line or load changes. Halving C_O will double output ripple voltage and double control to output gain. If the EA gain is halved, keeping the same pole frequency, voltage loop crossover and gain bandwidth will be the same as before. Input power factor will be the same. *However* -- output bus ripple will be doubled, and output voltage transient excursions are doubled in amplitude -- perhaps to an unacceptable level. This occurs even though the overall gain-bandwidth is the same, because gain has been "relocated" -- the power circuit gain has been increased but feedback gain is decreased.

If a large C_O value is dictated by a holdup requirement of 1 or 2 line cycles, there is little difficulty achieving 3% distortion with acceptable transient behavior. but if there is no

holdup requirement and the desire is to minimize C_O. some choices have to be made: 1. Keep the same f_C and gain bandwidth but have double the output ripple and transient excursions as above, or 2. Double the EA crossover and gain bandwidth which will reduce the excursions, but the ripple won't change and the harmonic distortion will double.

For this example, C_O of 2000μF (2μF/W) is assumed, providing 20ms holdup 353V min. from 380V.

The design procedure for the voltage control loop is as follows:

1. Calculate output ripple: Combining Equations (3) and (4) and solving for peak 120 Hz ripple across C_O at full power:

$$v_{Opk} = \frac{P_{INavg} X_{Co}}{V_O} \quad (13)$$

$$v_{Opk} = \frac{1000}{2\pi\ 120 \cdot 2000\times10^{-6} \cdot 380} = 1.75\ \text{V}pk$$

or 3.75Vpp.

2. Decide how much input current distortion will be contributed by the feedback path and the related 2nd harmonic ripple on the VEA output. To keep input 3rd harmonic distortion under 3%, the contribution from the feedback voltage will be limited to 0.75%. (Another 1.5% will be contributed by voltage feedforward, leaving a margin of 0.75% for other sources of input distortion.) The 0.75% 3rd harmonic contribution is generated by 1.5% second harmonic distortion on the *VEA* output. This means that the peak 120 Hz ripple on the *VEA* output at full load will be 1.5% of the effective V_{VEA} DC level (5V-1V):

$$v_{VEApk} = \%Ripple \times V_{VEA} = .015(5-1) = .06\ \text{V} \quad (15)$$

3. From the results of steps 1 and 2 above, calculate VEA gain desired at 120 Hz:

$$G_{VEA} = v_{VEApk} / v_{Opk} = .06 / 1.745 = .034 \quad (16)$$

4. Select the VEA input resistor value: Referring to Fig. 7, this is a somewhat arbitrary decision. Op amp bias current will cause errors if R_I is too large, and a small resistor will have high power dissipation. An R_I value of 1 megΩ will dissipate only 0.144 W.

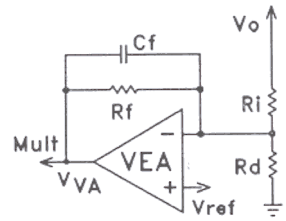

Fig. 7 - Voltage E/A

5. Calculate C_F value: C_F together with R_I determine the VEA gain, which varies inversely with frequency. C_F is calculated to achieve the desired gain at 120 Hz from step 3. *Divider resistor R_D has absolutely no effect on the error amplifier gain at any frequency. The VEA inverting input voltage is constant -- equal to V_{REF} on the non-inverting input -- so there is absolutely no AC current through R_D.*

$$C_F = \frac{1}{2\pi\ 2f_L G_{VEA} R_I} \quad (17)$$

$$C_F = \frac{1}{2\pi\ 120 \cdot .035 \cdot 1\times10^6} = .038\mu F$$

.036μF will be used.

6. Calculate and plot the VEA gain and power circuit gain:

$$G_{VEA} = \frac{v_{VEA}}{v_O} = \frac{-jX_{Cf}}{R_I} = \frac{-j}{2\pi f R_I C_F} \quad (19)$$

$$G_{VEA} = \frac{-j}{\quad\quad 1} = -j4.4/f$$

Power circuit gain includes the multiplier gain. The relationship between P_{IN} and V_{VEA} is linear, so the AC and DC ratio is the same. The following equation applies to *any* topology using average CMC:

$$G_{PWR} = \frac{v_O}{v_{VEA}} = \frac{P_{IN}}{\Delta V_{VEA}} \frac{-jX_{Co}}{V_O} \quad (21)$$

$$G_{PWR} = \frac{1000}{(5-1)} \frac{-j}{2\pi f 2000\times10^{-6}\cdot 380} = -j\,53/f$$

The two gain slopes previously calculated are now plotted in the Bode plot of Fig. 8.

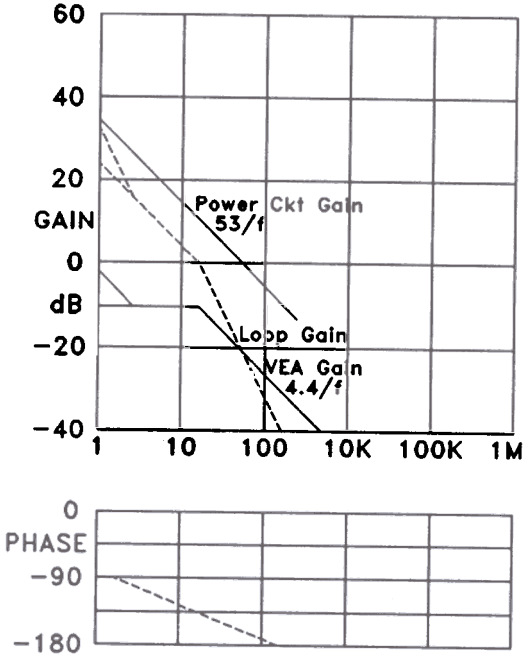

Fig. 8 - Boost Preregulator Bode Plot

The power circuit dB gain and the *VEA* dB gain can be added together on the logarithmic Bode plot to obtain the overall loop gain plot. The overall gain has a −2 slope at the crossover frequency f_C and will be unstable unless a pole is added near f_C. Fig. 8 shows the pole added to the *VEA* gain right at f_C. Below f_C, the VEA gain is flat and the overall loop gain has a -1 slope. This provides a 45° phase margin for optimum loop response.

Calculate the loop gain crossover frequency: The crossover frequency can be determined graphically from the Bode plot, but it is easier in this case to calculate it. Multiply the power circuit and *VEA* gain equations to obtain the overall loop gain, and set the result to zero:

$$G_{PWR}\cdot G_{VEA} = \frac{53}{f}\frac{4.4}{f} = \frac{233}{f^2} = 1 \quad (23)$$

$$f_C = \sqrt{233} = 15.3\ \text{Hz}$$

7. Calculate R_F to put a pole at f_C:

$$R_F = \frac{1}{2\pi f_C \cdot C_F} \quad (25)$$

$$R_F = \frac{1}{2\pi\, 15.3\cdot .036\times10^{-6}} = 290\text{K}$$

8. Calculate the divider resistor value R_D to set V_O at 380V: In the error amplifier circuit as shown in Fig. 7, there is a DC current through R_F that complicates setting up the divider ratio. The alternative is to put a capacitor in series with R_F (not shown) which eliminates the DC error and adds a zero to the *VEA* compensation network. This is not as good as it sounds, in this application. The zero frequency should be at or below 1/6 of the previously established pole frequency, or there will not be enough phase margin at f_C. This requires a capacitor 5 times bigger than C_F (not 6 times bigger). This large capacitor will charge to "wrong" voltage levels when the VEA is overdriven during startup and line voltage dropouts, and this will delay recovery. With the capacitor in series with R_F, although DC load regulation of the output is better, the peak-to-peak plus and minus transient excursions on the output bus when the load increases and decreases suddenly are twice the voltage range that will occur without the series capacitor. Try it!

In the *VEA* circuit as shown, calculate the error offset current through R_F, assuming that V_{VEA} is at 3V, the middle of its 1V-5V normal range:

$$I_{RF} = \frac{7.5V-3V}{R_F} = 15\,\mu\text{A}$$

Calculate the current through R_I:

$$I_{RI} = \frac{380-7.5}{1M} = 372\,\mu A$$

The current through R_D is:

$$I_{RD} = 372-15 = 357\,\mu A$$

Finally, calculate R_D:

$$R_D = \frac{7.5}{357} = 21K$$

It is worth mentioning again that with voltage feedforward applied as with the UC3854, the *VEA* output level programs a specific input power level, regardless of V_{IN}. As V_{EA} increases, power input increases until 5.6V is reached–the UC3854 multiplier/divider input functional limit. This V_{IN} should be set to correspond to the overload power limit. During startup or immediately after a line dropout, the feedforward voltage V_{FF} delay would cause excessive power demand, so it is necessary to have an independent 60Hz peak current limit. This is established in the UC1854 with resistor R_{SET}. The UC1854 also provides an instantaneous peak current limit.

In the UC1854, the VEA output is limited to +16V, which means that under startup or line dropout conditions, V_{VEA} will proceed well past the 5.6V power limit level. The feedback capacitor C_F will charge to this level, delaying subsequent recovery. It is a good idea to clamp the *VEA* output (VAOUT, Pin 7), through a diode to the 7.5V reference to prevent this.

Designing the Feedforward Circuit:

The voltage divider for the feedforward network was defined in Step 1 of the multiplier/divider setup procedure. The resistor values are shown in Fig. 9.

The % 2nd harmonic present in a full wave rectified waveform is 66.2% of the DC average value. With no capacitors in the feedforward network, the % 2nd harmonic on V_{FF} is exactly the same, If it is desired that the feedforward circuit contribute only 1.5% 3rd harmonic distortion to the input waveform (leaving room for other sources of distortion), then the % 2nd harmonic on V_{FF} must be reduced to 1.5%. The attenuation factor is therefore 1.5%/66.2% or .0226. Although not recommended, a single pole may be used to achieve this reduction by placing a single 3μF capacitor across the 20K divider resistor. The resulting pole frequency of 2.7 Hz results in an attenuation factor of 2.7/120 = .0225 to achieve the desired result. But the feedforward transient response is slowed so much that unacceptable dynamic behavior results. The desired 2nd harmonic attenuation can be obtained with acceptable transient behavior by using two cascaded poles instead of one. Each of the cascaded poles should provide an attenuation factor equal to the square root of .0226, or an attenuation factor of 0.15. The required pole frequencies are 0.15•120 Hz, or 18 Hz. This is achieved using 0.5μF and 0.1μF capacitors as shown in Fig. 9. Refer back to Fig. 4 to see the improvement in feedforward response that results. Fig. 10 shows the excellent transient behavior achieved with this fast feedforward network. The line voltage was changed instantaneously from 180V rms to 270V and back again -- the entire min to max range of a 220V line.

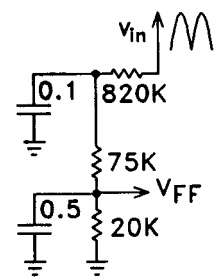

Fig. 9 Feedforward

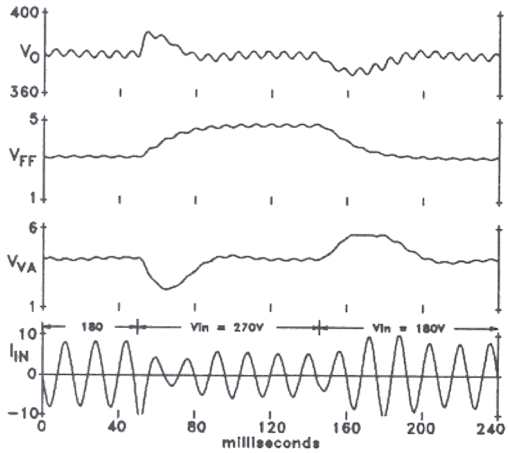

Fig. 10 - Line Regulation Waveforms

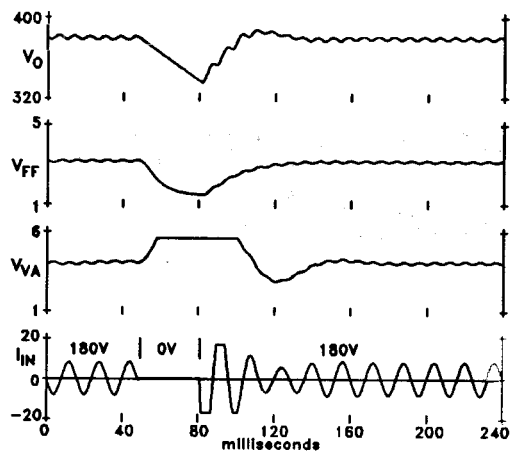

Fig. 11 - 32 millisecond Line Dropout

Line Voltage Dropouts: Fig. 11 shows that the UC3854 is quick and effective in regaining control after a line voltage dropout of 32 msec–two complete line cycles at 60 Hz. The circuit is operating at 1000W full load with 180V rms input before the dropout occurs at 48 msec on the time scale. The linear drop in output voltage is unavoidable–the output capacitor discharges into the 1000W load with no replenishment possible. Feedforward voltage V_{FF} diminishes, and the voltage error amplifier output V_{VEA} reaches the maximum multiplier input voltage, calling vainly for maximum power.

When the line voltage reappears at 80 msec, with V_{VEA} high the multiplier calls for full power. But V_{FF} cannot rise instantaneously, so the multiplier is mislead into calling for high current, restricted only by the 18A peak current limit. High power recharges the capacitor in a few half cycles, with a few volts of overshoot in V_O because of the slight delay in V_{VEA}.

The feedforward network will recover more rapidly after a line voltage dropout if V_{FF} is prevented from dropping all the way to zero. This may be accomplished by clamping the juncture of the 820K and 75K resistors to the 7.5V reference. V_{FF} will be supported at 1.47V, below the normal minimum of 1.57V.

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