



Design Note

Unitrode - UC3854A/B and UC3855A/B Provide Power Limiting With Sinusoidal Input Current for PFC Front Ends

by Laszlo Balogh

This design note focuses on one of the major improvements introduced to the industry standard UC3854 high power factor boost controller. The new UC3854A/B versions eliminated the need for external components to clamp the voltage and current error amplifier outputs and optimized the voltage levels of some of the sense circuitry. All of these issues are already covered by DN-39 design note (present release is version E). The following aspects were expressed implicitly, in previous literature, and are now described in further details.

What makes intelligent power limiting possible with the UC3854A/B and with the newer UC3855A/B ZVS high power factor controllers, is that the maximum value of the multiplier output current is not directly related to the current of the RSET resistor any more.

Instead, it is limited to be equal or smaller than twice the instantaneous value of the IAC current. This new feature provides a very delicate and effective way to limit input power to the power factor corrector front-end while the converter still maintains a sinusoidal input current waveform. It has to be emphasized here that the power limiting scheme of the UC3854A/B does produce sinusoidal input current waveform even if the load is a negative impedance, like DC-DC converters. In these cases, special care has to be taken to guarantee that the output voltage of the boost power factor corrector is greater than the peak value of the input line voltage at all operating equilibrium. This can be insured by setting the power limiting of the DC-DC converter below the maximum power handling capability of the PFC stage.

In order to establish a straightforward design procedure for the multiplier setup, first a basic relationship should be shown. The ratio of the multiplier output current, (IMO) and the IAC current is constant within one cycle of the AC input because:

IAC(t) = (VRMS * sqrt(2) * sin(omega * t)) / RAC (1)

and

IMO(t) = (IAC(t) * (VEA - 1.5)) / (K * (A * VRMS)^2) (2)

where,

VRMS is the RMS value of the AC input voltage;

VEA is the voltage error amplifier saturation voltage (VOH);

K is the multiplier constant (K = 1);

A is the divider ratio to the VRMS pin of the IC.

The ratio of IMO(t) to IAC(t) is given as:

R = (IMO(t) / IAC(t)) = (VEA - 1.5) / (K * (A * VRMS)^2) (3)

which is determined only by the RMS value of the input voltage and stays constant within one line cycle.

In the case of a well executed design, the ratio will be equal to two - right at the minimum input voltage where the rated output power is still expected to be delivered. Figure 1 shows the optimal ratio of IMO and IAC as a function of the normalized input voltage. The horizontal axis of

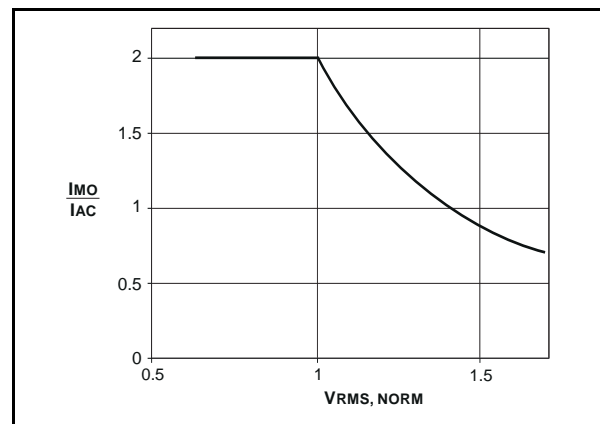


Figure 1. Ideal IMO/IAC Ratio

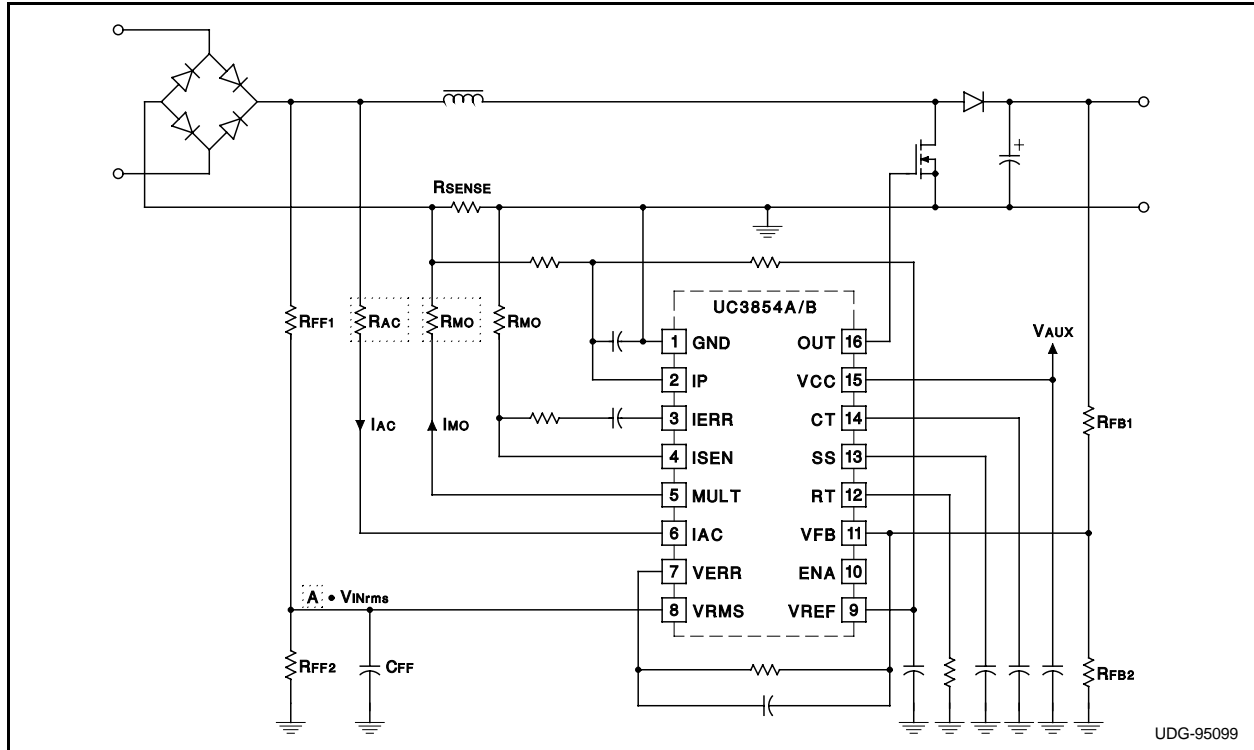


Figure 2. Multiplier Set Up Components in a Typical PFC Application

the graph is normalized for the minimum line voltage where full power can be obtained. For values below unity the converter will work in power limited mode.

To achieve precise power limiting the highlighted components of Figure 2 have to be calculated.

1. From the maximum peak input voltage and the highest allowable IAC value calculate RAC.

$$RAC = \frac{VRMSmax \cdot \sqrt{2}}{IACmax} \quad (4)$$

where $IACmax \leq 600\mu A$ is given in the datasheet.

2. The factor "A" of equation (2) can be determined from the specified minimum input voltage value where the circuit has to supply full rated power. At that point, the voltage error amplifier output (VEA) is about to saturate, and IMO shall be at its theoretical maximum which is $2 \cdot IACmax$. The required value of "A" can be expressed from (3) using the conditions previously stated:

$$A = \frac{\sqrt{2.25}}{VRMSmin} \quad (5)$$

Now every parameter is given for equation (2), and IMO is known for all operating conditions.

3. The next step is to calculate the peak value of the multiplier current ($IMOmax$) at the minimum input voltage ($VRMSmin$). From combining (2), (4) and (5),

$$IMOmax = \frac{VRMSmin \cdot \sqrt{2} \cdot (VEA - 1.5)}{K \cdot RAC \cdot 2.25} \quad (6)$$

4. $IMOmax$ will define the maximum value of the input current ($IINpeak$) which occurs at the peak of the minimum line voltage, ($VRMSmin$) and at maximum load. The required peak input current is given as:

$$IINpeak = \frac{PLIMIT}{VRMSmin \cdot \eta} \cdot \sqrt{2} \quad (7)$$

The relation between $IMOmax$ and $IINpeak$ is defined by the two resistors $RSENSE$ and RMO according to:

$$I_{INpeak} = I_{MOMax} \cdot \frac{R_{MO}}{R_{SENSE}} \quad (8)$$

5. The last parameter to be calculated is the value of R_{MO} from equations (6), (7) and (8), assuming that R_{SENSE} is already selected based on the allowed power dissipation of that resistor.

$$R_{MO} = \frac{2.25 \cdot K \cdot P_{LIMIT} \cdot R_{AC} \cdot R_{SENSE}}{V_{RMSmin}^2 \cdot \eta \cdot (VEA - 1.5)} \quad (9)$$

After all design parameters are defined, the normalized input RMS current values and the normalized input power can be calculated as the functions of the normalized input voltage.

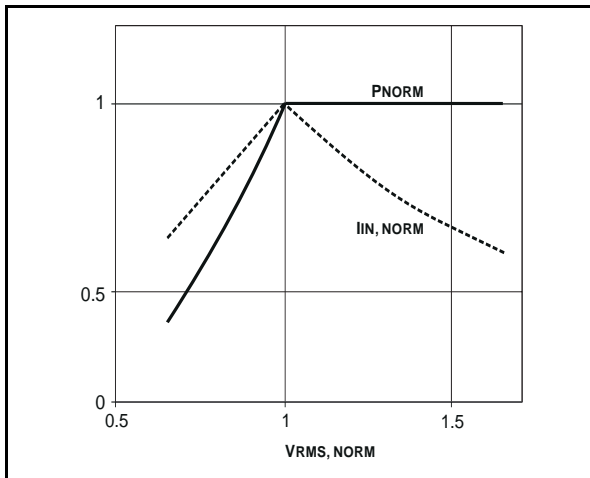


Figure 3. Power Limit and Maximum Input Current Values as a Function of Input Voltage (All Normalized)

As Figure 3 demonstrates, exact, and constant power limiting can be realized by the UC3854A/B high power factor controller ICs for the entire input voltage range. That is caused by the input voltage feedforward term in the multiplier equation, (2).

Design Example

The following example is to illustrate how to execute the procedure described above. The design example has the following start up parameters:

- $V_{IN} = 70 \dots 132 \text{ VACRMS}$
- $V_{INmin} = 90 \text{ VACRMS}$ (where full output power still obtainable)
- $P_{OUT} = 250W$ (power limit of the load converter)
- $P_{LIMIT} = 275W$ (set PFC power limit 10% above load converter)
- $\eta = 0.95$ (expected efficiency)

For optimum results follow the step-by-step design guide given below:

Step 1.

$$R_{AC} = \frac{132 \cdot \sqrt{2}}{600 \cdot 10^{-6}} = 311.1 \cdot 10^3$$

$R_{AC} = 330k\Omega$

Step 2.

$$A = \frac{\sqrt{2.25}}{90} = 0.01667$$

$A = 16.67mV/VRMS$

Step 3.

$$I_{MOMax} = \frac{90 \cdot \sqrt{2} \cdot (6 - 1.5)}{1 \cdot 330 \cdot 10^3 \cdot 2.25} = 771.4 \cdot 10^{-6}$$

$I_{MOMax} = 771.4\mu A$

Step 4.

$$I_{INpeak} = \frac{275}{90 \cdot 0.95} \cdot \sqrt{2} = 4.55$$

$I_{INpeak} = 4.55A$

Step 5.

Assume the maximum power dissipation of the current sense resistor $PR_S = 0.5W$, then:

$$R_{SENSE} = \frac{PR_S \cdot V_{INmin}^2 \cdot \eta^2}{P_{OUT}^2} \quad (10)$$

$$R_{SENSE} = \frac{0.5 \cdot 90^2 \cdot 0.95^2}{275^2} = 0.04833$$

$R_{SENSE} = 47m\Omega$

Step 6.

$$R_{MO} = \frac{2.25 \cdot 1 \cdot 275 \cdot 330 \cdot 10^3 \cdot 47 \cdot 10^{-3}}{90^2 \cdot 0.95 \cdot (6 - 1.5)}$$

$$= 277.1$$

$R_{MO} = 270\Omega$

The design just completed will exhibit the required power limiting characteristics for the entire operating input voltage range. The described calculations can be easily programmed as it is shown in the Mathcad® worksheet in the Appendix.

APPENDIX

This MathCAD file calculates the power limiting characteristic of the UC3854A/B and UC3855A/B high power factor controllers for wide input voltage range application.

INPUT PARAMETERS:

| | |
|----------------------------------|---|
| $V_{INmin} := 70$ | Input voltage (RMS) value, where the controller starts operating. |
| $V_{INlim} := 90$ | Minimum input voltage (RMS) where the circuit must deliver its rated output power. |
| $V_{INmax} := 270$ | Maximum input voltage (RMS). |
| $PLIM := 275$ | 110% of the load power requirements. |
| $\eta := 0.93$ | Expected efficiency of the PFC stage. |
| $IAC_{max} := 600 \cdot 10^{-6}$ | Maximum value of the IAC current as defined in the datasheet. |
| $VEAsat := 6$ | Output voltage of the voltage amplifier when it is saturated high. |
| $K := 1$ | The multiplier constant as it is given in the datasheet. |
| $Rs := 0.047$ | The current sense resistor value, defined previously based on the acceptable maximum power dissipation. |

DESIGN PROCEDURE:

Step 1. Estimate RAC resistance:

$$RAC_{est} = \frac{V_{INmax} \cdot \sqrt{2}}{IAC_{max}} \quad RAC_{est} = 6.364 \cdot 10^5$$

Pick the closest **higher** standard value:

$$RAC := 6.8 \cdot 10^5$$

Step 2. Divider ratio of the input RMS voltage to the VRMS pin (8) of the IC.

$$A := \frac{\sqrt{2.25}}{V_{INlim}} \quad A = 0.017 \quad [mV/VRMS]$$

Step 3. Determine the maximum multiplier output current. It occurs at the peak of the mains cycle at the minimum input voltage amplitude where full rated power is still obtainable.

$$I_{MOmaxpk} := \frac{V_{INlim} \cdot \sqrt{2} \cdot (VEAsat - 1.5)}{K \cdot RAC \cdot 2.25}$$

$$I_{MOmaxpk} = 3.744 \cdot 10^{-4}$$

Step 4. Calculate the highest peak input current value as defined by the rated output power and the minimum input voltage amplitude where full rated power is still obtainable.

$$I_{INpk} := \frac{P_{lim} \cdot \sqrt{2}}{V_{INlim} \cdot \eta} \quad I_{INpk} = 4.646$$

Step 5. Estimate RMO resistance.

$$RMO_{est} := \frac{I_{INpk}}{I_{MOmaxpk}} \cdot Rs \quad RMO_{est} = 583.367$$

Pick the closest **lower** standard value:

$$RMO := 560$$

DESIGN VERIFICATION:

Step := 20 Number of points to calculate.

i := 0..step Step variable.

Input voltage range definition:

$$V_{INRMS}(i) := V_{INmin} + \frac{V_{INmax} - V_{INmin}}{\text{step}} \cdot i$$

IAC current as a function of the input voltage:

$$IAC_{RMS}(i) := \frac{V_{INRMS}(i)}{RAC}$$

IMO current as defined by the input voltage and applying the $IMO < 2 \cdot IAC$ limit.

$$I_{MORMSest}(i) := \frac{IAC_{RMS}(i) \cdot (VEAsat - 1.5)}{K \cdot (A \cdot V_{INRMS}(i))^2}$$

$$I_{MORMS}(i) := \text{if}(I_{MORMSest}(i) > 2 \cdot I_{ACRMS}(i), \\ 2 \cdot I_{ACRMS}(i), I_{MORMSest}(i))$$

Calculating the maximum input RMS current level limited by the multiplier output current.

Graphical representation of the obtained data:

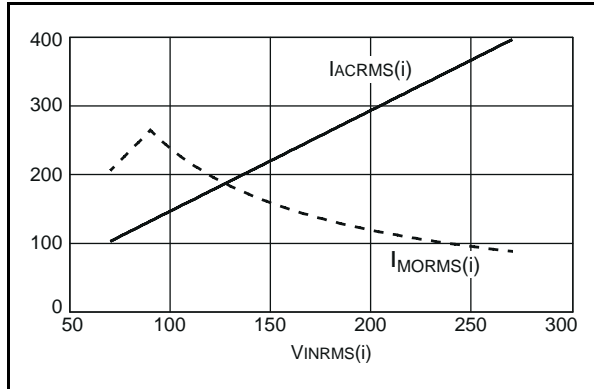


Figure 4. The IAC and IMO currents (in μAmps) as a function of the RMS input voltage.

$$I_{INRMS}(i) := I_{MORMS}(i) \cdot \frac{R_{MO}}{R_s}$$

The power limit of the power factor corrector.

$$P_{INmax}(i) := V_{INRMS}(i) \cdot I_{INRMS}(i)$$

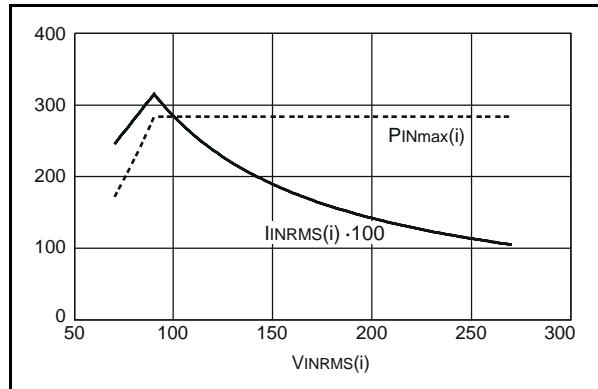


Figure 5. Input power [W] and input RMS current [A] (multiplied by 100 to fit the same scale) as a function of input RMS voltage.

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