Announcement

4th international conference on
thermal & mechanical simulation and experiments
in micro-electronics and micro-systems

EuroSIME 2003

www.eurosime.com
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March 30 – April 2, 2003

Centre de Congrès d'Aix
Aix-en-Provence, France

EuroSimE 2003 provides …

……. 6 courses given by professionals
……. 80 papers in 16 oral sessions
……. exhibition and exhibitor presentations

Conference overview

EuroSIME 2003

Sunday	March 30, 2003	Short courses
8.30 – 9.00	Registration for short courses	
9.00 – 12.30	Course **1** (half day)	**Moisture related reliability issues in electronic packages** by Xuejun Fan (Philips Research lab, USA)
13.30 – 17.00	Course **2** (half day)	**Introduction to IC process reliability** by Andreas Maryin (Infineon Technologies, Germany)
13.30 – 17.00	Course **3** (half day)	**Recent challenges for experimental and theoretical reliability assessment: fatigue of lead-free solder joints, fracture and interface fracture in packaging solutions** by Rainer Dudek (Fraunhofer IZM, Germany)
9.00 – 17.00	Course **4** (full day)	**Experimental characterisation of electronic components and system thermal performance** by Peter Rodgers (Electronic Thermal Management, Ireland)
9.00 – 12.30	Course **5** (half day)	**Coupled-field predictive simulation for virtual test and characterisation of Microsystems** by Gerhard Wachutka
13.30 – 17.00	Course **6** (half day)	**Advanced packaging** by H. Anthony Chan

Monday	March 31, 2003	Conference program, day 1
7.30 – 8.30	Registration	
8.30 – 10.30	Session 1: Trends in Microelectronics & Microsystems	
11.10 – 13.10	Session 2: State of the Art in Thermal and Mechanical Simulations	
12.40 – 14.20	Lunch	
14.20 – 15.50	Session 3: Adhesives, Encapsulation, and Underfill	
14.20 – 15.50	Session 4: Thermal Behavior Modeling	
16.30 – 18.00	Session 5: Reliability of Solder Interconnection	
16.30 – 18.00	Session 6: Thermal & Mechanical Problems in Advanced Packaging	
20.00 – …	Gala dinner	

Tuesday	April 1, 2003	Conference program, day 2
8.30 – 10.00	Session 7: Advanced Packaging and MEMS Designing	
8.30 – 10.00	Session 8: Thermal Modeling	
10.30 – 12.40	Session 9: Designing for Endurance and Reliability	
10.30 – 12.40	Session 10: Thermal Performance	
12.40 – 14.10	Lunch	
14.10 – 16.20	Session 11: MEMS, Sensors and Actuators	
14.10 – 16.20	Session 12: IC Process Reliability Modeling and Characterization	
16.50 – 18.10	Special exhibitor session	
18.10 – …	Cocktail party	

Wednesday	April 2, 2003	Conference program, day 3
8.30 – 10.00	Session 13: Characterization and Modeling of Materials and Reliability	
10.40 – 12.30	Session 14: Simulation and Optimization in Microelectronics	
10.40 – 12.30	Session 15: Designing towards Environmental Demands	
12.30 – 14.00	Lunch	
14.00 – 16.00	Session 16: New Techniques in Modeling and Characterization	
16.00	Closure	

Sunday March 30, 2002: Short courses

Place and date : Centre Congrès d'Aix, Aix-en-Provence (same place as for conference).

Agenda:

8.30 – 9.00	**Registration**				
9.00 – 12.30	**Morning session**	**Course 1**	**Course 2**	**Course 4**	
12.30 – 14.00	**Lunch**				
14.30 – 17.00	**Afternoon session**	**Course 1 (continued)**	**Course 3**	**Course 5**	**Course 6**

Course 1: Moisture related reliability issues in electronic packages

Xuejun Fan, Ph.D, Philips Research lab, USA.

Summary:

The realization of virtual prototyping depends on the capability and reliability of multi-physics modeling. This course focuses on the methods and solutions in multi-physics modeling, including the moisture diffusion, hydroswelling, vapor pressure, delamination and fracture modeling. The emphasis will be given to the implementations of these modeling techniques and methods into the commonly used commercial softwares such as ANSYS, ABAQUS and MARC. The course will also cover the material characterizations (diffusion properties, hydroswelling measurement, and the interface toughness characterization at high temperature, etc), and the verifications of the modeling results against experiments. Several case studies including CSP, FC-BGA and QFN packages will be presented to illustrate that the integrated modeling approaches with necessary material characterizations will yield much better understandings in the package development and design.

Course outline

1. Introduction to the reliability of electronic packaging
2. Failure modes and mechanisms
3. Moisture diffusion: modeling, characterization of material properties, and applications
4. Modeling of evolution of vapor pressure during soldering reflow in a whole package
5. Interface delamination and fracture modeling: methodologies (J-integral, stress intensity factors and energy release rate; nodal force method, virtual crack extension method, etc), and applications
6. Interface characterization: factors affecting interface adhesion, and measurement
7. Case studies: integrated modeling approach in designing CSP, FC-BGA and QFN packages
8. Summary and future trends

Instructor: Xuejun Fan received his Ph.D. degree in mechanical engineering from Tsinghua University, Beijing, China in December 1989. He is currently a Senior Member of Research Staff in Philips Research Lab-USA. He was with the Institute of Microelectronics (IME), Singapore as a Member, Technical Staff from September 1997 to September 2000. He was invited to give keynote lectures at 1st and 3rd EuroSime on moisture related reliability issues in electronic packaging, and is the technical committee member of Eurosime conference.

Course 2: Introduction to IC process reliability

Andreas Martin, Infineon Technologies AG, Germany

Course Description

Integrated circuits must meet customers requirements, for example 15 years lifetime at 125°C and a maximum allowed failure rate of 100 parts per million (ppm). Subsequently, the process line must achieve those specified targets. Highly accelerated reliability stresses are performed to assure the customer the required quality. The reliability is strongly dependent on process materials, device layout, process steps and treatments. First, at the implementation stage any process is qualified on test chips for the customer reliability target. Second, the stability of the reliability of the process line during high volume manufacturing is a key aspect for complex digital and analog integrated circuits and is therefore, monitored on scribe line test structures of product wafers.

Objectives

The goal of this half-day course is to give an overview of state-of-the-art process reliability issues such as, accelerated stress measurements, (self-heating) test structures, physical/predictive models and related calculations/simulations which are required to assess/achieve the process reliability for the product target. Also the course aims for the introduction of the most relevant reliability diagrams, models and termonologies commonly used in semiconductor industry.

Who should attend?

The course will benefit engineers, scientists and managers who are in the field of processing, process and circuit simulation with the intention to include reliability hazards and any aspect of IC quality, reliability, failure analysis or product target prediction either on side of the IC manufacturer or on the side of the IC vendor.

Course Description

The course is structured in three main parts. After a general introduction briefly reviewing the basic CMOS process the first part will describe the reliability concepts for the verification of the interconect scheme. In the second part the significant dielectric layer reliability topics will be presented. In the third part the CMOS device reliability will be discussed. Finally the course will be concluded. All parts will include a wide span of reliability investigation schemes from testing durations of weeks to test times of seconds.

The first part consists of a detailed introduction to the reliability of an IC interconnect scheme. It will be pointed out that new process technologies encounter different problems due to a radical changes from aluminum to copper for the interconnect material and from SiO2 to low-k-materials as insulation between interconnects. The various degradation modes will be described. The correct design of test structures including thermal and electrical simulations as well as the design of experiment is vital for the verification of a reliability target. Models and reliability plots will be introduced and explained.

In the second part, one of the most significant process step, processing a dielectric layer will be assessed in terms of reliability performance. Dielectric layers are a key feature for CMOS devices used in logic or memory applications as well as for insulation layers in interconnect schemes of any IC. The total area of dielectrics of an IC easily exceeds the total area of the chip. The reliability of those layers is vital for the functionality of the circuit and can be verified in various ways. Different materials and stacks, processing options or structure layout have huge impacts on the reliability performance. Predictive models will be presented and the physical background explained for the understanding of the dielectric layer degradation. Typical graphs and plots will be shown in order to be able to classify any of those dielectric reliability diagrams in the future.

The third part will deal with CMOS device reliability. The functionality of CMOS devices can degrade seriously over time. The key factors of the degradation are the operating conditions, the device geometry and process instabilities. The various degradation causes and the most common device degradation models will be presented. The accelerated stress measurements and significant types of reliability diagrams will be described. Also the temperature stability, its testability and the possibility of circuit simulation will be highlighted.

Course Outline

1. Introduction
2. Interconnect reliability: Introduction to the different interconnect reliability problems, test structure geometries, design of accelerated stress measurements, predictive models, use of simulation tools, process material issues.
3. Dielectric reliability: Introduction to the various dielectric layers in of an IC process, physical background of dielectric degradation, test structure layout, accelerated stress measurements set ups, reliability models for predictivs lifetime estimation.
4. CMOS Device reliability: Overview of degradation mechanisms for different stress applications, physical background, predictive reliability models, realisation of highly accelerated stress conditions.
5. Summary / discussion

Instructor:

Andreas Martin has over ten years of experience in the field of process reliability. After his study of Electronic Engineering in the Technical University of Darmstadt, Germany he has done 6 years of research in predictive dielectric reliability models in the National Microelectronics Research Centre (NMRC) of Cork, Republic of Ireland. He holds a masters degree in Electronic Engineering / Microelectronics. Currently, he is with the central Reliability Methodology department of Infineon Technologies AG in Munich, Germany, where he does development and research work in the field of fast Wafer Level Reliability tests and WLR data analysis in his fifth year for Infineon worldwide for logic and memory technologies. His areas of interests are dielectric stress measurements, plasma induced damage and the design of state-of-the-art test structures for reliability testing.

He has published or co-authored over 30 publications besides a numerous number of Infineon-internal research notes. He is memeber of the IEEE Reliability society. For the last 9 years he has been involved in the Organisation ot the IEEE Integrated Reliability Workshop (IRW) which he has organised as General Chair in 2001. His involvement in the JEDEC subcommittee 14.2 includes the Foundary Qualification Procedure, Dielectric Reliability Testing and Plasma Induced Damage Testing. He is involved in the organisation of the Workshop on Dielectrics in Microelectronics (WoDiM) since 1992. He had hosted WoDiM 2000 as General Chair in Munich. He also coordinates a wafer level reliability subcommittee of the VDE in Germany.

Course 3: Recent Challenges for Experimental and Theoretical Reliability Assessment: Fatigue of Lead-free Solder Joints, Fracture and Interface Fracture in Packaging Applications

Rainer Dudek and Jürgen Auersperg (Fraunhofer IZM, Germany)

Course objectives

The course focuses on thermo-mechanical issues of microelectronics packaging. FE strategies and methodologies are presented, and their theoretical background for the prediction of physical parameters impacting on thermo-mechanical behavior, such as local stresses and strains, is outlined. Detailed insight into the non-linear constitutive description of electronic materials is provided, especially concerning solder materials. For the implementation of lead-free solders in electronic packaging, knowledge of lead-free solder materials is provided concerning mechanical properties, solder joint reliability tests, failure analysis and fatigue life prediction. Additional application examples for the analysis methods presented towards failure prediction of advanced packaging technologies are given, including experimental verification.

Who Should Attend

Design, manufacturing, quality and reliability professionals who are involved in thermo-mechanical issues or reliability of electronic systems, especially those interested in FE-simulations for solder interconnects and packaging solutions for advanced electronic assemblies.

Course content

1. Packaging Related FE-Simulation
   - Typical thermo-mechanics related questions.
   - Theoretical background based on continuum mechanics, failure types and prediction hypothesis.
2. Fracture and Interface Fracture
   - Some remarks on fracture and interface fracture mechanics, materials non-linear constitutive behavior.
   - Simulation and experimental approaches.
   - Example flip chip on board failure, interface stress and delamination
   - Example “Popcorn” failure in plastic packages, remarks on moisture diffusion analysis, fracture mechanical analysis
3. Lead-Free Solder Mechanical Properties, Testing and Modeling
   - Mechanical properties of lead-free solders (SnAg, SnCu, SnAgCu).
   - Fatigue performance of lead-free solders (SnAg, SnCu, SnAgCu). Creep and stress relaxation behavior, bulk versus joint behavior (SnAg, SnAgCu, SnPb).
4. Solder Joint Reliability Tests and Analysis
   - Temperature cycle data on SMT-components, FCOB with and without underfills, CSPs and BGAs for different test conditions and solder alloys types (SnPb, SnAg, SnCu, SnAgCu).
   - Failure mechanisms related to the solder joints of the new alloys, will creep deformation still play a dominant role for e.g. thermally induced low cycle fatigue?
5. Intermetallic Compounds (IMC)
   - Solder-surface finish interactions.
   - Intermetallic growth and metallization consumption.
   - Intermetallics within the solder.
   - Thermo-mechanical properties of the intermetallics.
6. Solder Fatigue Life Prediction by Finite Element Analysis
   - Material constitutive models – implementation of time and temperature dependent behavior of solders (SnPb, SnAg, SnAgCu).
   - Life prediction models – Strain-based relations (accumulated creep strain) or Energy-based relations (average viscoplastic strain energy density dissipated).
   - FEA modeling and simulation of Thermal Shock and Thermal Cycling Tests (SnAg and SnAgCu versus SnPb).
   - Life prediction models – Strain-based relations (accumulated creep strain) or Energy-based relations (average viscoplastic strain energy density dissipated).
   - Comparison between simulation results and experimental results.

About the instructors:

Rainer Dudek received the Ph.D. degree in mechanical engineering from the University of Technology Chemnitz, Germany, in 1986. From 1986 to 1993, he was with the Institute for Mechanics, Department of Fracture and Micromechanics, Chemnitz. He joined the Fraunhofer Institute for Reliability and Microintegration (IZM), Berlin in 1993. He has been working on nonlinear finite element analysis with respect to different advanced material applications since 1980. His current research interests are in the area of design-for-reliability of electronic packages, with emphasis on constitutive modeling and

failure prediction for electronic materials. Dr. Dudek has given many lectures on thermo-mechanical FE-simulation related issues in microsystem packaging at national and international workshops and conferences. He is a member of the conference program committee of the international ESIME conference. He has authored and co-authored many technical publications at international journals and conferences, two of them awarded with “best paper prizes”.
Jürgen Auersperg received his Ph.D. in applied mechanics from the Chemnitz University of Technology, Germany in 1980 . He joined Fraunhofer IZM, Dept. Of Mechanical Reliability and MicroMaterials as a senior scientist in 1996 and is head of the group "Nanomechanics and Micromechatronics". Furthermore, he is responsible for numerical simulations at the AMIC company in Berlin since 1999.His specialties are nonlinear finite element simulation, fracture and damage mechanics, fatigue and failure analysis of microelectronic components.

Course 4: Experimental Characterisation of Electronic Components and System Thermal Performance

Peter Rodgers (Electronics Thermal Management, Ltd., Ireland)

Summary:
To satisfy consumer demands for more compact and sophisticated electronic devices, advances of semiconductor technology have achieved increased Integrated Circuit (IC) functionality and miniaturisation. However, the continuous increase of both switching speed and transistor density, still described by Moore's law, have inadvertently resulted in rising die heat fluxes, which, if not efficiently removed from the device, may impact on product performance and reliability. While no generic relationship exists to relate component and Printed Circuit Board (PCB) temperature with reliability, it has been shown that die circuit performance can be highly sensitive to operating temperature, and therefore temperature must be controlled.
This need, combined with the demand for more reliable electronic systems, has heightened the requirement for accurate characterisation of product thermal performance. Although thermal design practices have evolved to a high reliance on virtual prototyping using numerical predictive techniques, relying solely on numerical predictions without experimental analysis still remains an unreliable design strategy. An efficient thermal design process therefore requires a balanced combination of experimental and numerical efforts, whereby experimentation is used to both provide critical physical boundary conditions for numerical analysis and verify the numerical models. Ultimately, experimental characterisation is necessary to assess the effectiveness of the cooling design both at system level and locally at critical component locations, from which component reliability, hence product life, can be estimated.
This course covers the fundamentals of thermofluid measurements to characterise electronics thermal performance, from component to system level. The principles and application of experimental techniques to measure the critical physical parameters involved, such as temperature, fluid flow and heat transfer, are reviewed. Specific methods for characterising important system elements, such as IC packages, populated boards, racks, heat sinks, fans, and grilles/vents are outlined. Electronics thermal characterisation standards, and both standard and non-standard characterisation environments are reviewed. Practical case studies dealing with the thermal characterisation of telecommunication products are presented.

Course objectives
This course provides experimental strategies and methodologies to characterise electronic system thermal performance, from component to system level. The application of these techniques will permit the thermofluid phenomena in a given application to be understood, will guide the thermal design process and ultimately permit product thermal performance to be qualified.

Who should attend?
The course will benefit engineers, managers and scientists involved in the thermal management, thermo-mechanical issues or reliability of electronic systems. It is aimed at participants with varying expertise levels in thermal management, from novice to advanced.

Course outline

1. The need for experimentation
   - Characterisation of electronics thermal performance for reliability
   - Supporting analysis for numerical modelling
     - § Physical boundary conditions
     - § Numerical model validation
   - Physical measurement parameters
     - § Primary: temperature, velocity, flow rate, pressure, heat transfer
     - § Secondary: humidity, acoustic noise, material thermal conductivity
   - Uncertainty analysis
     - § Estimating measurement uncertainty
     - § Mathematical analysis
     - § Single sample uncertainty analysis

- Reporting uncertainties

2. Measurement Techniques
   - Temperature measurement
     - Thermocouples
     - Thermistors
     - Resistance thermometry
     - Radiation thermometry
     - Liquid crystal thermometry
     - Interferometry
   - Velocity measurement
     - Pressure-based techniques
     - Hot Wire Anemometry (HWA)
     - Laser Doppler Anemometry (LDA)
     - Particle Image Velocimetry (PIV)
   - Flow rate measurement
     - Rotameter
     - Orifice plate
     - Laminar flow element
     - Vortex eddy flow meter
     - Thermal mass flow meter
   - Pressure measurement
     - Static and dynamic pressure measurement
     - Differential pressure methods (manometers)
     - Pitot-static probe design
     - Pressure tap design
   - Heat transfer
     - Heat flux gauges (thermopiles)
   - Humidity
     - Gravimetric procedure
     - Dry and wet bulb thermometer
     - Electrical transducer
   - Acoustic noise emission (air movement)
     - Sound pressure level
     - Sound power level
   - Material thermal conductivity and diffusivity measurement
     - Long bar method
     - Three-omega method
     - Flash method
3. Thermal characterisation environments
   - Wind tunnel design
     - Standard design: SEMI G38-0996, EIA/JEDEC JESD51-6
     - Customised design: design principles, aerodynamic design, flow management elements
   - Fan characterisation unit
     - International standards: BS 848, ANSI/AMCA 210-85, ANSI/ASCHRAE 51-1985
   - Enclosures
     - Temperature-controlled ovens, still-air enclosures
4. Component thermal characterisation
   - International standards for junction-to reference thermal resistance measurement
     - EIA/JEDEC, SEMI, MIL, DELPHI
   - Component junction temperature measurement
     - Direct methods: electrical techniques - thermal test chips, switching method
     - Indirect methods: infrared thermography, liquid crystals
     - Figures-of-merit calculation: junction-to-reference thermal resistance (applicability/limitations)
5. Unit level characterisation
   - Heat sink thermal characterisation
   - Fan performance testing
   - Grilles, vents: pressure loss coefficient measurement

- Flow visualisation
  - § Airflow visualisation
  - § Smoke entrainment: smoke-wire, smoke-tube methods
  - § Liquid flow visualisation
  - § Dimensional analysis and similitude
  - § Dye entrainment (ink streaks)
  - § Surface flow visualisation
  - § Paint film techniques: ink-dot and powder-based methods
  - § Mass transfer: sublimation- and evaporation-based methods
  - § Tuft probes

6. System thermofluid characterisation
   - Prototype mock-up design
   - Thermal characterisation procedure
   - System flow impedance measurement
7. Electronics thermal characterisation case studies
   - Multi-component printed circuit board
   - Mobile phone
   - Telecommunication cabinet
8. Summary

About the instructor:

Dr. Peter Rodgers is director of Electronics Thermal Management Ltd., a research and consulting firm specialised in electronics cooling. He holds a Ph.D. degree in mechanical engineering from the University of Limerick, Ireland and has been involved in electronics thermal management for thirteen years. Dr. Rodgers was formerly with the Nokia Research Center, Finland, where he consulted on electronics thermal management within the corporation, and lead a three-year research programme on benchmarking the predictive accuracy of CFD codes dedicated to the thermal analysis of electronic equipment. For publications associated with this work, he was awarded the 1999 Harvey Rosten Award for Excellence. He has an extensive experimental background in electronics cooling, which includes the development of advanced experimental techniques to characterise thermofluid phenomena. In his previous positions, he contributed to the development of state-of-the art thermofluids laboratories both at the University of Limerick, Ireland and the Nokia Research Center. Dr. Rodgers is a member of the EuroSIME, SEMI-THERM and THERMINIC conference programme committees, and has been an invited lecturer, keynote speaker, and panelist to discussions on simulation issues in electronics thermal management at international conferences. He has authored or co-authored over thirty refereed conference and journal publications. He is currently supervising doctoral research on the application of CFD analysis to electronics thermal design, undertaken at Electronics Thermal Management.

Course 5: Coupled-field Predictive Simulation for Virtual Test and Characterization of Microsystems

Gerhard K.M. Wachutka

Course summary:

The course will cover the following topics:

- methodology of coupled-field analysis of microdevices
- extraction of physically-based compact models for system macromodels
- methods of order reduction
- validation and calibration of models and model parameters
- case studies: electro-mechanically coupled microdevice with snap-in instability and/or fluidic damping effects using
- finite network approach

About the instructor:

Gerhard K.M. Wachutka (M'90) received the D.Sc. degree from the Ludwig-Macimilians-Universität, Munich, Germany, in 1985. From 1985 to 1988, he was with Siemens Corporate Research and Development, Munich, where he headed a modelling group active in the development of moderh high-power semiconductor devices. In 1989, he joined the Fritz-Haber-Institue of the Max-Planck Society, Berlin, Germany, where he worked in the field of theoretical solid state physics. From 1990 to 1994, he was head of the microtransducer modelling and characterization group of the Physical Electronics Laboratory at the Swiss Federal Institute of Technology, Zurich. There, he also directed the microtransudecers modelling module of the Swiss Federal Priority Program M2S2 (MicroMechanics on Silicon in Switzerland). Since 1994, he has been heading the Institute for Physics of Electrotechnology, Munich University of Technology, where his research activities are focused on the design, modelling, characterization and diagnosis of the fabrication and operation of semiconductor

microdevices and Microsystems. He has authored and coauthored more than 180 publications in scientific or technical journals. He is a consultant to research institutes in industry and universities. He is a reviewer fro various scientivic journals and other institutions. Among his many educational activities, he has set up and taught courses funded by European Community training programmes such as UETP, EUROFORM and EUROPRACTICE. Prof. Wachutka is a member of the American Electrochemical Society, the American Materials Research Society, the ESD Association, the German Physical Society and AMA Societry for Sensorics.

Course 6: Advanced Packaging

Professor H. Anthony Chan

Course description

The world has been changing faster than ever before in the use of computers, communications and emerging technologies. There has been continuous push of the products for higher performance, higher speed, smaller size, mobile, more ruggedness, more user-friendly, faster to market, and yet lower cost. As the technologies for chip, photoelectronics, photonics, and micrsystems are changing fast while encountering these challenges, the technologies of packaging and system integration must also change fast and face these challenges. The technologies for device packaging and systems integration have been changing rapidly in recent years. The areas are diverse and the required skills are highly interdisciplinary. In terms of packaging products, advanced packaging include microelectronic packaging, optoelectronic packaging, Radio frequencies packaging, and bioelectronics packaging. In terms of packaging technologies, packaging may be at chip scale level, component level, board level, and systems level integration. In terms of size, systems are migrating through microsystems technologies to nanotechnologies. In terms of evolution, systems move from conventional systems, through system on package (SOP), system in package (SIP) and Wafer Level Packaging (WLP), and then to system on chip (SOC). In terms of fundamental science and engineering, they include electrical aspects especially that of radio frequencies (rf), mechanical aspects, thermal aspects, materials science, optoelectronics, photonics, reliability, environmental science, and biotechnology.

This short course covers the fundamentals of the different packaging technologies.

Course outline

1. Trends:
   - Technology Drivers
   - Electronics Technology Trends
   - Packaging Trends
2. Multidisciplinary Design Considerations
   - Electrical considerations
   - Mechanical considerations
   - Thermal considerations
   - Materials science considerations
   - Environmental considerations
   - Robustness considerations
   - Optical considerations
3. Interconncetion Technologies
   - Wire bond
   - Solder bump
   - Ball Grid Array
   - Flip Chip and different types of Flip Chip
4. Packaging
   - Different Ball Grid Array packages
   - Different Flip Chip packages
   - Wafer Level Packaging / Chip Scale Packaging
   - Optoelectronic packaging
   - System in Package

About the instructor:

H. Anthony Chan received PhD from University of Maryland in 1982 and then continued research there in areas of experimental superconductivity and gravitation. He joined the former AT&T Bell Labs in 1986. Since then, his work had spread over different areas of interconnection, electronic packaging, reliability, and assembly in manufacturing, telecommunication network, datanetwork architecture and wireless. He was the AT&T delegate in several standards work groups under 3rd generation partnership program (3GPP) in 1999. In 2001, He moved back to the academia at San Jose

State University as the Pinson (Endowed) Chair Professor. Tony is Administrative Vice President of IEEE CPMT Society. He is distinguished speaker of IEEE CPMT Society and is in the speaker list of IEEE Reliability Society since 1997. Tony has co-authored/co-edited a book with IEEE Press/Addison Wesley and a Video tutorial with IEEE Press.

About the co-author:

Dr. Guna Selvaduray is Professor in Materials Engineering at San Jose State University, where he teaches a variety of undergraduate and graduate courses including biomaterials, engineering ceramics, microelectronic packaging, thermodynamics of solids, experimental methods in materials engineering, materials processing methods, corrosion and design for the environment. He initiated the Microelectronic Packaging concentration area within the MSE Program in 1991. Prior to joining the university, he worked in industry for 10 years. His research areas include microelectronic device interconnects and packaging, Pb-free solders, corrosion, surfaces and surface-related phenomena, recyclability of industrial materials.

Dr. Selvaduray has been the recipient of the Japanese Government (Mombusho) Scholarship (1964-1969) and the Fullbright-Hayes Fellowship (1974-1976). In 1997 he was awarded the SJSU College of Engineering's Excellence in Scholarship Award, and The California Emergency Services Association's Gold Award.

Monday March 31, 2003: Technical programme day 1

7.30	60	**Registration**

8.30		**Start Monday Morning Sessions**

		Opening Session
8.30	10	**Opening** *Olivier de Saint-Leger, MTA, France*

Session 1:		**Keynote session on Trends in Microelectronics & Microsystems**
8.40	30	**Keynote: From Smart Card to Smart Object** *Henri Boccia, Gemplus, France*
9.10	30	**Keynote: Market Situation, Trends and Reliability Issues of Micro-Systems as Enabler for Automotive Applications.** *Günter Lugert, Thomas Riepl, Siemens, Germany*
9.40	30	**Keynote: Needs for advanced packaging and new developments of IC process** *Didier Grenier STM, France*
10.10	30	**Keynote: Carbon nanotube applications in microelectronicss** *W. Hoenlein, F. Kreupl, G.S. Duesberg, A.P. Graham, M. Liebau, R. Seidel, E. Unger, Infineon, Germany*

10.40	30	Break

Session 2:		**Keynote session on State of the Art in Thermal and Mechanical Simulations**
11.10	30	**Keynote: Delamination of Electronic package** *Matthew Yuen, Haibo Fan, Hong Kong Univ. of Science and Technology, Hong Kong*
11.40	30	**Keynote: Computer-Aimed Engineering of Electro-Thermal MST Devices: Moving from Device to System Simulation** *Jan G. Korvink, Evgenii B. Rudnyi, University of Freiburg, Germany*
12.10	30	**Keynote: Prediction of Microelectronics Thermal Behavior in Electronic Equipment: Status, Challenges and Future Requirements** *Peter Rodgers, Electronics Thermal Management, Ltd., Ireland*

12.40	100	Lunch	**Welcome address by Mr M. Salord** Vice President, Council for Economic Development of Aix County

14.20		**Monday Afternoon Sessions**

	Parallel sessions		
14.20-15.50	**Session 3**		**Session 4**
	Adhesives, Encapsulation, and Underfill		**Thermal Behavior Modeling**

Session 3:		**Adhesives, Encapsulation and Underfill**
14.20	30	**Keynote: Development of the Green Plastic Encapsulation for High Density Wire Bonded Packages** *T.Y. Lin , C.M. Fang, Y.F. Yao, K.H. Chua, Agere Systems Singapore Pte Ltd., Singapore*
14.50	20	**Thermal-Mechanical Properties of an Electrically Conductive Adhesive** *M.H.H. Meuwissen, H.L.A.H. Steijvers, M. van den Nieuwenhof, E.P. Veninga, TNO Institute of Industrial Technology, The Netherlands*

15.10	20	**Micromechanical Modeling of Stress Evolution Induced During Cure in a Particle Filled Electronic Packaging Polymer** *D.G. Yang , K.M.B. Jansen, L.G. Wang, L.J. Ernst, Delft University of Technology, G.Q. Zhang, , H.J.L. Bressers, Philips, The Netherlands*
15.30	20	**Reliability Investigations of Flip Chip Package with Porous Solder Joints** *K.-C. Liao, H. H. Tsai, Mechanical Engineering, Mingchi Institute of Technology, Taiwan*

Session 4:		**Thermal Behavior Modeling**
14.20	30	**Keynote: Thermal Behavior of Stacked System-in-Package** *Jani Valtanen, Pekka Heino, and Eero Ristolainen, Tampere University of Technology, Finland*
14.50	20	**Modeling the Assembly and Performance of Optoelectronic Packages** *D. Gwyer, C. Bailey, K. Pericleous, University of Greenwich, UK* *D. Philpott, P. Misselbrook, Celestica, UK*
15.10	20	**Thermal Management of Joule-Heating Microreactor using Modelling Tools** *Nicolás Cordero, Jonathan West, Helen Berney, NMRC, University College, Ierland, Lee Maltings, Ireland*
15.30	20	**Study of Semiconductor Surfaces in the Radiant-Heat Transfer Systems** *V.I. Rudakov, V.V. Ovcharov, V.P. Prigara, Institute of Microelectronics and Informatics, Russian Academy of Sciences, Russia*

15.50	40	Break

	Parallel sessions		
16.30-18.00	**Session 5**		**Session 6**
	Reliability of Solder Interconnection		**Thermal & Mechanical Problems in Advanced Packaging**

Session 5:		**Reliability of Solder Interconnection**
16.30	30	**Keynote: Thermo Mechanical Solder Joint Fatigue Under Mobile Device Usage Conditions** *Pirkka Myllykoski, Nokia, Finland*
17.00	20	**Microstructure Evolution of Tin-Lead Solder** *R.L.J.M. Ubachs, P.J.G. Schreurs, and M.G.D. Geers, Eindhoven University of Technology, The Netherlands*
17.20	20	**Quantitative Microscopy of Microstructural Evolution in Eutectic Solders Subjected to Static Thermal load** *M.A. Matin, W.P. Vellinga, M.G.D. Geers, Eindhoven University of Technology, The Netherlands*
17.40	20	**FE Modeling of a Shear Test: Correlation with Experiments** *M. Gonzalez, B. Vandevelde, R. Van Hoof and E. Beyne, IMEC*, Belgium

Session 6:		**Thermal & Mechanical problems in Advanced Packaging**
16.30	30	**Keynote: Mechanical, Thermal and Electrical Issues in System-in-a-Package on Low-Cost Liquid Crystal Polymer Substrate** *Johan Liu, Liu Chen, Gang Zou, Chalmers University of Technology C/O IVF, Sweden, Jorma Kivilahti, Helsinki University of Technology, Finland*
17.00	20	**Reliability Prediction of Exposed Pad Type Semiconductor Packages** *Torsten Hauck, Tina Bohm, Motorola GmbH, Germany*
17.20	20	**Reliability Analysis of a New Type of Optical Fiber Array Module for Transceivers** *Hsiao-Tung Ku and Kuo-Ning Chiang, National Tsing Hua University, Taiwan*
17.40	20	**Feasibility Study of the Athermal Packaging for Fiber Bragg Gratings by Invar Effect Substrate** *H.H., Tsai, K.C. Liao, Mingchi Institute of Technology, Taiwan*

18.10		End of 1st day Technical Sessions

Tuesday April 1, 2003: Technical programme day 2

Tuesday, April 1, 2003

8.30		**Start Tuesday Morning Sessions**

	Parallel sessions		
8.30-10.00	**Session 7**		**Session 8**
	Advanced Packaging and MEMS Designing		**Thermal Modeling**

Session 7:		**Advanced Packaging and MEMS Designing**
8.30	30	**Keynote: Requirements in Advanced Packaging Curriculum** *Guna Selvaduray, Joseph F. Becker and H Anthony Chan, San Jose State Univ. ,USA*
9.00	20	**Nonlinear Reduced Modeling Of a Damped Dual-axis Accelerometer** *Eskild R. Westby, Tor A. Feldly, Norwegian Univ. of Science and Technology, Norway*
9.20	20	**FEA Simulation of Package Stress in Transfer Molded MEMS Pressure Sensors** *Rudolf Krondorfer, Timothy C. Lommasson, SensoNor asa, Norway* *Yeong Kim, Samsung, USA*
9.40	20	**Characterization of P and N Type Silicon Piezo-resistive Strain Gauges** *D. O'Mahoney, O. Slattery, E. Sheehan, F. Waldron, National Microelectronics Research Centre, University College Cork, Ireland*

Session 8:		**Thermal Modeling**
8.30	30	**Keynote: Component Modeling Methodology in Consumer Electronic Product Development** *Geneviève Martin,Wendy Luiten, Philips, The Netherlands*
9.00	20	**An Approach to a Numerical Simulation of Thermal Contact Problems in Electronic Packages** *K. Friedel; A. Wymysłowski, Wrocław University of Technology, Poland*
9.20	20	**A Model Based Optimization of a Line Shaped Laval Nozzle for Micro Abrasive Air Jetting** *A. Holtsmark, M. Achtsnick, A. M. Hoogstrate, B. Karpuschewski, A. Beukers, Delft University of Technology, The Netherlands*
9.40	20	**Investigations of the Thermal Properties of AII-BVI Mixed Crystals with the Piezoelectric Phase Method** ***M. Maliński, Technical University of Koszalin*** *J. Zakrzewski, H. Męczyńska, Nicolaus Copernicus University, Poland*

10.00	30	Break

	Parallel sessions		
10.30-12.40	**Session 9**		**Session 10**
	Designing for Endurance and Reliability		**Thermal Performance**

Session 9:		**Designing for Endurance and Reliability**
10.30	30	**Keynote: Design Analysis and Optimization of Wirebond Stacked Die BGA Packages for Improved Board Level Solder Joint Reliability** *Tong Yan Tee, Hun Shen Ng, Xavier Baraton, STMicroelectronics Singapore* *Zhaowei Zhong, Nanyang Technological University, Singapore*
11.00	20	**Optimization of the Reliability of a BGA Package by Finite-Element-Simulation** *Anton Legen, Manuel Carmona, Jens Pohl, Jochen Thomas, Infineon Technologies AG, Germany*
11.20	20	**Response Surface Methodology for Enhancing Theoretical Models: Application to Warpage Prediction of CSP BGAs*** *Eric Egan, Tom O'Donovan, Peter Kennedy, National University of Ireland* *Gerard Kelly, Cork Institute of Technology, Ireland*

11.40	20	**Solution and Test of a Numerical Model Describing Lithium-ion Batteries Internal State** *F. Ternay, A. Laurent, S. Martinet, CEA/Grenoble, DTEN/SCSE, France*
12.00	20	**Fatigue Damage Modeling in Solder Interconnections: A Cohesive Zone Approach** *Adnan Abdul-Baqi, Piet J.G. Schreurs, Marc G.D. Geers,* *Eindhoven University of Technology, The Netherlands*
12.20	20	**The Reliability Study of Underfill Flip Chip in Micro-electronic Packaging** *Xiaosong Ma, J.J. Chen, D.G. Yang, Xi'an Univ. of Electronic Technology and* *Guilin Univ. of Electronic Technology*

Session 10:		**Thermal Performance**
10.30	30	**Keynote: Board Via Effect on Thermal Performance of a Leadless Package** *Heinz Pape, Kay Schiller, Rudolf Kutscherauer, Infineon Technologies AG, Germany*
11.00	20	**Wafer Scale Power Transistor Package: Electro-Thermal Modeling and Validation** *A.W.J.P. den Boer, M.A.J. van Gils, G.M. Janssen, Philips, The Netherlands*
11.20	20	**Comparative Study of Power Module Technologies by means of Thermal Simulation Tools** *Peter Hansen, Flemming Nielsen, Hans S. Nielsen, John Jacobsen,* *Grundfos A/S, Denmark*
11.40	20	**An Investigation of Thermal Enhancement of MPM BGA Package** *Abe-JM Yang, Cary Yang, Carol Liang, Jeng Yung Lai, Yu-Po Wang, CS Hsiao,* *Siliconware Precision Industries Co., Ltd., Taiwan*
12.00	20	**Packaging Simulation in Gas Flow Sensors** *N.Sabaté, I.Gràcia, J.Berganzo, C.Cané, Centre Nacional de Microelectrònica,* *CNM-CSIC, Spain*

12.40	90	Lunch

14.10		**Start Tuesday Afternoon Sessions**

	Parallel sessions		
14.10-16.20	**Session 11**		**Session 12**
	MEMS, Sensors and Actuators		**IC Process Reliability Modeling and Characterization**

Session 11:		**MEMS, Sensors and Actuators**
14.10	30	**Keynote: Design Study for Stacked MEMS** *Jan Eite Bullema, Marcel Meuwissen, Erik Veninga, TNO, The Netherlands*
14.40	20	**Thermal FEM Simulation of Ultra-Miniaturised Wall Shear Stress Sensors** *Delphine Meunier, Jumana Boussey, Chargée de Recherche CNRS, Institut de* *Microélectronique, Electromagnétisme et Photonique, IMEP, France,* *Sedat Tardu, Laboratoire des Ecoulements G´eophysiques et Industriels,* *LEGI, INPG-UJF-CNRS, France*
15.00	20	**Design, Analysis and Validation of Vertical Probing Technology** *Chang-An Yuan, Hsing-Chih Liu, Ming-Hung Sun and Kou-Ning Chiang* *National Tsing Hua University, Taiwan*
15.20	20	**Development of a Compact Thermal Model for a Micro-Pyrotechnic Actuator** *M. Salleras, J. Palacín, M. Puig, J. Samitier, S. Marco, Univ. de Barcelona, Spain*
15.40	20	**Experimental Verification of the Finite-Element Model of a Thick-film Ceramic Pressure Sensor** *Marina Santo Zarnik, Darko Belavic, HIPOT-R&D / Jozef Stefan Institute, Slovenia* *K.P. Friedel; A. Wymysłowski, Wroclaw University of Technology, Poland*
16.00	20	**Modeling of Pyroelectric Sensor Arrays** *Günter Milde, Jörg Drescher, Gerald Gerlach, Herbert Balke, Hans-Achim Bahr, TU Dresden, Germany*

Session 12:		**IC Process Reliability Modeling and Characterization**
14.10	30	**Keynote: Prediction of Crack Growth of IC Passivation Layer** *G.Q. Zhang, M.A.J. van Gils, R.B.R. Silfhout, W.D. van Driel, Philips, The Netherlands* *Y.T. He, L.J. Ernst, Delft University of Technology, The Netherlands*

14.40	20	**The Impact of Wafer-Level Stress on Package Warpage and Die Attach Stress** Eric Egan, Anne-Marie Kelleher, Tom O'Donovan, Peter Kennedy, National University of Ireland *Gerard Kelly, Cork Institute of Technology, Ireland*
15.00	20	**Prediction of Interfacial Delamination in Stacked IC Structures using Combined Experimental and Simulation Methods** *Zhang G.Q, Van Driel W., Van Gils M., Van Silfhout R., Philips, The Netherlands* *Liu C.J., Ernst L.J., Delft University of Technology, The Netherlands*
15.20	20	**Mechanical FEM Simulation of Bonding Process on Cu lowK Wafers** *Dominiek Degryse, Bart Vandevelde and Eric Beyne, IMEC, Belgium*
15.40	20	**Effect of Delamination of IC/Compound Interface on Passivation Cracking** *R.B.R van Silfhout, J.D. Roustant, W.D. van Driel, Y. Li, G.Q. Zhang, M.A.J. van Gils,* *Philips, The Netherlands, D.G. Yang, Delft University of Technology*
16.00	20	**Prediction of Thermo-mechanical Integrity of Wafer Backend Processes** *G.Q. Zhang, J. den Toonder, J. Beijer, Philips, The Netherlands* *R.J.O.M. Hoofman, Philips Belgium* *V. Gonda, , L.J. Ernst, Delft University of Technology, the Netherlands*

16.20	30	Break

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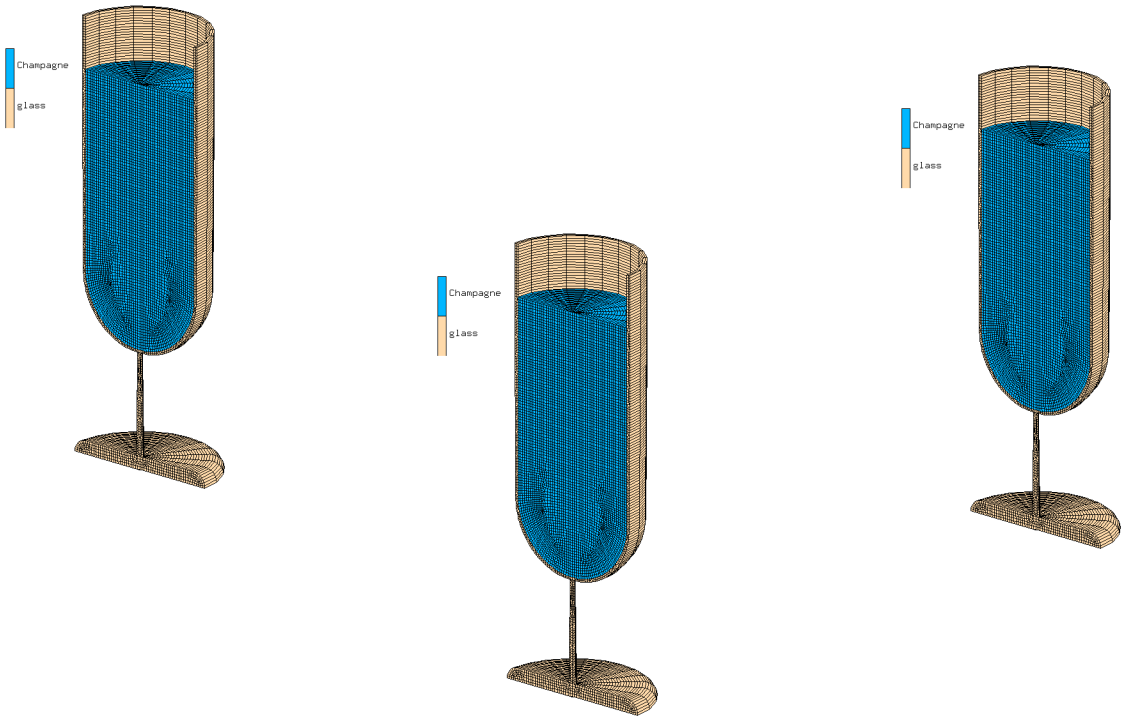
16.50 – 18.10	**Special Exhibitor session**

18.10		End of 2nd day Technical Sessions

18.10		Cocktail reception



Wednesday April 2, 2003: Technical programme day 3

8.30		Start Wednesday Morning Sessions

Session 13:		Keynote session on Characterization and Modeling of Materials and Reliability
8.30	30	**Keynote: New Failure Analysis Methods in Microelectronics** *Ingrid de Wolf, IMEC, Belgium*
9.00	30	**Keynote: Simulation of Microstructure Evolution in Metallic Alloys** *Markus Apel, B. Böttger, G.J. Schmitz, Univ. of Aachen, Germany*
9.30	30	**Keynote: Investigations on Low Cycle Fatigue of Electrodeposited Thin Copper and Nickel Films** *Rainer Dudek, Hans Walter, and Bernd Michel, Fraunhofer-IZM, Germany* *Jörg Zapf, Siemens AG, Germany*

10.00	40	Break

	Parallel sessions		
10.40-12.30	**Session 14**		**Session 15**
	Simulation and Optimization in Microelectronics		**Designing towards Environmental Demands**

Session 14:		Simulation and Optimization in Microelectronics
10.40	30	**Keynote: Optimization and Finite Element Analysis for Reliable Electronic Packaging** *S. Stoyanov, C. Bailey, University of Greenwich, UK*
11.10	20	**Numerical Simulation and Optimization of Capacitive Transducers** *H. Landes, R. Lerch, M. Kaltenbacher, R. Peipp, University of Erlengen-Nuremberg* *F. Vogel, inuTech GmbH, Nuremberg, Germany*
11.30	20	**Comparison of Lifetime Predictions with 3D Finite Element Models of a High Density Flip Chip without Underfill on LTCC** *M. Spraul, W. Nüchter, A. Möller, Robert Bosch Gmbh, Germany* *A. Schubert, B. Michel, Fraunhofer IZM, Germany*
11.50	20	**The Reliability Analysis and Structure Design for Fine Pitch Flip Chip BGA Packaging** *Chih-Tang Peng, Chang-Ming Liu, Ji-Cheng Lin, Kuo-Ning Chiang,* *National Tsing Hua University, Taiwan*
12.10	20	**Influence of Material Combinations on Delamination Failures in a Cavity Down TBGA Package** *W.D. van Driel, G.Q. Zhang, Philips, The Netherlands* *A.Y.L. Chang, Philips Semiconductors Kaohsiung, Taiwan* *G. Wisse, L.J. Ernst, Delft University of Technology, The Netherlands*

Session 15:		Designing towards Environmental Demands
10.40	30	**Keynote: The State of the Art of Lead-Free Solders** *Sabine Knott and Adolf Mikula*
11.10	20	**Microstructure and Creep Behaviour of Eutectic SnAg and SnAgCu Solders** *S. Wiese, K.J. Wolter, Technische Universität Dresden, Germany*
11.30	20	**Tensile and Fatigue Isothermal Properties of Copper Joints with Sn63-Pb37, Sn62-Pb36-Ag2 and Sn42-Bi58 Alloys** *E. M. Grigoletto, A. Damasco, I. Ferreira, State University of Campinas, Brasil*
11.50	20	**Parametric Study on Flip Chip Package with Lead-Free Solder Joints by using the Probabilistic Designing Approach** *J.S. Liang, D.G. Yang, Q.Y. Li, Guilin University of Electronic Technology, China* *L.J. Ernst, Delft University of Technology, The Netherlands* *G. Q. Zhang, Philips, The Netherlands -*

12.30	90	Lunch

14.00		**Start Wednesday Afternoon Sessions**

Session	**16:**	**Keynote session on New Techniques in Modeling and Characterization**
14.00	30	**Keynote: Material Response Prediction and Understanding Through the use of Molecular Modeling** *Nancy Iwamoto, Honeywell, USA*
14.30	30	**Keynote: Micro-Digital Image Speckle Correlation and Its Applications to Microelectronics Packages** *Xunqing Shi, Singapore Institute of Manufacturing Technology, Singapore*
15.00	30	**Keynote: Understanding Morphology Changes in Solders** *Wolfgang H. Müller, Technische Universitat Berlin, Germany*
15.30	30	**Keynote: A Simulation-Based Multi-Objective Design Optimization of Electronic Packaging under Thermal Cycling and Bend Load** *Leon Xu, Wei Ren, and Tommi Reinikainen -- NOKIA Mobile Phones, USA*

16.00	End of Conference

List of exhibitors

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I shall attend (please tick boxes) :

the course(s) on Sunday March 30:

- ☐ C1 (½ day) Moisture related reliability issues in electronic packages.
- ☐ C2 (½ day) Introduction to IC process reliability.
- ☐ C3 (½ day) Theoretical Reliability Assessment in Packaging
- ☐ C4 (full day) Experimental characterisation of Components and System Thermal Performance
- ☐ C5 (½ day) Coupled-field Predictive Simulation for Virtual Test of Microsystems
- ☐ C6 (½ day) Advanced Packaging

Half day courses (C2..C5): **250** € (registration till **March 15th**, 2002) or **350** € (after March 15th)

Full day course (C1) : **500** € (registration before **March 15th**, 2002) or **600** € (after March 15th).

Includes course notes and lunch.

☐ the conference on March 31, April 1-2 — **500** € (early registration till **March 14**, 2003) or **600** € (after **March 14**, 2003).
Includes proceedings, 3 lunches, and dinner on Monday March 31

☐ additional person(s) at the Monday dinner: **60 €** per person

☐ programme for accompanying person (Aix and surroundings, 1 day visit): **100 €** per person

☐ tick if you wish vegetarian meals

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Cancellation policy

- We reserve the right to cancel a course if the number of attendants is not sufficient by March 15, 2003. We shall then refund you the corresponding amount.
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