Power Electronics Research at UCF

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Florida Power Electronics Center (*FloridaPEC*)
University of Central Florida (UCF)
Orlando, Florida, USA
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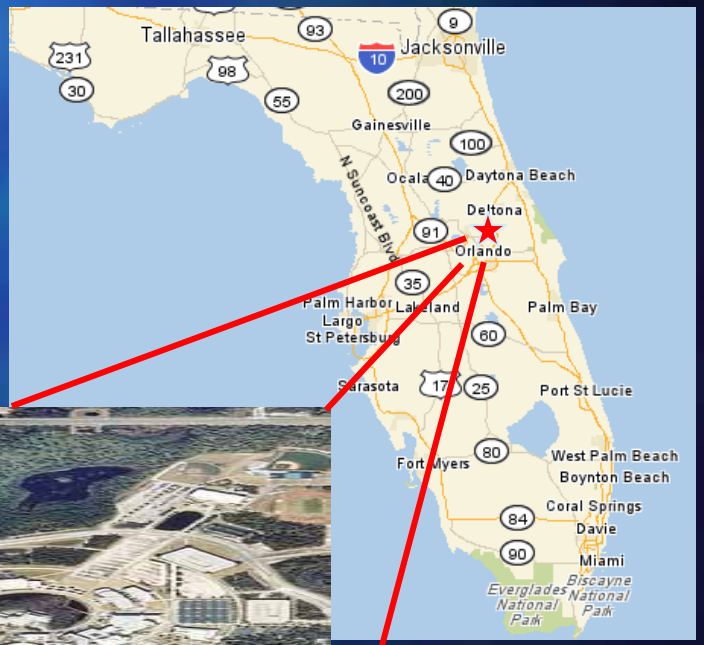
University of Central Florida (UCF)

- UCF is a public, metropolitan research university, dedicated to serving its surrounding communities with their diverse and expanding populations, technological corridors, and international partners.
- UCF, founded in Orlando in 1967, is now the 8th largest university in the nation with an enrollment of about 44,000 in 2004.
- UCF College of Engineering and Computer Science (CECS) has an enrollment of 5,000 undergraduate and 1,300 graduate students in 2004.
- CECS is ranked in the top 9% of colleges for the number of Bachelor's degrees, and top 12% for the number of PhD degrees awarded in engineering.



School of Electrical Engineering and Computer Science (EECS)

- **60** fulltime faculty with research interests in wireless communication, digital signal and image processing, microelectronics and solid state devices, power electronics, microwaves and antennas, intelligent systems, robotics and controls, VLSI design, computer architecture, network and mobile computing, software engineering, computer graphics, computational imaging, evolutionary computation, computer vision, artificial intelligence, and database systems.
- **2109** undergraduate, **274** MS, and **286** PhD graduate students in 2005.
- Research funding was over **$6M** in 2005.

Florida Power Electronic Center (*FloridaPEC*)

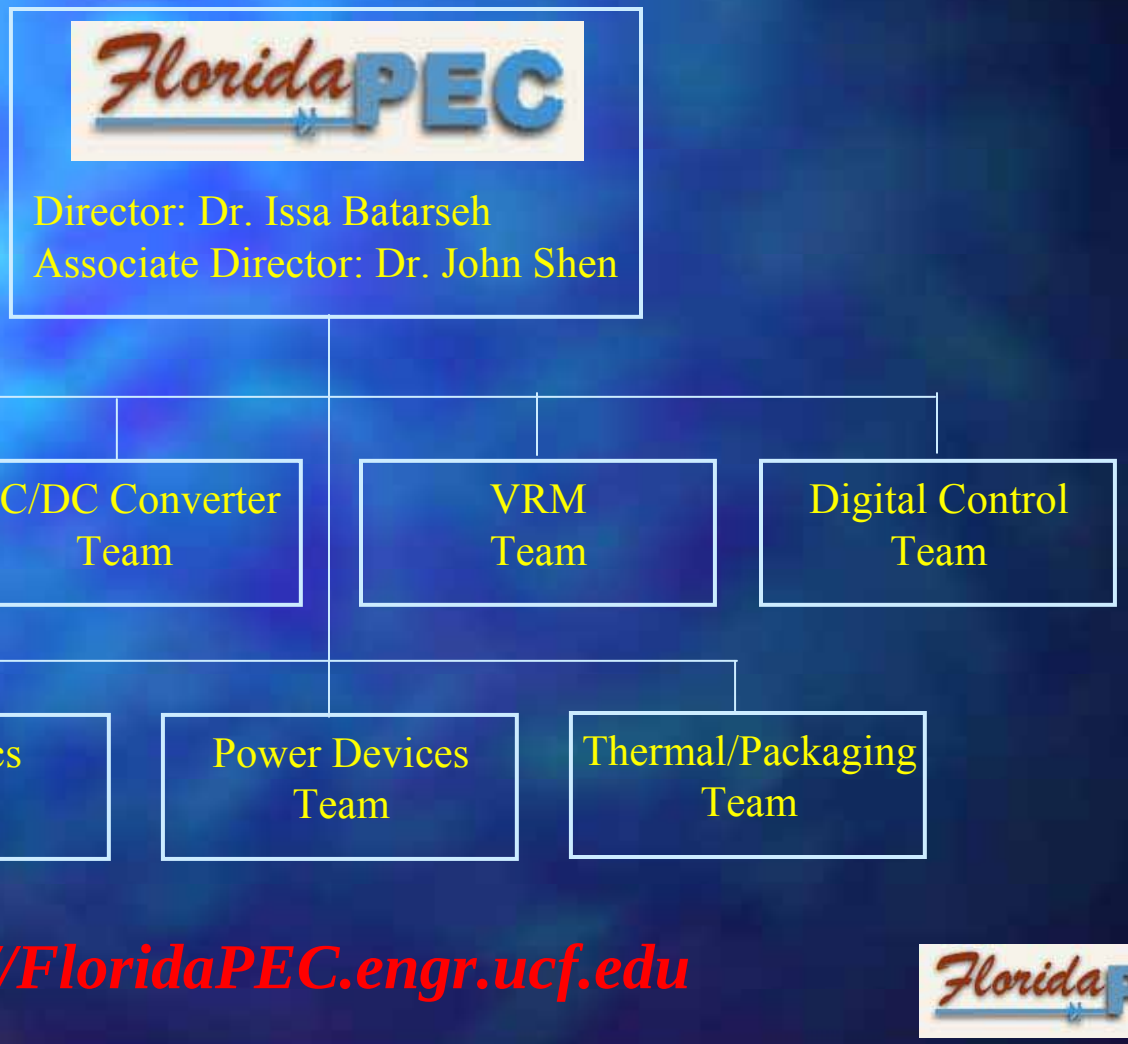
- ***FloridaPEC* was established in 1998 at UCF to carry on research and development activities in various areas of power electronics. The center is focused on development of high frequency power electronic systems to improve power density, efficiency and performance.**
- **The center currently has 4 faculty members, 3 affiliate faculty members, and 25 graduate research assistants and staff members.**

Research Areas

- *High-frequency dc-dc conversion*
- *Active power factor correction*
- *Soft-switching resonant dc-dc technology*
- *Control and dynamic modeling of power electronic systems*
- *Advanced power semiconductor devices and ICs*
- *Advanced and integrated magnetic components*
- *New thermal management and packaging technology.*
- *Photovoltaic Modeling*

http://FloridaPEC.engr.ucf.edu

Florida Power Electronic Center



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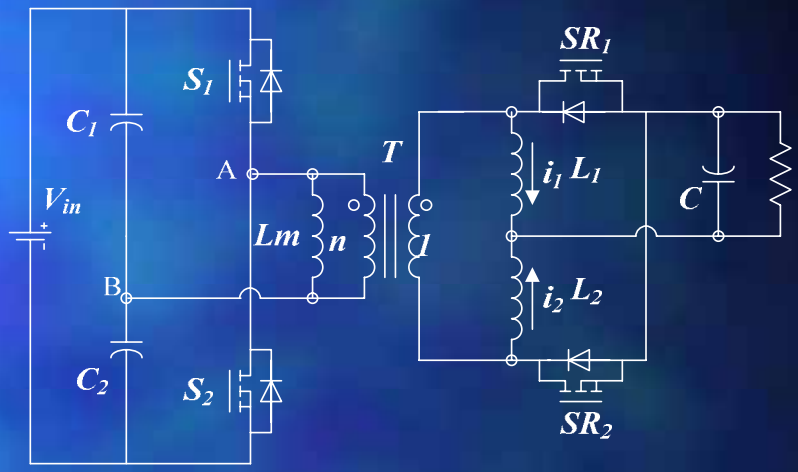
Research at a glance

50W Quarter Brick DC/DC Converter

- Input: 36~75V
- Output: 1.0V/50A
- Size: 2.3*0.9*0.2 inch^3
- Efficiency: 90% peak/88% @ full load
- Voltage ripple: Vp-p=10mV(no noise)
- Transient Deviation: 50mV deviation for 50% (10A/us) load change



DCS Half Bridge DC-DC Converter with Current Doubler Rectification

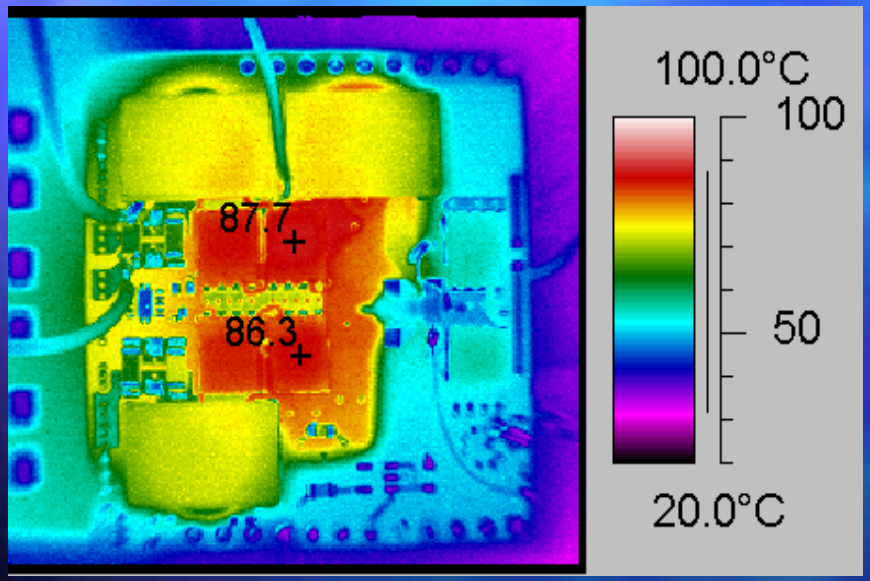
Features:

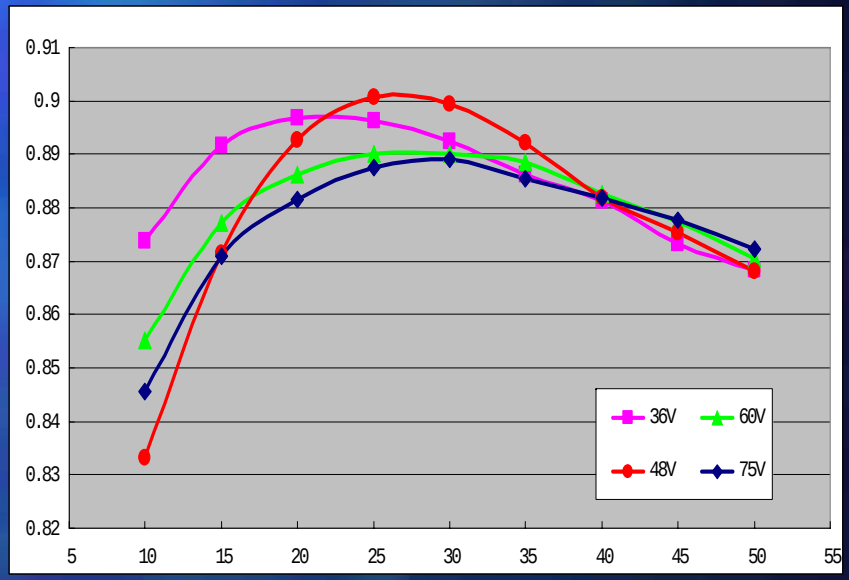
- Soft-switching for one switch
- Reduced leakage inductance ringing
- No DC bias of transformer magnetizing current
- Same voltage and current stresses as symmetric HB

Research at a glance

50W Quarter Brick DC/DC Converter

Thermal Photograph with fan cooling





Vin =48V, Vo=1V@ 50A Full Load with
23 Degree C of Ambient Temperature

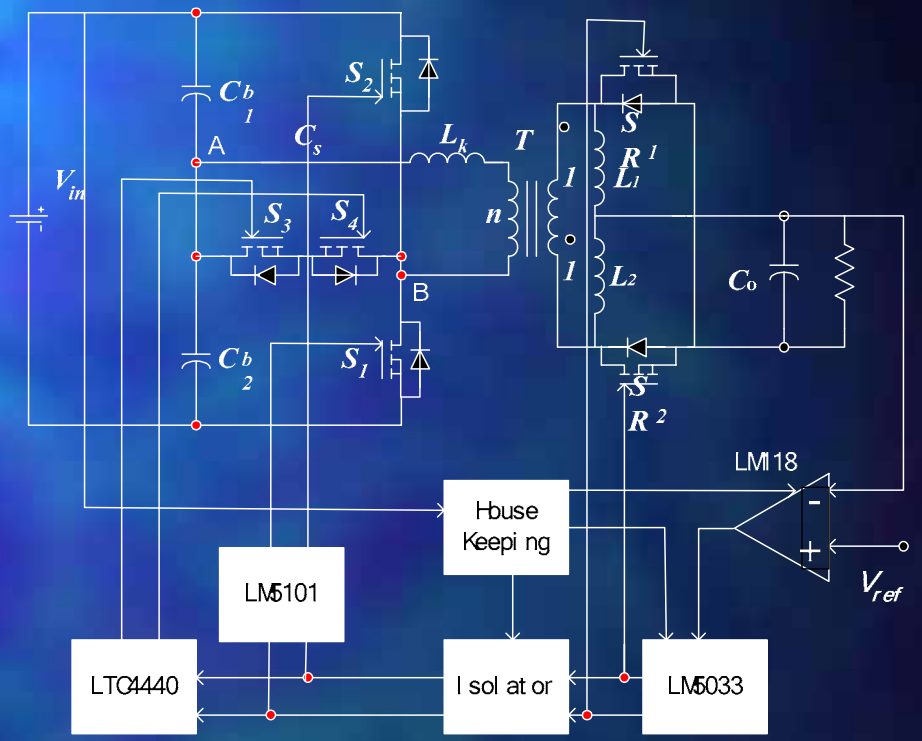
Research at a glance

30W 1/16th Brick DC/DC Converter

- Input: 36~75V
- Output: 1.0V/30A
- Size: 1.3*0.9*0.2 inch³
- Efficiency: 86% @ full load
- Voltage ripple: Vp-p=10mV(no noise)
- Load Slew Rate : 50 amps/usec. 10 us max. 2% max deviation at zero external capacitance

Features:

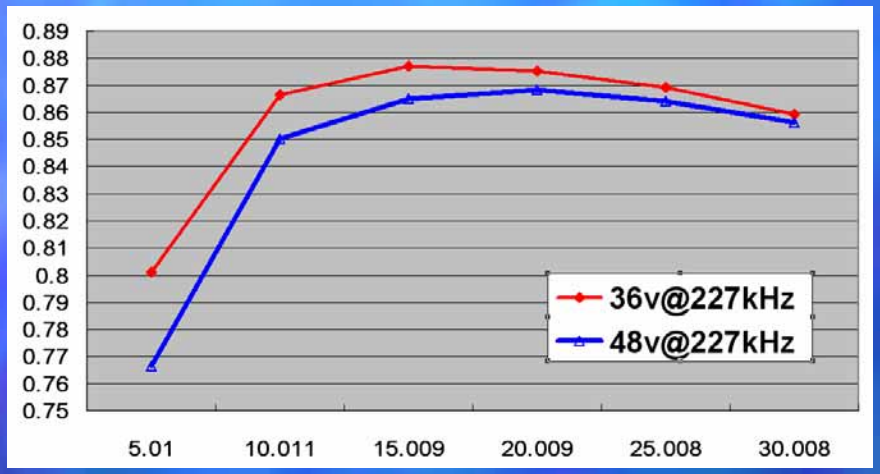
- Secondary-side control to eliminate isolation delay
- ZVS for high switching frequency



Active Clamped Half Bridge DC-DC Converter with Current Doubler Rectification

Research at a glance

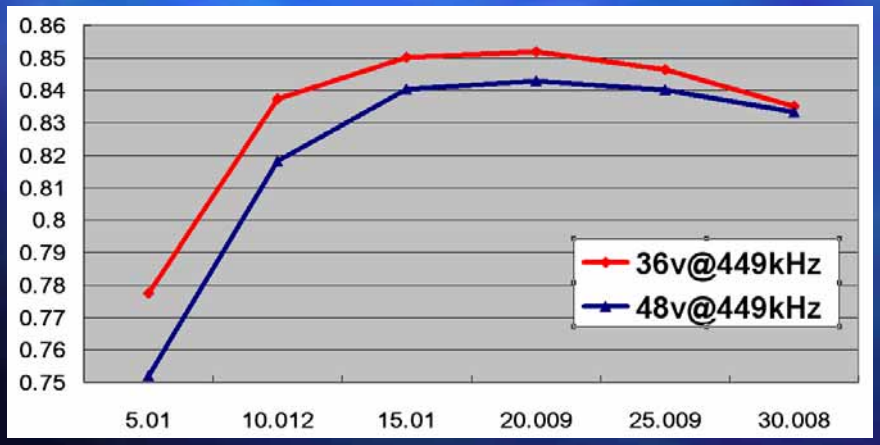
30W 1/16th Brick DC/DC Converter



Vin=48V, Vo=0.995V

Io=30A, Fs=227kHz

EFF=85.64%



Vin=48V, Vo=0.995V

Io=30A, Fs=449kHz

EFF=83.33%

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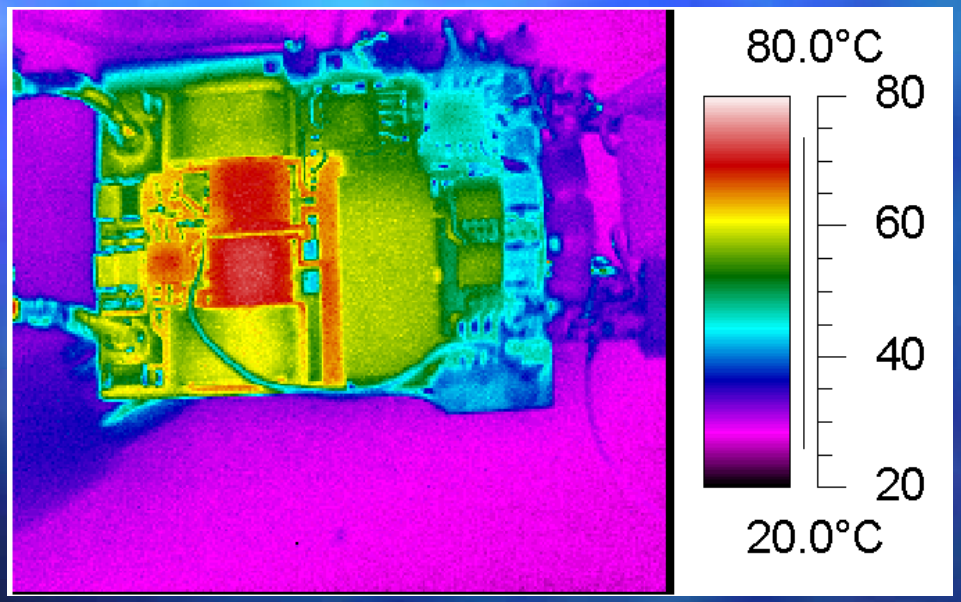
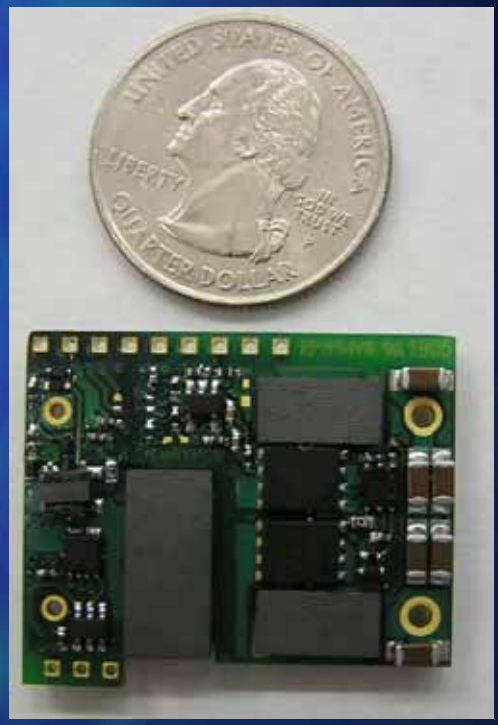
Research at a glance

30W 1/16th Brick DC/DC Converter

Thermal Photograph with fan cooling





Vin =48V, Vo=1V@ 30A Full Load with
Fs=450 kHz

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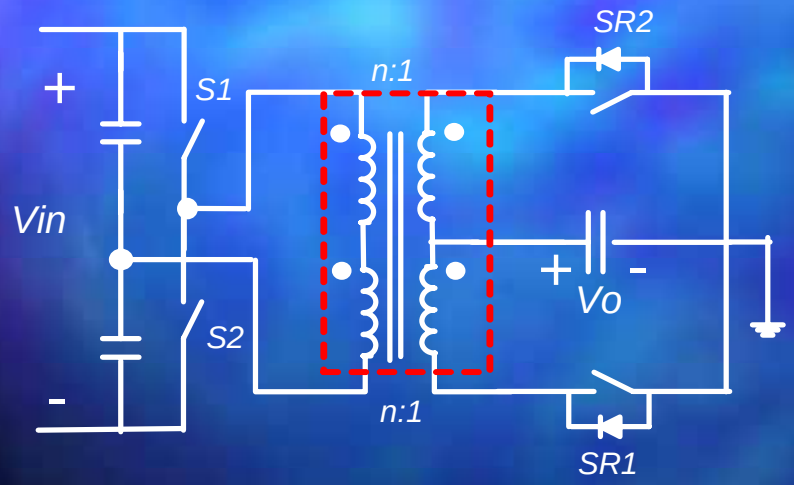
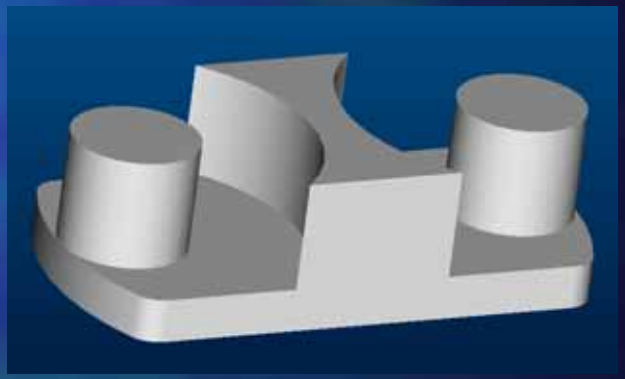
30W 1/16th Brick DC/DC Converter: Single Stage With IM Topology

Research at a glance

- Increased leakage inductance is helpful to achieve ZVS for main switches
- Control is exactly same as active-clamp half-bridge converter
- Magnetic core is customized for the specific design

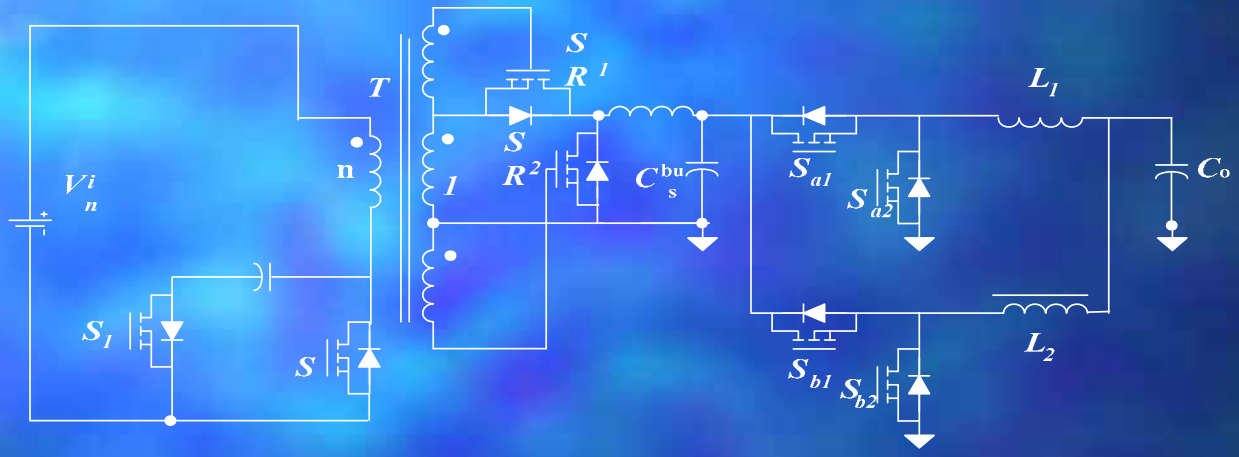




Customized Core

1/8th Brick DC/DC Converter: Two Stage Topology

Research at a glance



1st Stage: Active Clamped Forward DC-DC Converter

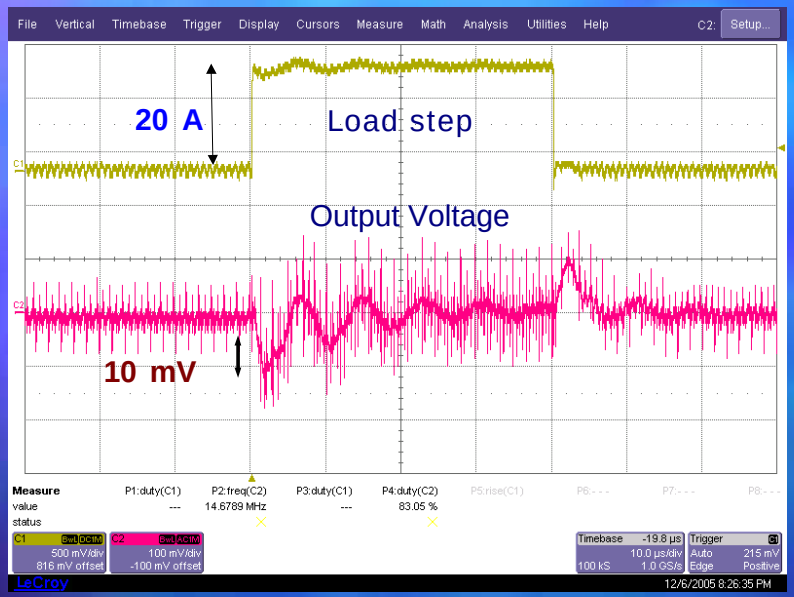
- ✓Soft switching
- ✓Simple control
- ✓Self-driven SRs
- ✓High efficiency

2nd Stage: Two Phase Buck Converters with Coupled Inductors

- ✓State-of-the-art technology
- ✓Two-phase interleaved and inductor-coupled buck converters
- ✓No isolation opto-coupler delay, high bandwidth
- ✓Low input voltage to reduce switching loss
- ✓1.5MHz to 2MHz output voltage ripple

1/8th Brick DC/DC Converter: Two Stage Topology Transient Response

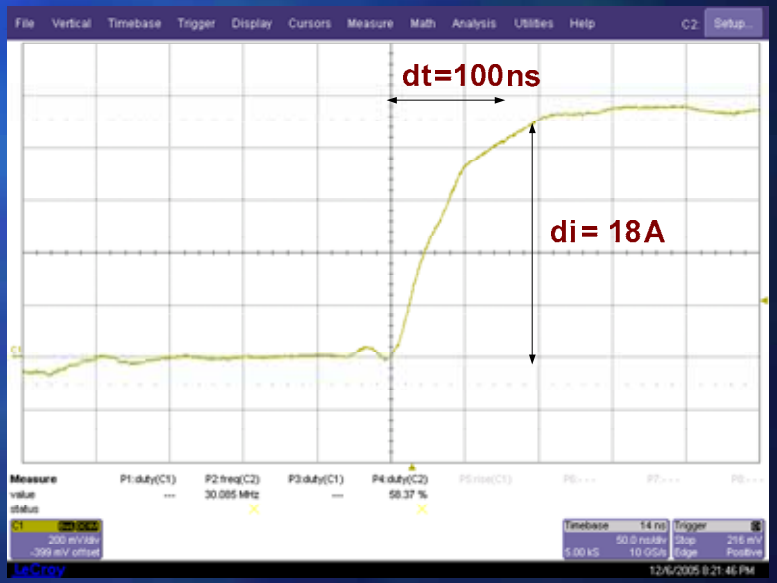
Research at a glance



Output Voltage = 1V

Output Current Step=20 A

Output capacitance= 800uF

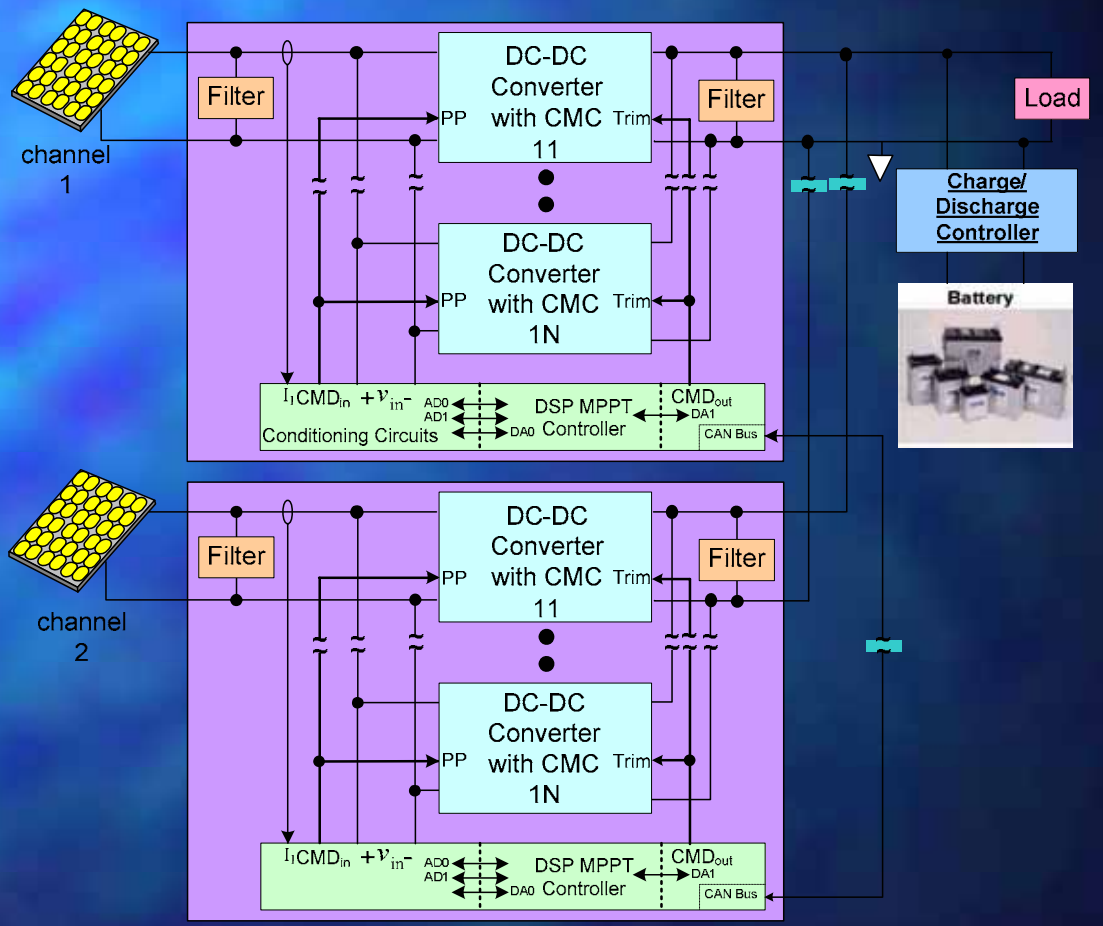


- ✓ di/dt =18A/100 ns = 180 A/us
- ✓ Overshoot & Undershoot = 10 mV

Modular Solar Power for Satellites: System Architecture

Research at a glance

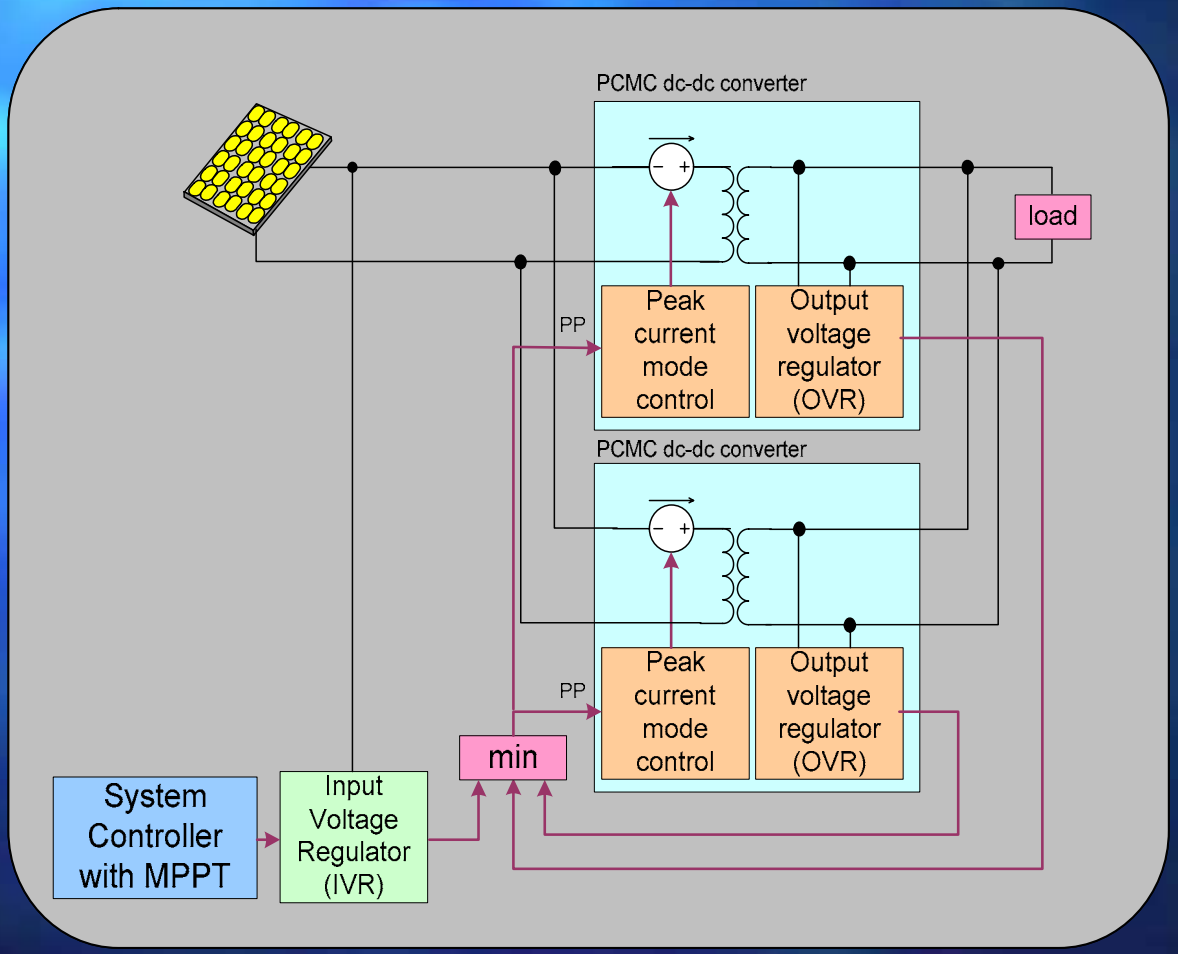
- **COTS based:**
  - **Easily customizable**
  - **Shorter design cycle**
- **Modular:**
  - **Master-less control**
  - **Scalable**
  - **Fault-tolerant**
  - **N+1 Redundant**
- **Digitally controlled:**
  - **Flexible**
  - **Reconfigurable**
  - **Lower cost**
- **Peak power tracking:**
  - **Maximize power yield**
  - **Avoid instability**



Research at a glance

Modular Solar Power for Satellites: Solar Channel Structure

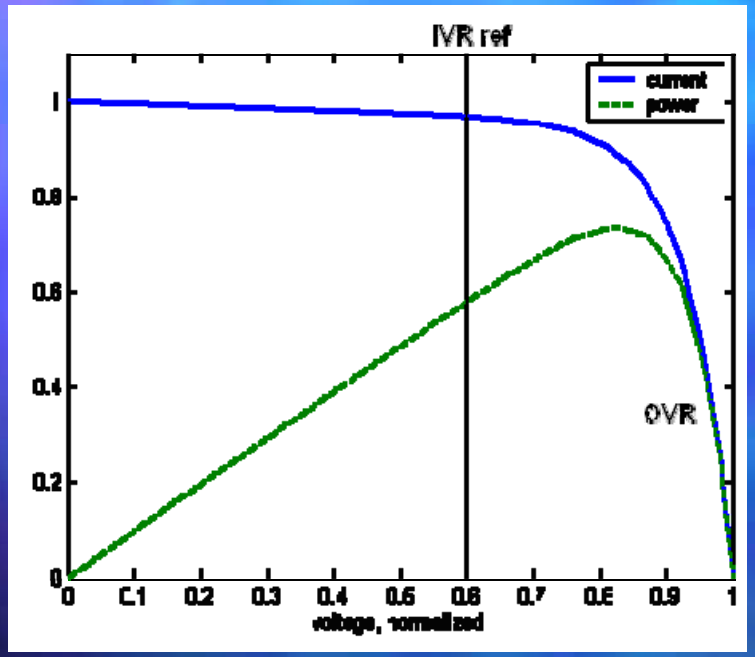
Input voltage regulation is added to allow operation in MPPT at excessive loads.



Output voltage regulation is built into the dc-dc modules, and is active for light loading.

Modular Solar Power for Satellites: Solar Channel Operating Modes

Research at a glance

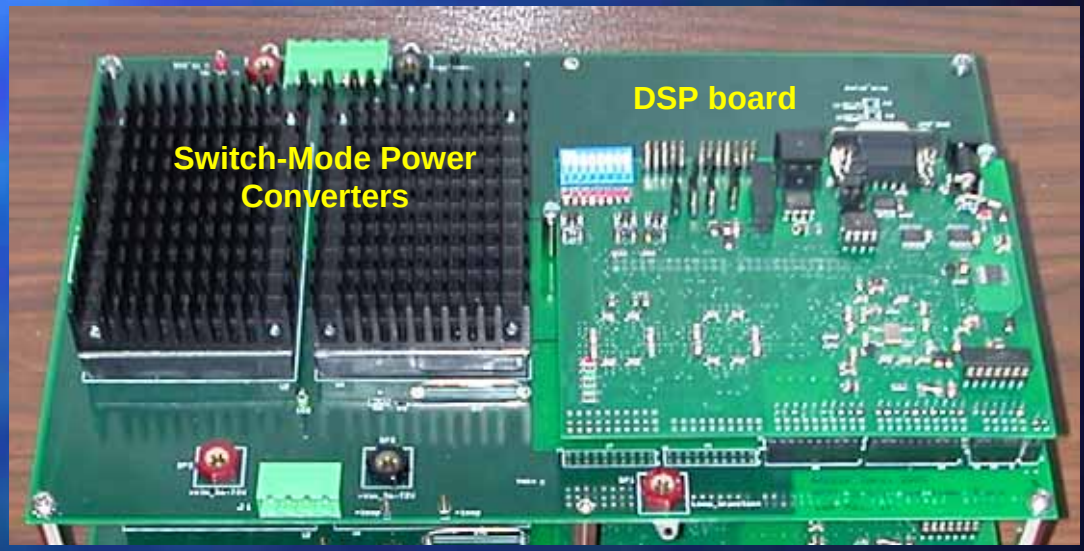


- Input voltage regulator (IVR) is activated in MPPT mode, i.e. when loading exceeds available power.
- Output voltage regulator (OVR) is built in and is active when loading is low.

Power rating: 2 COTS/channel @ 250W/unit = 500W/channel

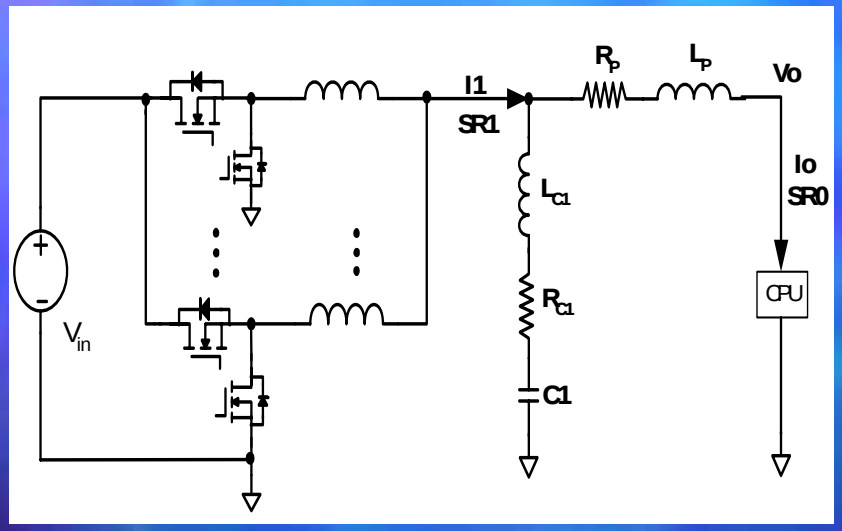
Input voltage range: 36-72V

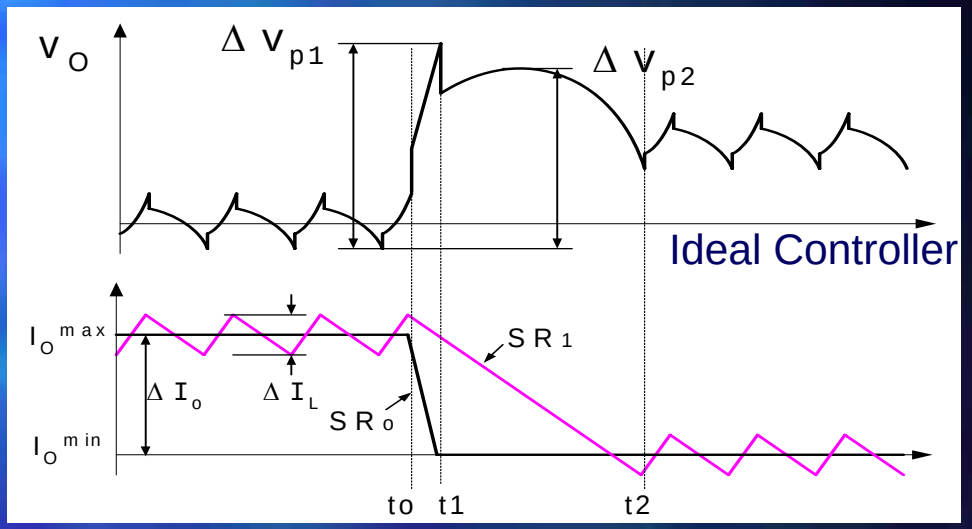
Output voltage: regulated at 28V



Research at a glance

The Problem in VRM High Slew Rate Load





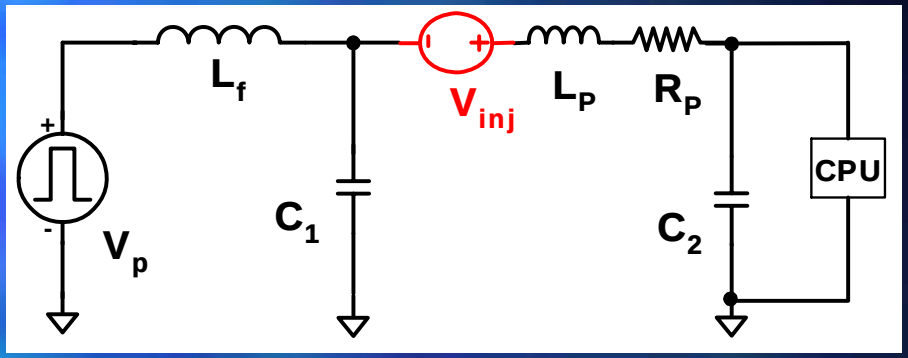
- **Basic issue: SR_1 cannot catch up with SR_0**
  - 1st ΔVp1:mainly determined by ESR, ESL and ΔIo
  - 2nd ΔVp2:mainly determined by ESR, C1 and ΔIo
- **×Higher fs and lower Lf benefit ΔVp, resulting in lower efficiency**
- **×Delay time in controller deteriorates ΔVp**

Active Transient Voltage Compensator for VRM Load Line Improvement

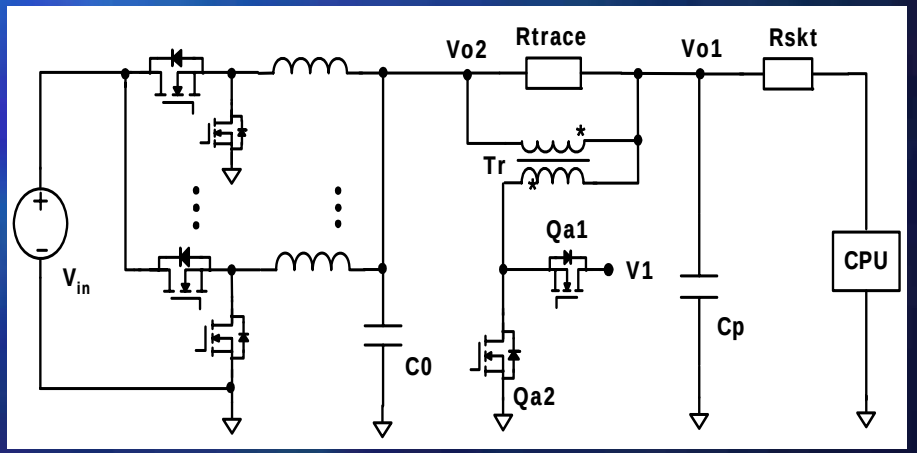
Research at a glance

- An Active Transient Voltage Compensator (ATVC) injects positive voltage to compensate the voltage drop in step-up load and energy recovery in step-down load.
- An transformer (n:1) is introduced for voltage injection so that current stresses of ATVC are largely reduced, only 1/(1+n) of prior arts, resulting in high efficiency in aux-converter.

Series ATVC



Parallel ATVC



Active Transient Voltage Compensator for VRM Load Line Improvement

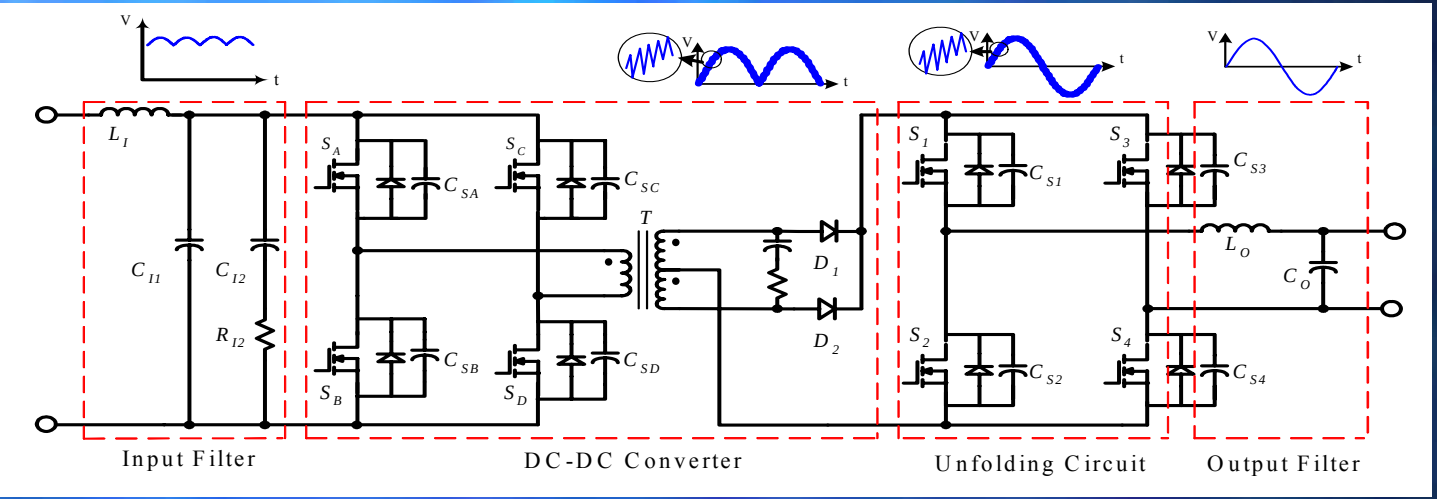
Research at a glance

VR10.1, VTT Tools, Vo=1.5V, $R_{LL\text{-}DC}$=1.15mΩ, ATVC for 2nd voltage spike $R_{LL\text{-}AC}$ improvement
ATVC: ER11, 1:1, 5Vin, 1.5MHz, **6*560uF in north, 4*560uF in east, Intel MB**

Slew rate		5~50A			5A~80A			5A~100A		
		Base	ATVC	Δ(+)	Base	ATVC	Δ(+)	Base	ATVC	Δ(+)
Step up load	180A/us	1.58mΩ	1.33mΩ	15.6%	1.63mΩ	1.33mΩ	18.4%	1.57mΩ	1.32mΩ	15.9%
	250A/us	1.58mΩ	1.35mΩ	14.6%	1.63mΩ	1.39mΩ	14.7%	1.60mΩ	1.37mΩ	16.9%
	550A/us	1.62mΩ	1.42mΩ	12.3%	1.67mΩ	1.43mΩ	14.4%	1.63mΩ	1.45mΩ	11%
	10A/ns	1.62mΩ	1.39mΩ	14.2%	1.67mΩ	1.47mΩ	12%	1.66mΩ	1.52mΩ	8.4%
Step down load	180A/us	1.53mΩ	1.30mΩ	15%	1.51mΩ	1.35mΩ	10.6%	1.54mΩ	1.39mΩ	9.7%
	250A/us	1.55mΩ	1.32mΩ	14.8%	1.53mΩ	1.36mΩ	11.1%	1.56mΩ	1.41mΩ	9.6%
	550A/us	1.58mΩ	1.33mΩ	16.5%	1.59mΩ	1.43mΩ	10.1%	1.60mΩ	1.47mΩ	8.1%
	10A/ns	1.6mΩ	1.42mΩ	13.8%	1.60mΩ	1.49mΩ	6.9%	1.64mΩ	1.54mΩ	6.1%
LL_{AC} in step up	Maxi	24mV 0.53mΩ			34mV 0.45mΩ			39mV 0.41mΩ		
	Expected	14mV 0.31mΩ			24mV 0.32mΩ			29mV 0.31mΩ		
LL_{AC} in step down	Maxi	22mV 0.49mΩ			29mV 0.39mΩ			38mV 0.4mΩ		
	Expected	12mV 0.27mΩ			19mV 0.25mΩ			28mV 0.29mΩ		

Research at a glance

PV Based Grid-Tie Inverter System



- **Single-staged inverter system only have a single high switching frequency of power processing stage, which regulates both input DC source and output under the control of DSP.**
- **With MPPT Algorithm, the power of PV array can be regulated at its maximum power point.**
- **By reducing the high frequency power processing stage from two to one, single-staged inverter system can achieve higher efficiency and reliability**

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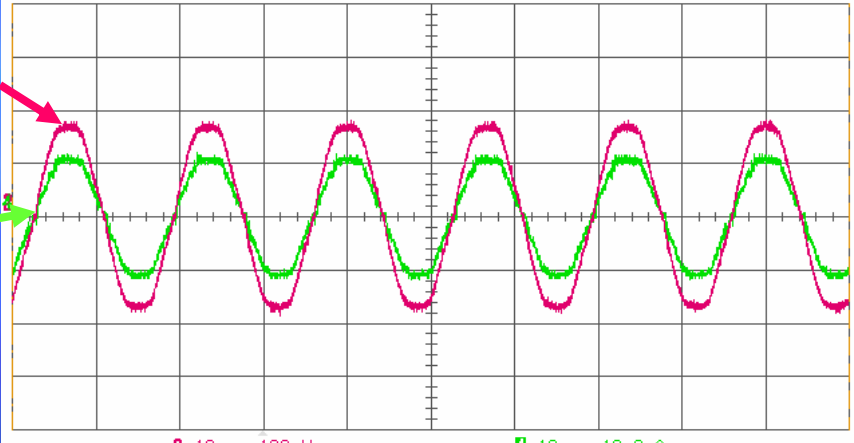
Research at a glance

Grid-Tie for 1kW Inverter Prototype

Grid Voltage

Inverter Output Current



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Power Semiconductor Research: Modeling and Design Capability

Research at a glance

Power Electronic Systems

Circuit/System Level

PSPICE, SABER, CADENCE, ANSOFT (Simplorer), Simulink

Circuit design verification, IC design, control design

Device/Process Level

Synopsis (ISE-TCAD), ANSOFT

Device behavior and internal physics modeling, device/circuit interaction, process development

Packaging/Thermal/Mechanical

ANSOFT, UCF FEA Software

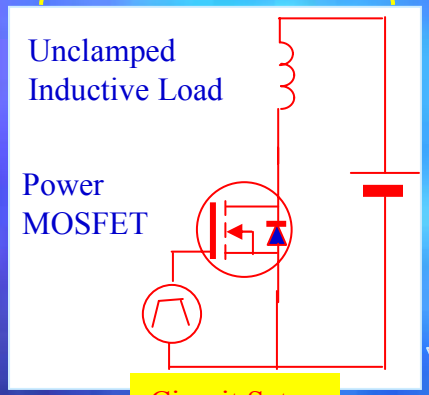
Thermal, mechanical stress modeling, electromagnetic modeling, package development

Power Semiconductor Research: Mixed-Mode Device/Circuit Modeling

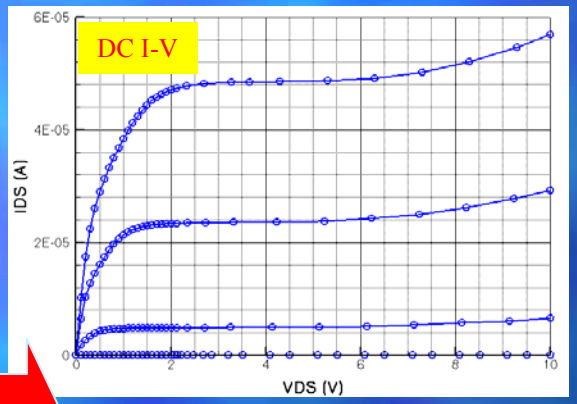
Research at a glance

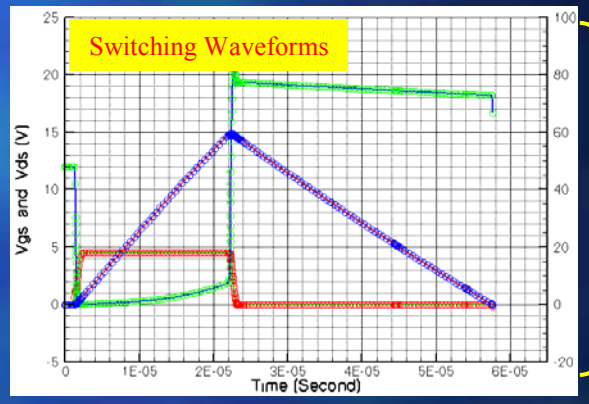
INPUT INFORMATION

OUTPUT INFORMATION

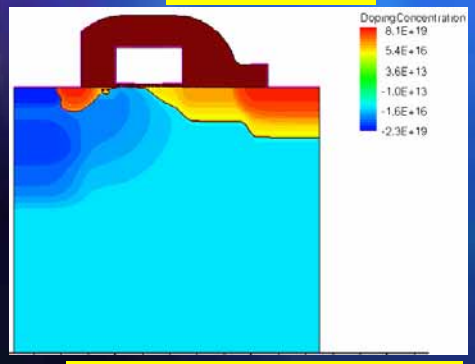


Circuit Setup

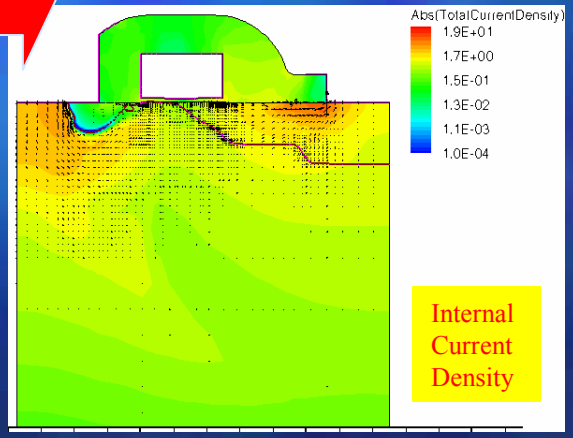


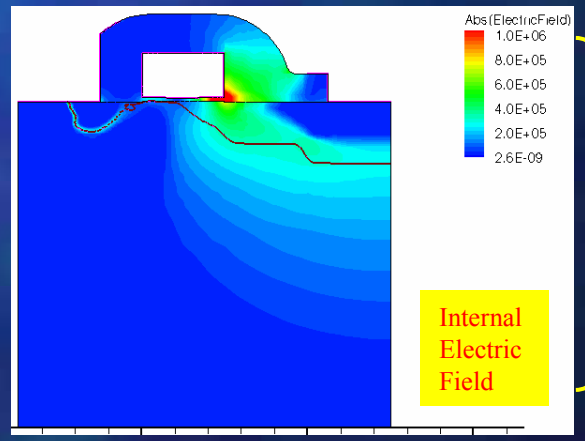


External Device Behavior



Device Structure (LDMOS)





Internal Device Physics

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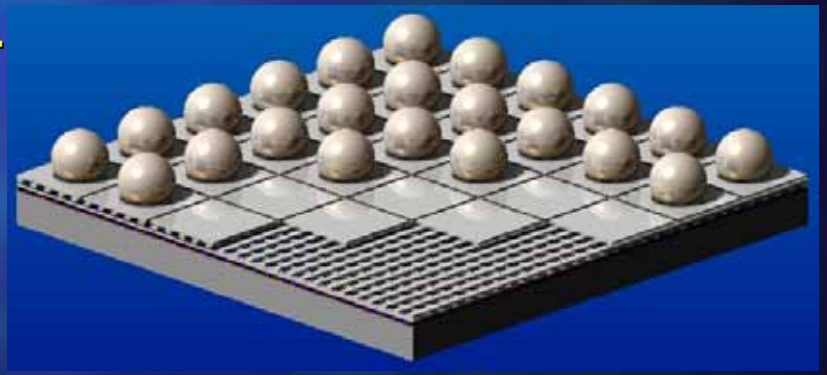
Research at a glance

Lateral Flip-Chip Power MOSFET for MHz-Frequency, High Density DC/DC Converters

- We have successfully developed an N-channel LDD MOSFET with a record low R_{DSON} of 1mΩ at a gate voltage of 6V or 1.20mΩ at a gate voltage of 4.5V, approximately 50% of the lowest R_{DSON} previously reported.
- The new device has a a performance FOM of less than 30 mΩ*nC, representing a 3X improvement over the state of the art trench MOSFETs.
- The new MOSFET demonstrates a breakdown voltage of 11V and is suitable for sub-10V class DC/DC applications.
- The MOSFET was fabricated with a 0.5µm simplified CMOS process of 10 masks including 3 metal layers.
- A DC/DC converter based on the MOSFET has been developed (by an industrial partner) to achieve a 3.5MHz switching frequency, 97-99% efficiency, and an amazing 970W/in^3 power density.



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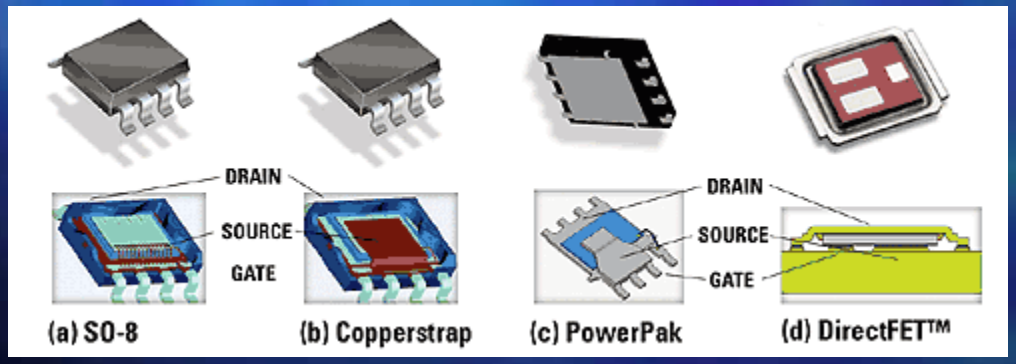
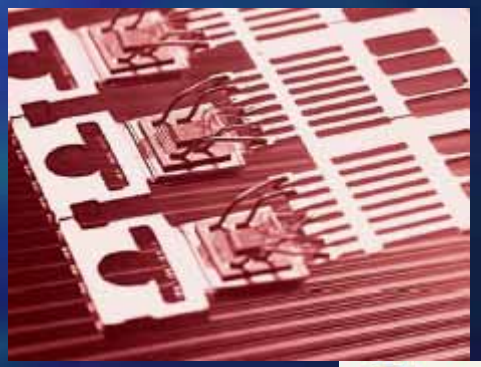
Research at a glance

Modeling and Minimization of Metal Interconnect Resistance in Power MOSFETs

- With the continuous reduction in on-resistance of power MOSFET to below 3-4 mΩ, the top metal resistance contribution become more and more significant. However, there is a lack of modeling tools to help device and package designers to minimize this effect.
- We are developing a Finite Element Analysis (FEA) tool to provide accurate calculation of the metal resistance contribution for various device layout, number and location of wirebond, and novel wirebondless packages (such as DirectFET or BGAFET).
- We will extend the study to lateral MOSFET in power ICs and Smart Power devices.





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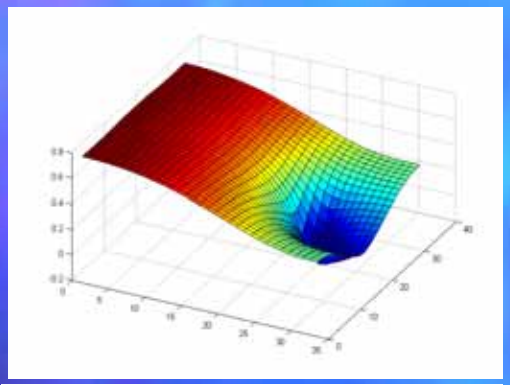
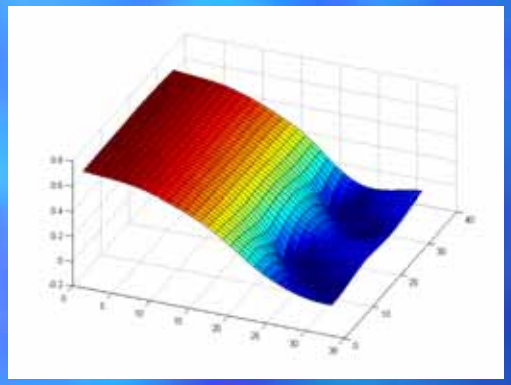
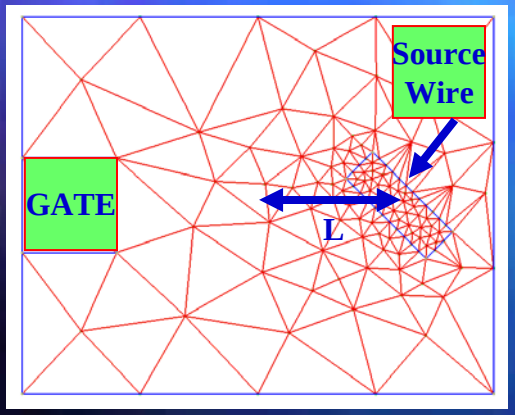
Research at a glance

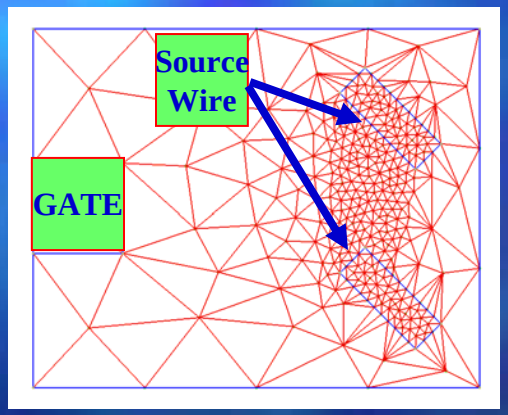
Modeling and Minimization of Metal Interconnect Resistance in D²PAK MOSFET



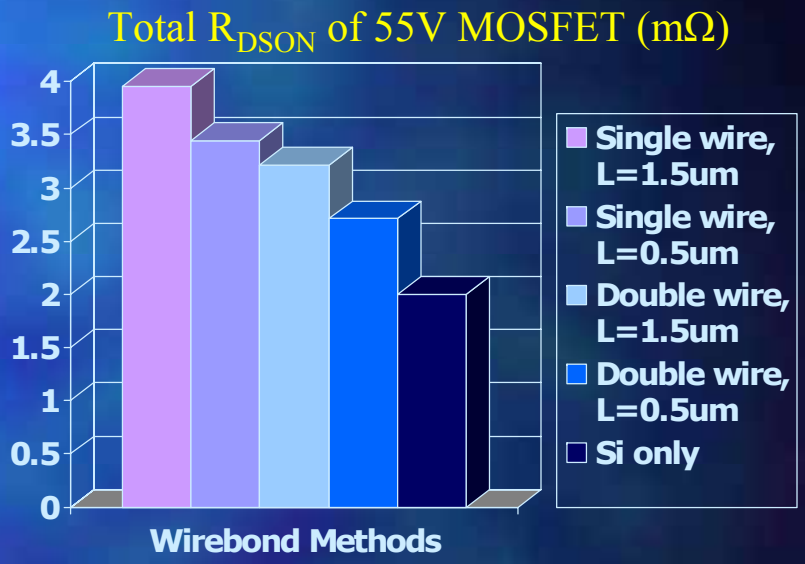




Single Source Wirebond



Double Source Wirebonds



- Finite Element Analysis (FEA) approach
- D²PAK Active Area=4x5mm²
- R_{DSON} of MOSFET (Si only)=40Ωmm²
- 3um Aluminum R= 10mΩ per square
- Wirebond Contact Area=0.4x1.2mm²

FloridaPEC

Power Electronics Research at Universities: Defining Our Role and Niche

Industry R&D

- Adequate budget and resources
- Experienced engineers
- Disciplined project management
- Product oriented

- Shorter term thinking
- More constraints in generating ideas
- Objective-oriented, more focused project team structures
- Skunk works are discouraged
- R&D jobs outsourced offshore
- Engineers are expensive

University Research

- Limited budget and resources
- Inexperienced graduate students
- Free-wheeling management style
- Education and training oriented

- Longer term thinking
- Less constraints in generating ideas
- Dynamic, interactive, interdisciplinary research and learning environment
- Skunk works are a way of life
- Offshore talents insourced to US
- Faculty/graduate students are inexpensive

University research in power electronics should compliment rather than duplicate industry R&D!!!

Summary

- There are tremendous challenges and opportunities co-existing in the field of power electronics in which university researchers can and should play an important role.
- UCF has well-established research capabilities in power electronics topology and control, magnetic elements, power semiconductor devices, packaging, modeling and simulation, and thermal management.
- UCF power electronics research team consists of experienced faculty in different expertise areas and a large graduate student talent pool. Team members work in a collaborative, interdisciplinary environment.
- Industrial partnership is absolutely essential.