Power Delivery Challenges in Computer Platforms Ed Stanford



Scaling Continues

Intel® Core[™] Duo 65nm Process 90.3 mm2 die size 151.6 million transistors





SRAM test-chip 45nm process 119 mm2 die size >1 billion transistors



2001 2002 2003 2004 2005 2006 2007 2008 2009 2010



Future options subject to change – Images not to scale

Through the Next Decade and Beyond





But Power Becomes a Dominant Design Factor With Simple Scaling



Note: Direct CMOS scaling relationships shown



Future options subject to change



Power Constrained Through Technology, Circuits and Architecture Innovations





Power Constrained Through Technology, Circuits and Architecture Innovations





CPU Power Delivery Impact



Impedance drops with lower operating voltages

Z=V_{tolerance}/I_{step},

 < 1u dielectric layer MLCC capacitors loose ~40-60% @ 1V dc, 10mV ac bias

• IE. 47 uF, 1206 = ~ 27 uF at use conditions



CPU Power Delivery Impact

Power Delivery Impedance Drives Capacitor Development



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Platform Power Delivery Impact









Up to 30% Board Area

Power delivery components



Platform Power Delivery Impact



Large Number of Regulators Drive dc-dc Density and Efficency









Desktop PC System Trends

Worldwide Desktop PC Form Factor Shipments, 2002-2008



SOURCE: IDC, Worldwide PC Client Form Factor Forecast: 2004-2008, April 2004.

All products, dates, and figures specified are preliminary based on current expectations, provided for planning purposes only, and are subject to change without notice. Projected data is merely a projection and has been simulated and is provided for informational purposes only.



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Similar Trends for Server Platforms



Source: IDC WW Quarterly Server and Workstation Trackers, Nov 2005



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Power Supply Density

Desktop Power Supplies

- 3 6 W/in³ * typical
- 68 -70 % efficient typical
- 80+ and other programs driving to > 80%

Server Power Supplies

- 6 12 W/in³ typical *
- 18 W/in³ state of art *

 EPA is currently revising efficency targets for both Desktop and Server products

* including fan and EMI filter





 Multi-Core Architecture and Other Techniques level Off CPU Power Consumption

- Regulator Impedance Driving New Decoupling Capacitor Technologies
- Smaller systems and more features per system drive up density and require higher efficency
- Government Regulations Driving up Power Supply Efficency Requirements

