Xseries, IntelliStation, BladeCenter Development

# APEC
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# Agenda

- Who we are
- What we need
- Requirements
- Summary

# Systems and Technology Group

## Who We Are

- **One of the Top:**
  - **Systems Vendors**
    - ***$22B Revenue in 2005***
  - **Fastest growing vendor in storage, UNIX servers and Intel-based servers**
- **Top blade-server vendor**
- **21 development sites World Wide**
- **10,000 development employees worldwide**

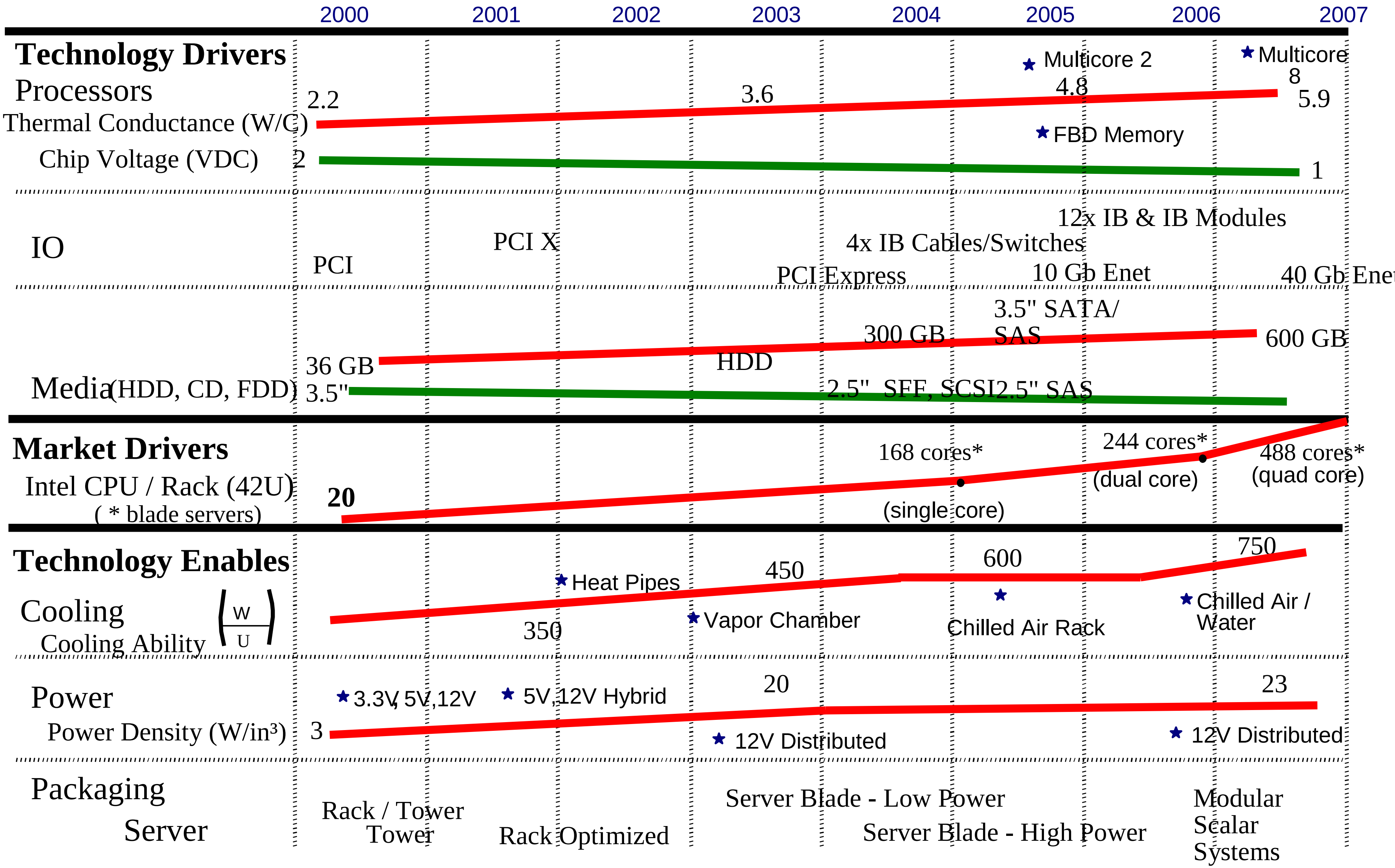
## What We Do

- ***IBM eServer***
  - ***zSeries mainframe***
  - ***iSeries midmarket***
  - ***pSeries UNIX***
  - ***xSeries Intel-based***
  - ***BladeCenter***
  - ***Systems Control Software***
- ***IBM TotalStorage***
  - ***Tape***
  - ***Disk***
  - ***Storage software***

# System Technology Challenges

- More speed!
- Higher Density!
- More data capacity!
- More bandwidth!
- Lower Cost!
- Smaller!
- More portable!
- More Open!

# Trends That Affect Power, Packaging & Cooling



# System Level Challenges:

- Server designs have reached several limits:
  - ***Power supply density: cooling a bottleneck, continued push higher***
  - ***Thermal: ability to move enough air to cool at server, rack and building levels***
  - ***Accoustics:  increased airfow = more noise***
- Ability to provide primary power, building and rack: over 30kW per rack
  - ***Higher power driving higher input currents***
    - ***Running out of AC ampacity with primary connector, C13/C14 must use C19/C20 and further as input connectors***
  - ***racks require more capacity than 60A 3-phase service***
- Other technology drivers
  - ***Number of planar voltages is increasing.***
    - ***To conserve planar area, VRMs & SIPs need to be more common / smaller***
  - ***Lower load voltages, 1.8V, 1.5V, 1.2V, etc., coupled with high dynamic loads continues to drive "point-of-load" VRs.***
  - ***Power Management***
    - ***Growing need to monitor currents and power***
    - ***Dynamic voltage adjustments***

# Power Challenges and Solutions:

## What we need

- **Higher Reliability – MTBF**
- **Higher Power Density**
- **Higher Transient Response - di/dt**
- **Higher Efficiency**
- **Lower Voltage - Higher Current**
- **Voltage/Current Distribution**
- **Increased Number Of Voltage Domains**
- **Ability to Hot Swap**
- **Lower Cost**
- **Shorter Development Cycles**
- **Best Industry Quality**
- **Error and Status Reporting**

## How we get there

- **More Integration**
- **Higher Switching Frequencies**
- **Lower Switching and Conduction Losses**
- **Topology Influences**
  - ***RES/ZVS/ZCS***
- **Better EMI Design**
- **Innovative Design**
- **Lower Output Impedance**
- **Thermal Management**
- **Component Improvements**
  - ***Integrated***
  - ***Battery Technology***
  - ***Power Semiconductors***
  - ***Capacitors***

# Power Supply Roadmap

## *General*

- ***N+N bulk power required for redundancy***
- ***12V distribution within the chassis drives VRM/VRD input, DASD, PCI, FANS***
- ***High efficiency converter technologies***
- ***Design for future power increases (mech. package, connectors)***
- ***Focus on quality and reliability***
- ***Voltage and current monitoring circuitry***

## *Low End*

- ***Density pressure will continue driving lower number of output voltages***
- ***Facilitates denser power supply packaging trend***
- ***Improved power supply efficiency***
- ***Requires more use of VRDs and VRMs Common Building Blocks***

## *Issues*

- ***Power supply densities limited at system level by cooling***
- ***Connector ratings / ac & dc power distribution (60A 3-phase) / Efficiencies***
- ***Need more robust communication link***

# Communication Link Challenges

- I2C is outdated and being abused
  - Over 10 years old
  - Developed in the age of single master and dumb devices
    - No Data Checking (CRC, ECC, etc.)
    - No Hot Plug Capability
    - Limited  throughput
    - Limited Isolation
  - Today's technology are smart devices, bus masters
    - Drives Multi-master, critical communications
- Consequence
  - Faulty Mastering
    - Bus Hangs
    - Slow Response
  - Limited Diagnosis Capability

# Link Issues

- Information content is in edges
  - di/dt approaching 1000A/uS - 6000A/ns
  - Noise
  - Reflections
- Ground shifts
- Card layout limitations
  - Bus runs next to signal wires
  - Distance between slaves
  - Bus length and loading
- Traffic bottlenecks.   Major areas:
  - Server Startup
  - Error recovery

# Requirements

- Differential front end
- Require minimum coding resources
- Check method (CRC, EEC, parity, etc)
- Effective bus mastering
- Interrupt driven
- Robust
- Cost effective
- Architecturally sound specification
- Simple validation and test

# Summary

- Need more of everything except cost and size
- Need a new communications link for the intelligent PS's
- The Industry has made tremendous strides ----- But
- More is needed

# Backup

# A Proposal

- Hardware
  - Arbitration
    - Handled by hardware only
    - No handshake protocol used
  - Merge I2C with SPI
    - Separate DATA IN and DATA OUT lines
    - Buffer CLOCK, DATA IN, DATA OUT
    - Supports longer nets, faster frequencies
    - Differential buffers can be used
- Firmware
  - Use standard I2C or PMBus protocol
  - Requires data checking