



AN INTRODUCTION TO IGBTs

by M. Melito, A. Galluzzo

INTRODUCTION

In the low and medium power range, Bipolar Junction Transistors (BJTs) have up to now been the most commonly used power semiconductors, and they still hold a large part of the market, despite some limitations due in part to the current drive (which can be uneconomic in terms of the number of components and the dimensions of the resulting circuits), and also the fact that minority carrier conduction places a limit on the maximum frequency of use.

The introduction of Power MOSFET (Metal Oxide Semiconductor Field Effect Transistor) devices allowed much simpler voltage drives to be used, and made operation at much higher frequencies possible, as conduction occurs with majority carriers. The use of this device has grown rapidly in low voltage

applications, but the dissipation characteristics in conduction have limited its use in high voltage.

IGBTs (Insulated Gate Bipolar Transistors) are a newer class of high voltage devices which combine the simplicity of drive of the MOS structure with the ability to handle high values of current typical of a bipolar device.

This paper includes a brief description of the structure and the physics of the device, followed by an analysis of the principal static and dynamic characteristics. Aspects of the device which must be considered to obtain maximum performance are also discussed, in particular the robustness in forward bias, reverse bias and short circuit, and the influence of gate polarisation.

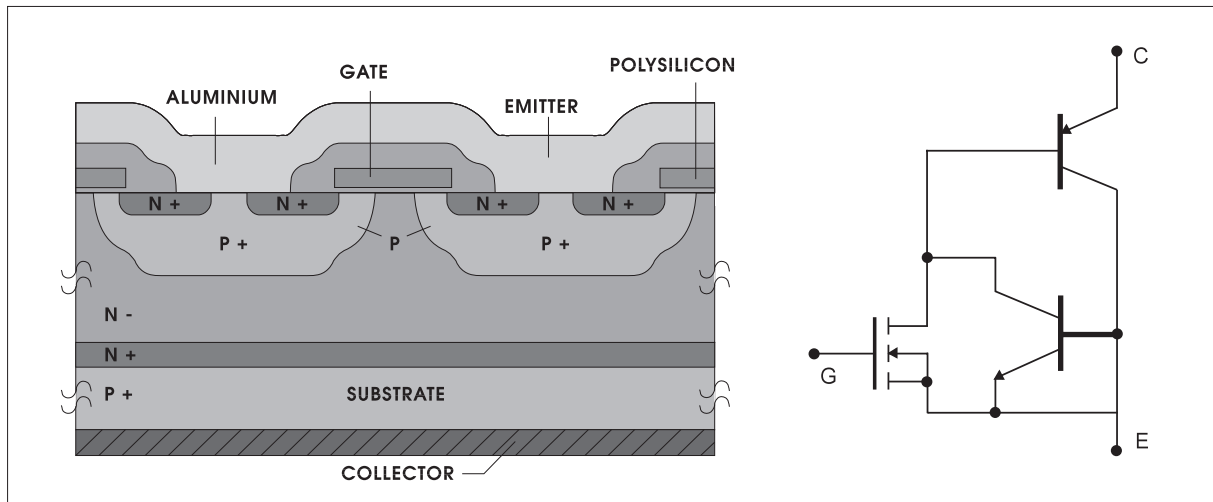
1 IGBT STRUCTURE

The IGBT is a natural evolution of the vertical Power MOSFET for high current, high voltage applications. It eliminates the main disadvantage of current high voltage Power MOSFETs, which is the high value of $R_{DS(on)}$ caused by the high resistivity of the source-drain path necessary to obtain a high breakdown voltage BV_{DSS} . The lower $V_{CE(sat)}$ which can be obtained with IGBTs allows operation with a current density much higher than that which can be achieved with bipolar devices; alternatively, under the same conditions, the $V_{CE(sat)}$ of the IGBT is lower. The vertical section shown in figure 1 together with the equivalent circuit shows

that the structure of the IGBT is very similar to that of a Power MOSFET. The fundamental difference is in the addition of a p^+ type substrate. In this way a junction is created with the n^- area of the collector; such a junction injects holes into the n^- area during conduction, modulating the resistance and significantly reducing the $V_{CE(sat)}$ of the device.

When the device is blocked there is no injection of holes and consequent modulation of resistance, and so the breakdown voltage of the IGBT depends only on the doping and the thickness of the n^- region.

Figure 1: IGBT Basic Structure



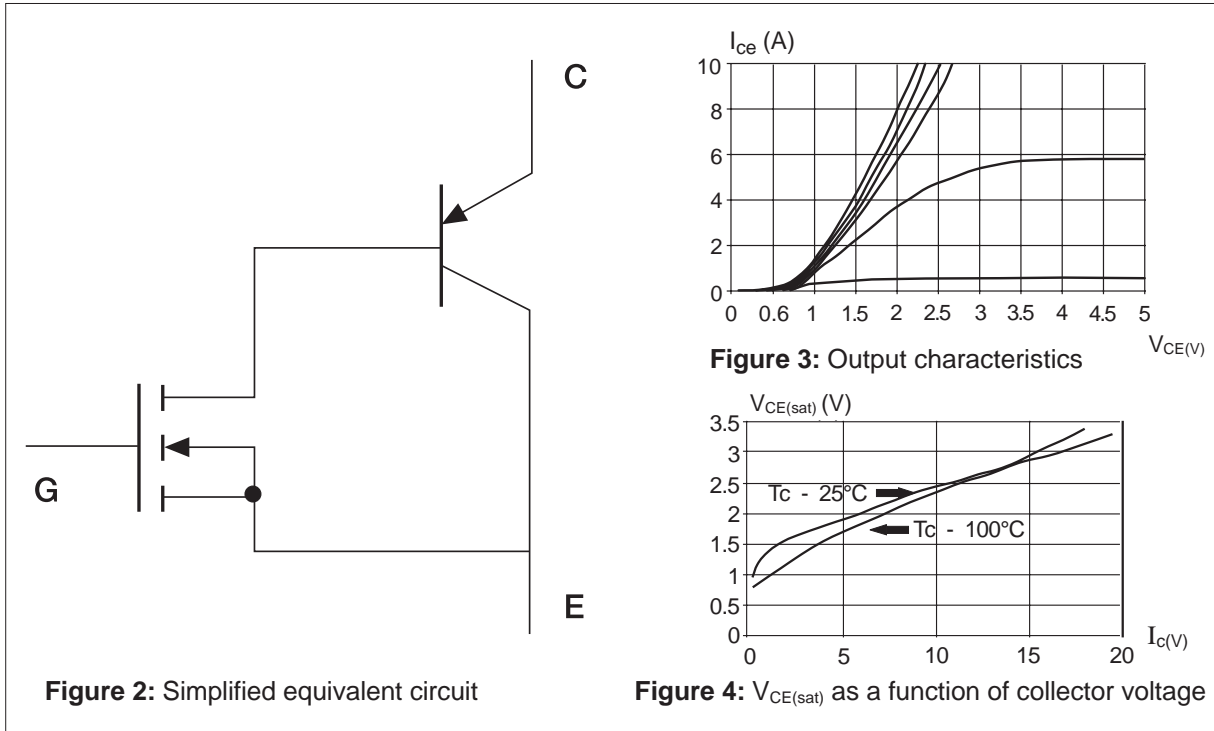
2 STATIC CHARACTERISTICS

The IGBT can be modelled, as a first approximation, as a pnp transistor driven by a Power MOSFET. Figure 2 shows only the elements of the structure necessary for the understanding of the operation of the device; ignoring, for the moment, the parasitic elements. The output characteristics of the IGBT are shown in figure 3, and it can be seen that they are very similar to those of a Darlington type bipolar device.

2.1 Temperature dependence

As the IGBT structure includes both a bipolar and a Power MOSFET, its temperature characteristics depend on the net effect of the two components, which have contrasting properties. The Power MOSFET has a positive temperature coefficient, while that of the bipolar is negative. Figure 4 shows the change in $V_{CE(sat)}$ as a function of the collector current for two different values of junction temperature.

Figures : 2,3 & 4



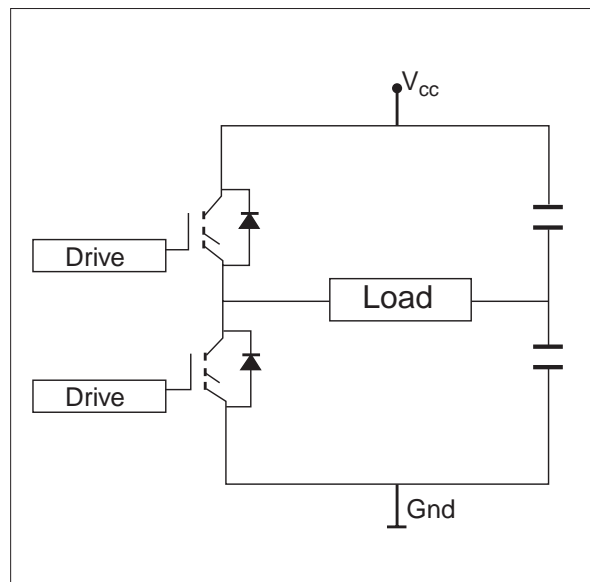
3 DYNAMIC CHARACTERISTICS

The equivalent circuit of the input of the IGBT is of a MOSFET type and so is purely capacitive. This allows the use of voltage drive which means that it is possible to have a less complex circuit with lower power consumption than that required by a bipolar device.

3.1 Gate Polarisation Voltage and Drive Resistance

The gate drive voltage generally adopted is 15V both to obtain a saturation voltage large enough to have negligible conduction losses, and because the information provided in data sheets refers to such a value which has almost become a standard. In some circuit configurations, for example the half bridge shown in figure 5, the increased value of dV/dt generated by the turn off of one of the devices can cause the accidental turn on of the other. A high value of dV/dt applied between the collector and the emitter can cause, due to the collector-gate capacitance

Figure 5: Half Bridge circuit



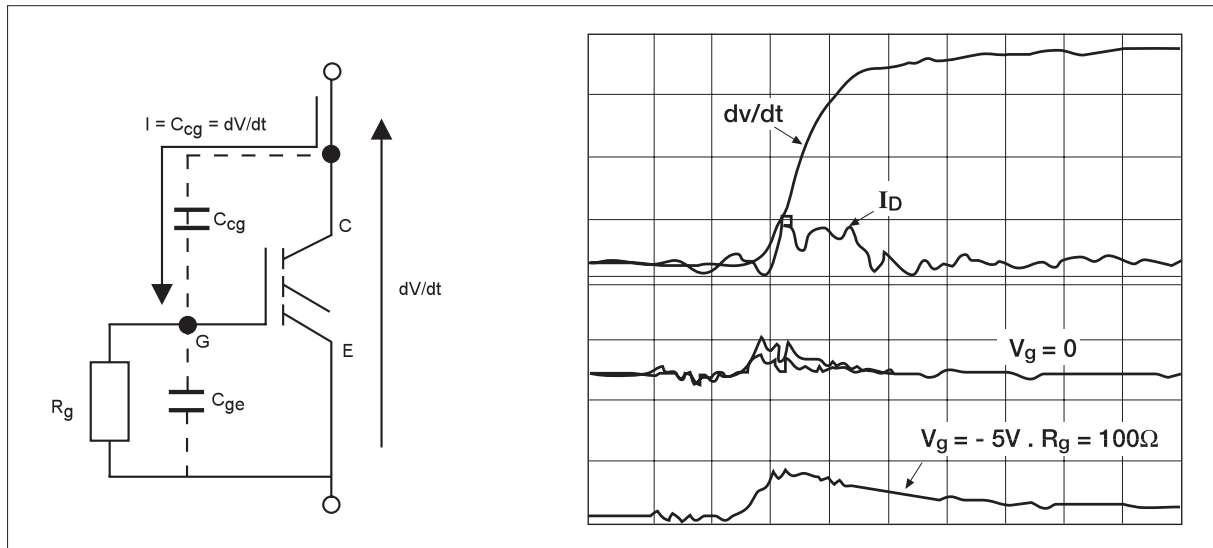
(C_{res}) and the impedance of the drive circuit (R_g, C_{ies}), the turn on of the device at high currents and voltages. Such undesirable behaviour is not generally destructive, but can cause large power dissipation. To

APPLICATION NOTE

prevent this problem arising the MOSFET should be driven with a negative offset (typically 5V is sufficient) and with the lowest drive impedance possible compatible with

the demands of the RBSOA (which will be discussed later). Figure 6 shows waveforms demonstrating the effect of dV/dt , along with the relevant equivalent circuit.

Figure 6: Effect of dV/dt



3.2 Turn on

The turn on behaviour of the IGBT is identical to that of the Power MOSFET, and the turn on time is a function of the output impedance of the drive circuit and the applied gate voltage. It is possible to control the turn on

speed of the device by choosing an appropriate value of gate resistance. Figure 7 shows waveforms for the switching of an inductive load, and the equivalent circuit.

Figure 7: Turn-on with inductive load

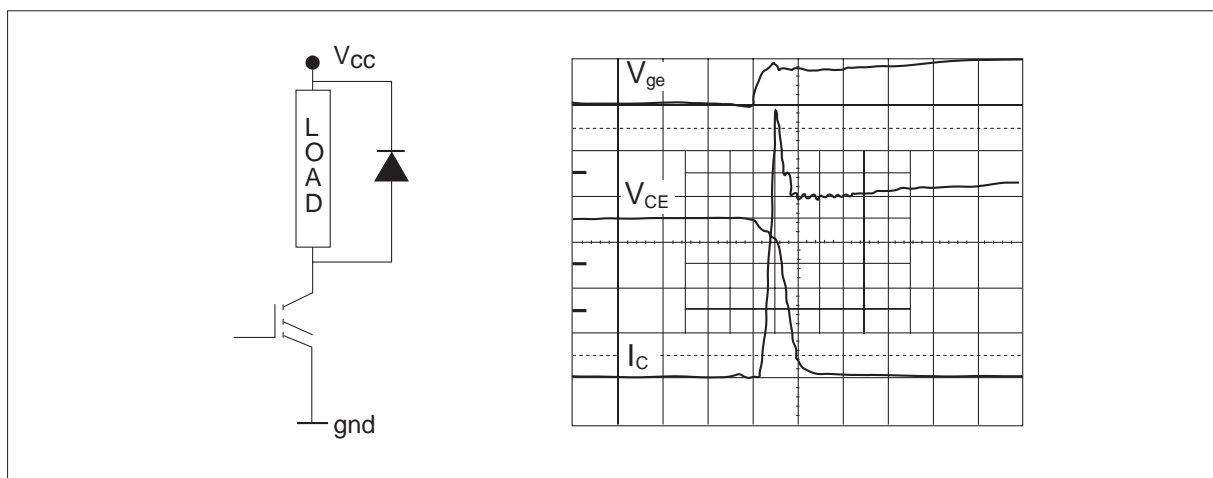


Figure 8 shows the variation of the current gradient with the value of the gate resistance for a typical device.

Turn on losses can be calculated using the following relationship:

$$E_{on} \approx 0.5 * V_{CC} * (I_O + I_{RM})^2 * (dl/dt)^{-1}$$

This is shown graphically in figure 9.

Figure 8: dl/dt as a function of drive resistance

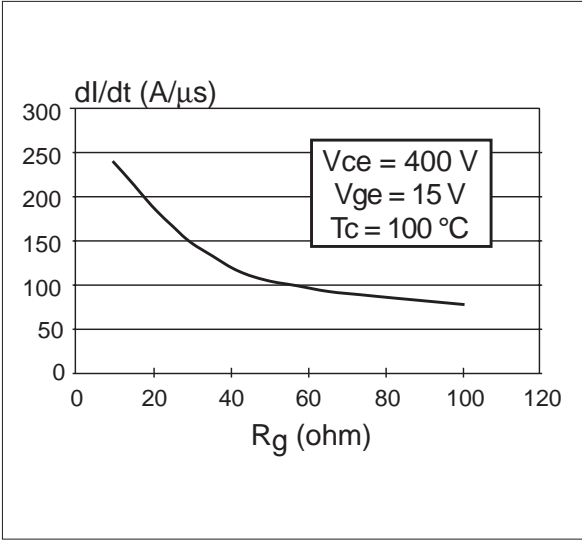
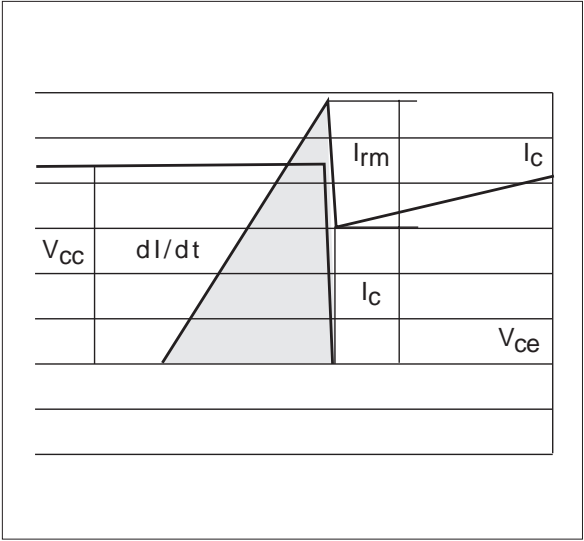


Figure 9: Calculation of energy dissipated in turn on of inductive load

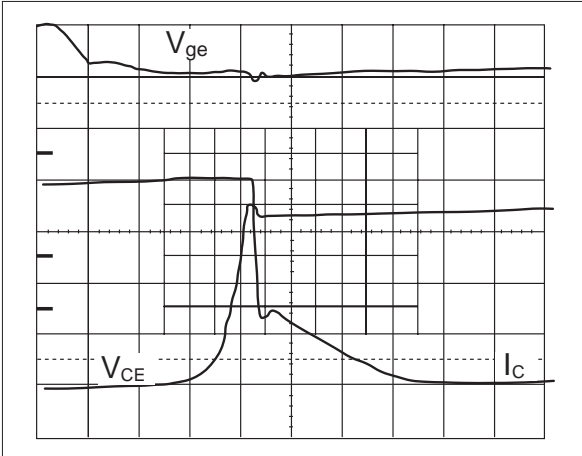


3.3 Turn off

The turn off behaviour has typical characteristics of both Power MOSFET and BJT devices. The turn off waveform shown in figure 10 shows distinct phases.

During the first phase, the gate voltage decreases to a value at which the Miller effect begins and the V_{CE} starts to increase. In the second phase the gate voltage remains constant because of the modulation of the collector-gate capacitor by V_{CE} which continues to increase to its maximum value at a rate controlled by the drive circuit. The third phase, which defines t_{fall} , can be divided, with respect to the collector current, into two parts: the first, very fast and due to the turn off of the MOSFET part of the device; the second slower and caused by the recombination of the minority carriers that cannot be extracted from the base of the pnp bipolar section which is already open. The length of this “tail” depends essentially on the lifetime of these carriers.

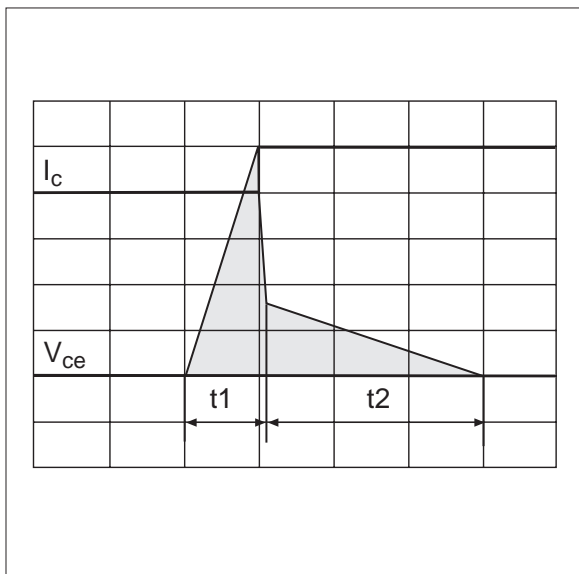
Figure 10: Turn off with inductive load



APPLICATION NOTE

Figure 11 shows that the energy dissipated at turn off can be considered as being due the result of two elements: the first is tied to the speed at which the collector voltage reaches its maximum voltage; the second to the duration of the tail of the collector current.

Figure 11: Calculation of energy dissipated in turn-off of inductive load



In total:

$$E_{\text{off}} = 0.5 * (I_C * t_1 + I_{\text{tail}} * t_2) * V_{CC}$$

To minimise this energy, at a fixed I_C , V_C and temperature it is only possible to affect t_1 . This parameter can be controlled via the gate resistor. The contribution of the tail, related to the value of I_{tail} and to its duration, depends strongly on the junction temperature and on the values of I_C and V_D . Figures 12-15 show, for a typical device, the variation in dV_C/dt as a function of R_g , and the variation of I_{tail} as a function of I_C , V_D and T_C .

Figure 12: dV/dt as a function of drive resistance

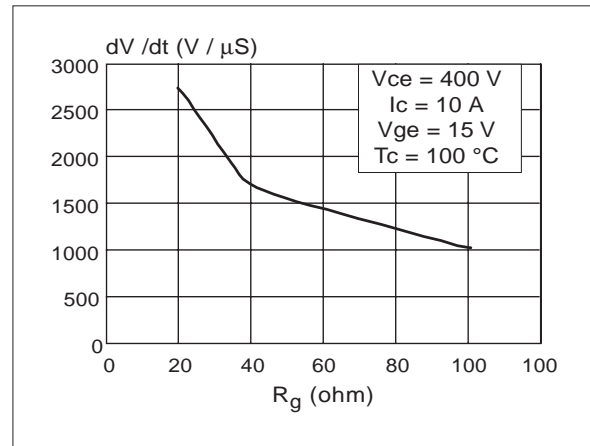


Figure 13: I_{tail} as a function of I_C

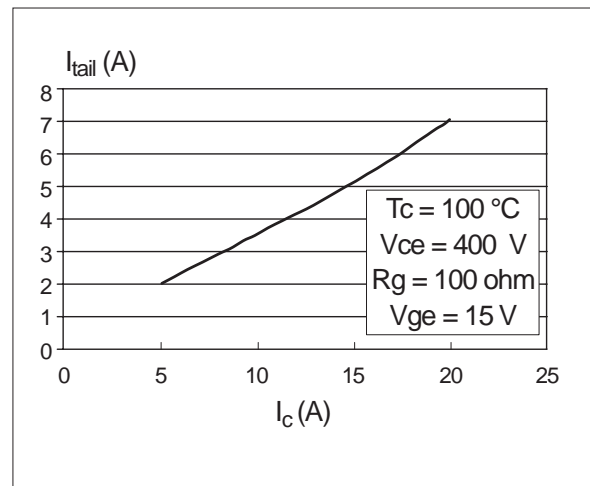


Figure 14: I_{tail} as a function of clamp voltage

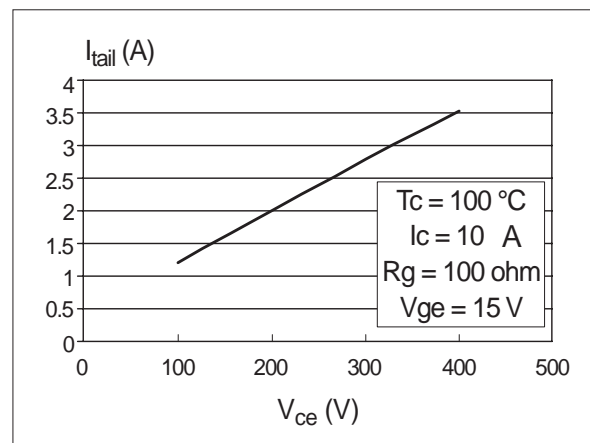
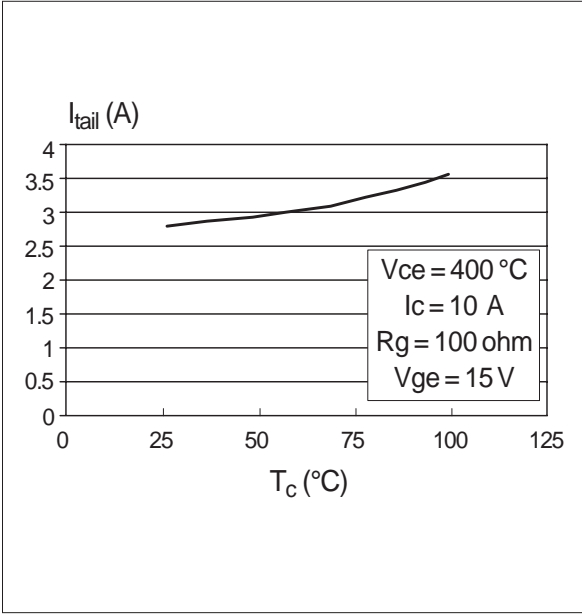


Figure 15: I_{tail} as a function of temperature



The total power dissipated in the device is:

$$P_d = (I_{(AV)} * E_O + I_{(RMS)}^2 * R) * \delta + (E_{on} + E_{off}) * f$$

$I_{(AV)}$ = Mean Current
 $I_{(RMS)}$ = Effective Current
 δ = Duty Cycle
 R = Differential Resistance
 f = frequency

This formula was used to calculate the continuous power dissipation in the approximation of the output characteristics shown in figure 16. Figure 17 shows the variation of switchable power with switching frequency, with the device held a constant voltage and the current adjusted such that the power dissipated by the device remains constant at 10W.

3.4 Maximum Operating Frequency

The dissipation of power during switching limits the maximum operating frequency of electronic switches. The junction temperature during normal operation depends on the amount of power dissipated from the device and on the efficiency of the cooling system:

$$T_j = T_{ambient} + P_d * R_{th(ja)}$$

The more efficient the heatsink on which the device is mounted, the lower the case temperature, the greater the temperature difference allowed between case and junction, and therefore the greater the power that can be dissipated. T_j should be maintained as low as possible with the smallest size, and hence cost, of heatsink possible. In practice it is acceptable to have, with a switchable power of 10kW, a maximum power of 10W dissipated in the device.

Figure 16: Approximation of output characteristics

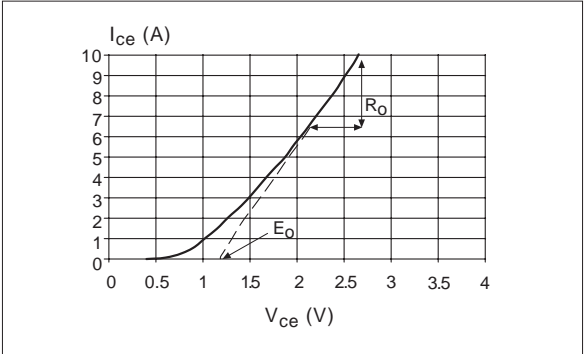
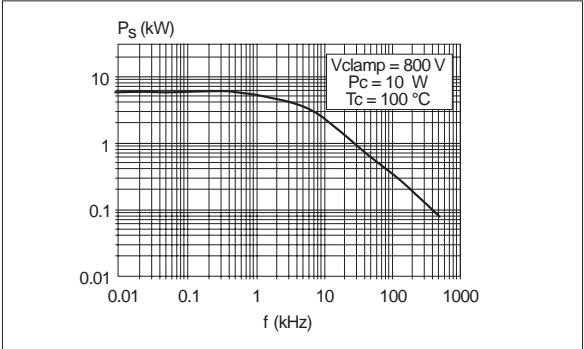


Figure 17: Switchable power at constant dissipated power



APPLICATION NOTE

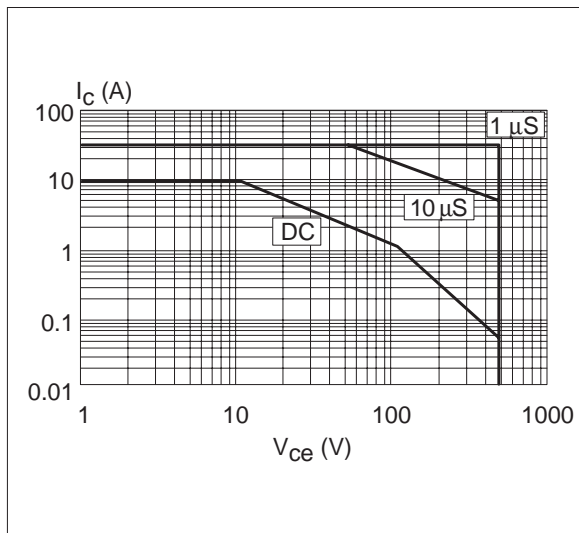
4 SAFE OPERATING AREA

A power device must have a safe operating area large enough in terms of switchable current and voltage and also to allow it to survive in anomalous conditions, for example short circuit, for a long enough time to allow protection circuits to take action. Typically the curves describing robustness in forward conduction (Forward Bias Safe Operating Area, FBSOA), in reverse (Reverse Bias Safe Operating Area, RBSOA), and in short circuit are available.

4.1 FBSOA

The forward conduction robustness characteristics of the IGBT are more similar to those of the Darlington than to those of a Power MOSFET. The FBSOA graph shown in figure 18 shows a variation in the gradient, which depends on an effect known as secondary breakdown which does not occur in the Power MOSFET.

Figure 18: FBSOA



4.2 RBSOA

In the equivalent circuit of the IGBT shown in figure 1 shows the presence of a parasitic

nnp transistor. This transistor, together with the pnp, forms an SCR, which in certain conditions can trigger. When this occurs, the device can no longer be controlled via the gate. The latest IGBTs do not exhibit this type of behaviour, since with appropriate modifications to the structure and the process the triggering of this parasitic SCR can be made to occur at a current much higher than that encountered in normal operation (typically $I_{latch} > 5 * I_{nominal}$). Figures 19 and 20 show the variation in latch current as a function of junction temperature and gate resistance respectively.

Figure 19: I_{latch} as a function of junction temperature

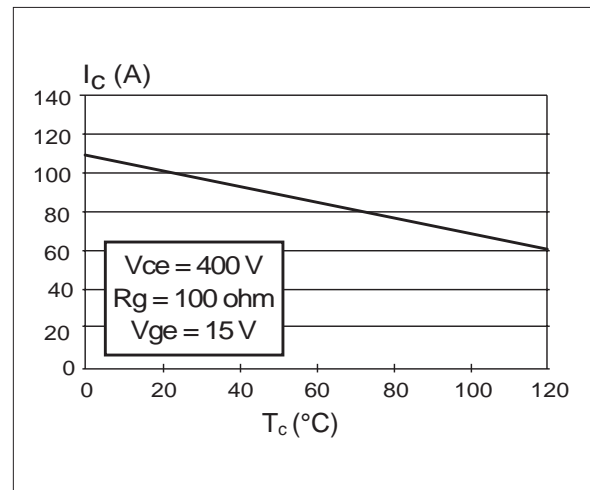
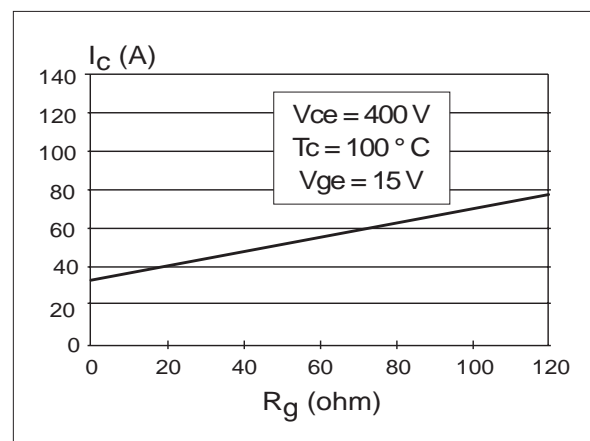


Figure 20: I_{latch} as a function of drive resistance

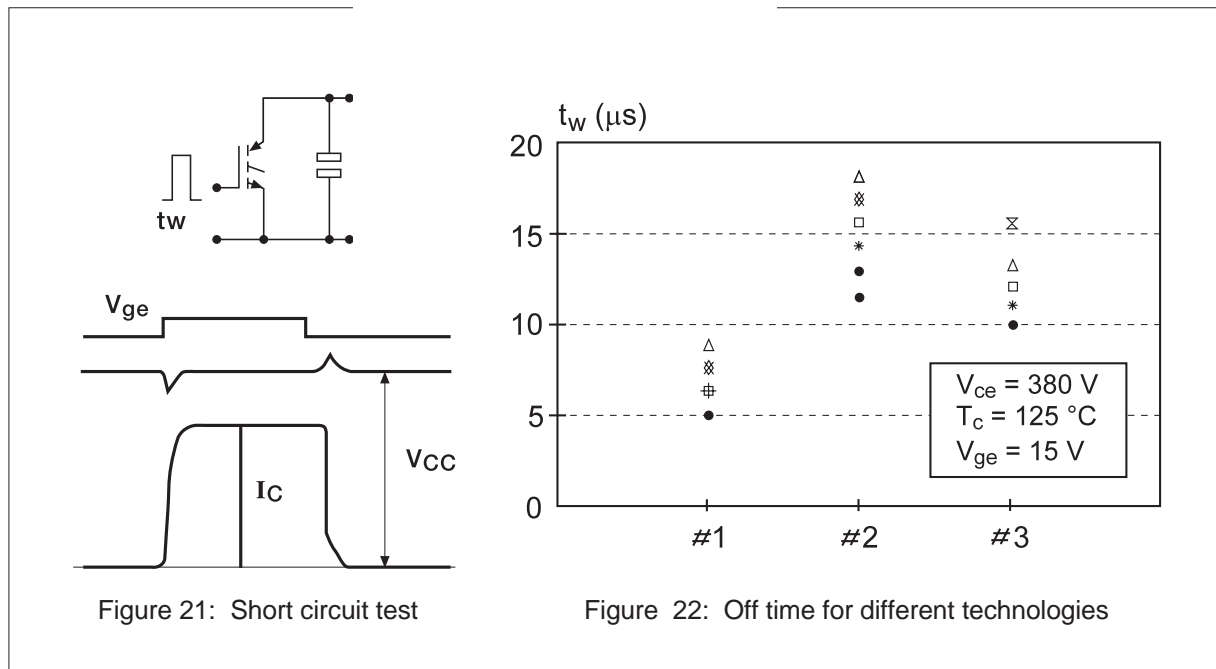


4.3 Short Circuit Robustness

This is measured by turning on the device at the supply voltage and measuring the maximum time during which the drive circuit can control the device under test. Figure 21

shows the shape of the waveform and figure 22 the off time for three devices with equivalent characteristics but manufactured using different technologies.

Figures : 21 and 22



5 FUTURE DEVELOPMENTS

The particular structure of the IGBT means that the turn off of the device is controlled by the turn off of the pnp bipolar which, in practice, turns off with an open base. For this reason the switching can only end after the recombination of the excess minority carriers in the base region of the pnp, which therefore dominate the turn off behaviour.

To increase the speed of the turn off characteristics of the device requires the adoption of techniques to reduce the minority carrier lifetime, through which the t_{fall} of the IGBT can be reduced to a time in the order of hundreds of nanoseconds.

The technique involves doping the device with gold or platinum, irradiation with electrons, or bombardment with heavy ions.

Changes can also be made at the structural level, for example the introduction of a buried n+ type layer, see figure 1, between the base and emitter of the pnp. This results in both an increase in the turn off speed, and an improvement in the robustness due to the decrease in the gain of the parasitic transistors. The optimisation of the above technique allows the best compromise between the conflicting demands of speed, current handling capability and robustness, eliminating the inconveniences of first generation IGBTs.

The latest generation IGBTs are at least twice as fast as the first, and the RBSOA is rectangular.

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 1999 STMicroelectronics - Printed in Italy - All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>